HYMA6V16730E14HGTG
16Mx72 buffered EDO DRAM DIMM

PRELIMINARY

Description

The HYMA6V16730E14HGTG familiy is an 16Mx72 bits Dynamic RAM Module which is assembled 18 pieces of 16Mx4bit DRAMs in 32pin TSOP-II package and two 16bit driver ICs in 48pin TTSOP package mounted on a 168pin printed circuit board with decoupling capacitors.

The HYMA6V16730E14HGTG is optimized for application to the systems which are required high density and large capacity such as main memory of the computers and an image memory systems, and to the others which are requested compact size.

The HYMA6V16730E14HGTG provides common data inputs and extended data outputs

Features

- Extended data output(EDO) mode capability
- All inputs and outputs TTL compatible
- /RAS only refresh, /CAS before /RAS refresh,Hidden refresh capability
- Single Power supply
- 4K Refresh cycle / 64ms
- 168pins Dual In-Line Package
  - HYMA6V16730E14HGTG : Gold plating
- Low power
  - active : 9144/8496mW(Max)
  - standby : 105mW(CMOS level : Max)

***Fast access time & cycle time**

Part No	tRAC	tCAC	tRC	tHPC
HYMA6V16730E14HGTG-5	50ns	18ns	84ns	20ns
HYMA6V16730E14HGTG-6	60ns	20ns	104ns	25ns

Ordering Information

Part No.	Power Suppy	Clock Frequency	Interface	Form Factor
HYMA6V16730E14HGTG-5	3.3V	50ns	TTL	168pin buffered DIMM 5.25x1.25 inch
HYMA6V16730E14HGTG-6		60ns		

Pin Description

Pin	Pin Description	Pin	Pin Description
A0, B0, A1~A11	Address Inputs	/PDE	Presence Detect Enable
DQ0 ~ DQ71	Data Input / Output	Vcc	Power (+3.3V)
/RAS0, /RAS2	Row Address Strobe	Vss	Ground
/CAS0, /CAS4	Column Address Strobe	NC	No connection
/WE0, /WE2	Read / Write Enable	/OE0, /OE2	Output Enable
PD 1~8	Presence Detect	RSVD	Reserved Use
ID 0~1	ID bit	RFU	Reserved for future use

Pin Assignment

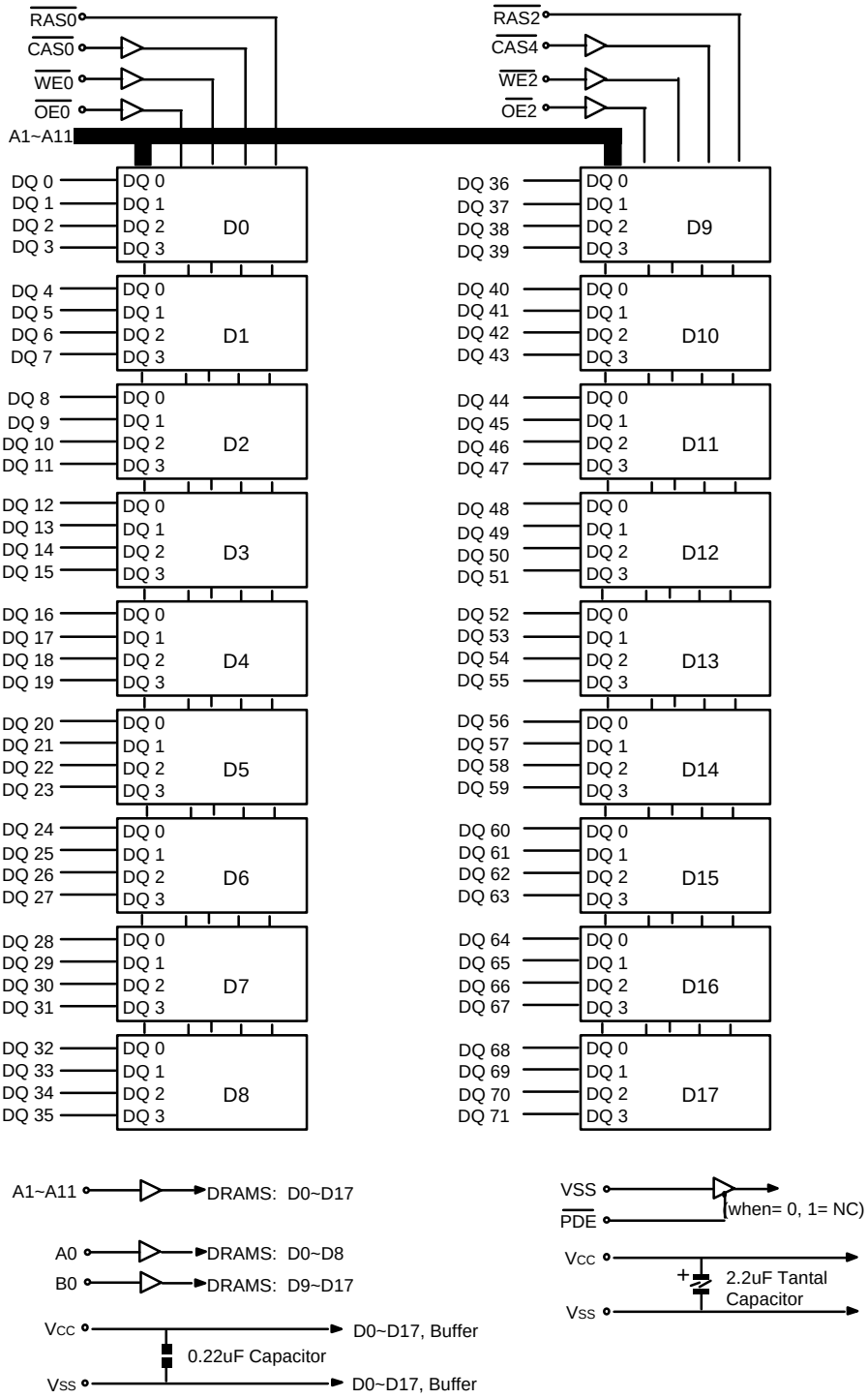
Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	Vss	29	RSVD	57	DQ22	85	Vss	113	RSVD	141	DQ58
2	DQ0	30	/RAS0	58	DQ23	86	DQ36	114	/RAS1*	142	DQ59
3	DQ1	31	/OE0	59	Vcc	87	DQ37	115	RFU	143	Vcc
4	DQ2	32	Vss	60	DQ24	88	DQ38	116	Vss	144	DQ60
5	DQ3	33	A0	61	RFU	89	DQ39	117	A1	145	RFU
6	Vcc	34	A2	62	RFU	90	Vcc	118	A3	146	RFU
7	DQ4	35	A4	63	RFU	91	DQ40	119	A5	147	RFU
8	DQ5	36	A6	64	RFU	92	DQ41	120	A7	148	RFU
9	DQ6	37	A8	65	DQ25	93	DQ42	121	A9	149	DQ61
10	DQ7	38	A10	66	DQ26	94	DQ43	122	A11	150	DQ62
11	DQ8	39	A12*	67	DQ27	95	DQ44	123	A13*	151	DQ63
12	Vss	40	Vcc	68	Vss	96	Vss	124	Vcc	152	Vss
13	DQ9	41	RFU	69	DQ28	97	DQ45	125	RFU	153	DQ64
14	DQ10	42	RFU	70	DQ29	98	DQ46	126	B0	154	DQ65
15	DQ11	43	Vss	71	DQ30	99	DQ47	127	Vss	155	DQ66
16	DQ12	44	/OE2	72	DQ31	100	DQ48	128	RFU	156	DQ67
17	DQ13	45	/RAS2	73	Vcc	101	DQ49	129	/RAS3*	157	Vcc
18	Vcc	46	/CAS4	74	DQ32	102	Vcc	130	/CAS5*	158	DQ68
19	DQ14	47	RSVD	75	DQ33	103	DQ50	131	RSVD	159	DQ69
20	DQ15	48	/WE2	76	DQ34	104	DQ51	132	/PDE	160	DQ70
21	DQ16	49	Vcc	77	DQ35	105	DQ52	133	Vcc	161	DQ71
22	DQ17	50	RSVD	78	Vss	106	DQ53	134	RSVD	162	Vss
23	Vss	51	RSVD	79	PD1	107	Vss	135	RSVD	163	PD2
24	RSVD	52	DQ18	80	PD3	108	RSVD	136	DQ54	164	PD4
25	RSVD	53	DQ19	81	PD5	109	RSVD	137	DQ55	165	PD6
26	Vcc	54	Vss	82	PD7	110	Vcc	138	Vss	166	PD8
27	/WE0	55	DQ20	83	ID0	111	RFU	139	DQ56	167	ID1
28	/CAS0	56	DQ21	84	Vcc	112	/CAS1*	140	DQ57	168	Vcc

Note : Pins marked * are not used in this module

Presence Detect Pins(Optional)

Pin	50ns	60ns	Pin	50ns	60ns
PD1	1	1	PD6	0	1
PD2	1	1	PD7	0	1
PD3	1	1	PD8	0	0
PD4	1	1	ID0	0	0
PD5	1	1	ID1	0	0

Functinal Block Diagram



Absolute Maximum Ratings* (TA=0 to 70 °C)

Parameter	Symbol	Rating	Unit
Ambient Temperature	T_A	0 ~ 70	°C
Storage Temperature	T_{STG}	-55 ~ 125	°C
Voltage on Any Pin relative to V_{SS}	$V_{IN / OUT}$	-0.5 ~ 4.6	V
Voltage on V_{CC} relative to V_{SS}	V_{CC}	-0.5 ~ 4.6	V
Short Circuit Output Current	I_{OUT}	50	mA
Power Dissipation	P_D	21	W

*Note : 1.Stress greater than above absolute maximum ratings may cause permanent damage to the device

Recommended DC Operating Conditions (TA=0 to 70 °C)

Parameter	Symbol	Min	Typ.	Max	Unit	Note
Power Supply Voltage	V_{CC}	3.0	3.3	3.6	V	1
Input High Voltage	V_{IH}	2.0	-	V_{CC} + 0.3	V	1
Input Low Voltage	V_{IL}	-0.3	-	0.8	V	1

* Note : 1. All voltage referenced to Vss

DC Electrical Characteristics (TA = 0 ~ 70°C, Vcc = 3.3V +/- 0.3V)

Symbol	Parameter		Min	Max	Unit	Note
VOH	Output Level Output "H" Level voltage(Iout= -2mA)		2.4	Vcc	V	
VOL	Output Level Output "L" Level voltage(Iout=2mA)		0	0.4	V	
ICC1	Operating current Average power supply operating current (/RAS, /CAS Cycling : tRC = tRC min)	50ns	-	2540	mA	1, 2
		60ns	-	2360		
ICC2	Standby current (TTL interface) Power supply standby current (/RAS, /UCAS,/LCAS=VIH, Dout = High-Z)		-	56	mA	
ICC3	/RAS only refresh current Average power supply current /RAS only refresh mode (/RAS cycling, /CAS=VIH, tRC= tRC min)	50ns	-	2540	mA	2
		60ns	-	2360		
ICC4	Extended data out page mode current (/RAS=VIL, /CAS, Address cycling : tHPC=tHPC min)	50ns	-	2000	mA	1, 3
		60ns	-	1820		
ICC5	Standby current (CMOS) Power supply standby current (/RAS, /UCAS, /LCAS >= Vcc-0.2V, Dout = High-Z)		-	29	mA	
ICC6	/CAS-before-/RAS refresh current (tRC=tRC min)	50ns	-	2540	mA	
		60ns	-	2360		
ICC7	Battery back up operating current (standby with CBR) (tRC=31.25us, tRAS=300ns, Dout=High-Z)		-	110	uA	1
II(L)	Input leakage current, Any input (0V<= Vin<=Vcc)		-5	5	uA	
IO(L)	Output leakage current, (Dout is disabled, 0V<= Vout<=Vcc)		-5	5	uA	

Note : 1. Icc depends on output load condition when the device is selected. Icc(max) is specified at the output open condition
2. Address can be changed once or less while /RAS = VIL
3. Address can be changed once or less while /CAS = VIH

Capacitance (Vcc = 3.3V +/- 0.3V, TA = 25C, f = 1MHz)

Parameter	Symbol	Min.	Max	Unit	Note
Input capacitance (A0 ~ A12, B0)	CI1	-	20	pF	1
Input capacitance (/WE0, /WE2, /OE0,/OE2)	CI2	-	20	pF	1,2
Input capacitance (/RAS0, /RAS2)	CI3	-	65	pF	1,2
Input capacitance (/CAS0, /CAS4)	CI4	-	20	pF	1,2
Output capacitance (DQ0 ~ DQ71)	CI/O	-	20	pF	1, 2

Note : 1. Capacitance measured with Boonton Meter or effective capacitance measuring method
2. /CAS = VIH to disable Dout

AC Characteristics (Vcc=3.3V +/-10%, TA=0~70C, Note 1, 2, 19)

Test Condition

- Input rise and fall times : 2ns
- Input level : V_{IL} / V_{IH} = 0.0 / 3.0V
- Input timing reference levels : V_{IL} / V_{IH} = 0.8 / 2.0V
- Output timing reference levels : VOL / VOH = 0.8 / 2.0V
- Output load : 1 TTL gate + C_L(100pF) (Including scope and jig)

Read, Write, Read-modify-write and Refresh Cycles

Parameter	Symbol	-50		-60		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	tRC	84	-	104	-	ns	
/RAS precharge time	tRP	30	-	40	-	ns	
/CAS precharge time	tCP	8	-	10	-	ns	
/RAS pulse width	tRAS	50	10,000	60	10,000	ns	
/CAS pulse width	tCAS	8	10,000	10	10,000	ns	
Row address set-up time	tASR	5	-	5	-	ns	
Row address hold time	tRAH	8	-	10	-	ns	
Column address set-up time	tASC	0	-	0	-	ns	
Column address hold time	tCAH	8	-	10	-	ns	
/RAS to /CAS delay time	tRCD	12	32	14	40	ns	3
/RAS to Column address delay time	tRAD	10	20	12	25	ns	4
/RAS hold time	tRSH	18	-	20	-	ns	
/CAS hold time	tCSH	35	-	40	-	ns	
/CAS to /RAS precharge time	tCRP	10	-	10	-	ns	

- continued -

Parameter	Symbol	-50		-60		Unit	Note
		Min	Max	Min	Max		
/OE to Din delay time	tODD	18	-	20	-	ns	5
/OE delay time from Din	tDZO	0	-	0	-	ns	6
/CAS delay time from Din	tDZC	0	-	0	-	ns	6
Transition time (Rise and Fall)	tT	2	50	2	50	ns	7
Refresh period	tREF	-	64	-	64	ms	4K Ref.

Read Cycles

Parameter	Symbol	-50		-60		Unit	Note
		Min	Max	Min	Max		
Access time from /RAS	tRAC	-	50	-	60	ns	8, 9
Access time from /CAS	tCAC	-	18	-	20	ns	9,10,17
Access time from column address	tAA	-	30	-	35	ns	9,11,17
Access time from /OE	tOAC	-	18	-	20	ns	9
Read command set-up time	tRCS	0	-	0	-	ns	
Read command hold time to /CAS	tRCH	0	-	0	-	ns	12
Read command hold time to /RAS	tRRH	0	-	0	-	ns	12
Column address to /RAS lead time	tRAL	30	-	35	-	ns	
Column address to /CAS lead time	tCAL	15	-	18	-	ns	
Output buffer turn off delay time from /CAS	tOFF	-	18	-	20	ns	13,21
Output buffer turn off delay time from /OE	tOEZ	-	18	-	20	ns	13
/CAS to Din delay time	tCDD	18	-	20	-	ns	5
/RAS to Din delay time	tRDD	13	-	15	-	ns	
/WE to Din delay time	tWDD	13	-	15	-	ns	
Output buffer turn off delay time from /RAS	tOFR	-	13	-	15	ns	13,21
Output buffer turn off delay time from /WE	tWEZ	-	13	-	15	ns	13
Output data hold time	tOH	3	-	3	-	ns	21
Output data hold time from /RAS	tOHR	3	-	3	-	ns	21
Read command hold time from /RAS	tRCHR	50	-	60	-	ns	
Output data hold time from /OE	tOHO	3	-	3	-	ns	
/CAS to output in low-Z	tCLZ	2	-	2	-	ns	

Write Cycles

Parameter	Symbol	-50		-60		Unit	Note
		Min	Max	Min	Max		
Write command set-up time	tWCS	0	-	0	-	ns	14
Write command hold time	tWCH	8	-	10	-	ns	21
Write command pulse width	tWP	8	-	10	-	ns	
Write command to /RAS lead time	tRWL	18	-	20	-	ns	
Write command to /CAS lead time	tCWL	8	-	10	-	ns	
Data-in set-up time	tDS	0	-	0	-	ns	15
Data-in hold time	tDH	13	-	15	-	ns	15

Read-Modify-Write Cycles

Parameter	Symbol	-50		-60		Unit	Note
		Min	Max	Min	Max		
Read-modify-write cycle time	tRWC	116	-	140	-	ns	
/RAS to /WE delay time	tRWD	72	-	84	-	ns	14
/CAS to /WE delay time	tCWD	30	-	34	-	ns	14
Column address to /WE delay time	tAWD	42	-	49	-	ns	14
/OE hold time from /WE	tOEH	13	-	15	-	ns	

Refresh cycles

Parameter	Symbol	-50		-60		Unit	Note
		Min	Max	Min	Max		
/CAS set-up time (/CAS-before-/RAS Refresh Cycle)	tCSR	5	-	5	-	ns	
/CAS hold time (/CAS-before-/RAS Refresh Cycle)	tCHR	8	-	10	-	ns	
/WE set-up time (/CAS-before-/RAS Refresh Cycle)	tWRP	5	-	5	-	ns	
/WE hold time (/CAS-before-/RAS Refresh Cycle)	tWRH	8	-	10	-	ns	
/RAS precharge to /CAS hold time (/CAS-before-/RAS Refresh Cycle)	tRPC	5	-	5	-	ns	

Extended Data Out Mode Cycles

Parameter	Symbol	-50		-60		Unit	Note
		Min	Max	Min	Max		
EDO page mode cyle time	tHPC	20	-	25	-	ns	20
Write pulse width during /CAS precharge	tWPE	8	-	10	-	ns	
EDO mode /RAS pulse width	tRASP	-	100K	-	100K	ns	16
Access time from /CAS precharge	tACP	-	28	-	35	ns	9,17
/RAS hold time from /CAS precharge	tRHCP	33	-	40	-	ns	
/CAS hold time referred /OE	tCOL	8	-	10	-	ns	
/CAS to /OE set-up time	tCOP	5	-	5	-	ns	
Read command hold time from /CAS precharge	tRCHP	28	-	35	-	ns	
Output data hold time from /CAS low	tDOH	5	-	5	-	ns	9,22
/OE precharge time	tOEP	8	-	10	-	ns	

EDO Page Mode Read-Modify-Write Cycle

Parameter	Symbol	-50		-60		Unit	Note
		Min	Max	Min	Max		
EDO read-modify-write cycle time	tHPRWC	57	-	68	-	ns	
EDO page mode read-modify-write cycle /CAS precharge to /WE delay time	tCPW	45	-	54	-	ns	14

Present Detect Read Cycle

Parameter	Symbol	-50		-60		Unit	Note
		Min	Max	Min	Max		
/PDE to valid PD bit	tPD	-	10	-	10	ns	
/PDE to PD bit in active	tPDOFF	2	7	2	7	ns	

Notes :

1. AC measurements assume t_T = 2ns

2. AC initial pause of 200us is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing /RAS-only refresh or /CAS-before-/RAS refresh)

3. Operation with the t_{RCD}(max) limit insures that t_{RAC}(max) can be met, t_{RCD}(max) is specified as a reference point only : if t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.

4. Operation with the t_{RAD}(max) limit insures that t_{RAC}(max) can be met, t_{RAD}(max) is specified as a reference point only : if t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled exclusively by t_{AA}.

5. Either t_{ODD} or t_{CDD} must be satisfied.

6. Either t_{DZO} or t_{DZC} must be satisfied.

7. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals, also transition times are measured between V_{IH}(min) and V_{IL}(max)

8. Assumes that t_{RCD}<=t_{RCD}(max) and t_{RAD}<=t_{RAD}(max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown

9. Measured with a load circuit equivalent to 1 TTL loads and 100pF.

10. Assumes that t_{RCD}>=t_{RCD}(max) and t_{RCD} + t_{CAC}(max) >= t_{RAD} + t_{AA}(max)

11. Assumes that t_{RAD}>=t_{RAD}(max) and t_{RCD} + t_{CAC}(max) <= t_{RAD} + t_{AA}(max)

12. Either t_{RCH} of t_{RRH} must be satified for a read cycles

13. t_{OFF}(max), t_{OEZ}(max), t_{OFR}(max) and t_{WEZ}(max) define the time at which the outputs achieve the open circuit condition and is not referenced to output voltage levels

14 t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPW} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only : If t_{WCS} >=t_{WCS}(min), the cycle is an early write cycle and the data out pin will remain open circuit(high impedance) throughout the entire cycle : If t_{RWD}>=t_{RWD}(min), t_{CWD}>=t_{CWD}(min), t_{AWD}>=t_{AWD}(min), the cycle is a read-modify-write and the data output will contain data read from the selected cell : if neither of the above sets of conditions is satified, the condition of the data out (at access time) is indeterminate.

15. t_{DS} and t_{DH} are refered to /CAS leading edge in early write cycles and to /WE leading edge in delayed write or read-modify-write cycles

16. t_{RASP} defineds /RAS pulse width in extended data out mode cycles

17. Access time is determined by the longest among t_{AA}, t_{CAC} and t_{ACP}

18 In delaying write or read-modify-write cycles, /OE must disable output buffer prior to applying data to the device.

19. When output buffers are enabled once, sustain the low impedence state until valid data is obtained. when output buffer is turned on and off within a very short time, generally it causes large Vcc/Vss line noise, which causes to degrade V_{IH} min / V_{IL} max level

20. t_{HPC}(min) can be achieved during a series of EDO mode early write cycles or EDO mode read cycels If both write and read operation are mixed in a EDO mode, /RAS cycle[EDO mode mix cycle (1)(2)] minimum value of /CAS cycle t_{HPC}[t_{CAS} + t_{CP} + 2t_T] become greater than the specified t_{HPC}(min) value. The value of CAS cycle time of mixed EDO page mode is shown in EDO page mode mix cycle (1) and (2)

21. Data output turns off and becomes high impedance from later rising edge of /RAS and /CAS. Hold time and turn off time are specified by the timing specifications of later rising edge of /RAS and /CAS between t_{OHR} and t_{OH} and between t_{OFR} and t_{OFF}

22. t_{DOH} defines the time at which the output level go cross, V_{OL}=0.8V, V_{OH}=2.0V of output timing reference level.

23. Before and after self refresh mode, execute CBR refresh to all refresh addresses in or within 64ms period on the condition a) and b) below
    a) Enter self refresh mode within 15.6us after either burst refresh or distributed refresh at equal interval to all refresh addresses are completed.
    b) Start burst refresh or distributed refresh at equal interval to all refresh addresses within 15.6us after exiting from self refresh mode

24. In case of entering from /RAS-only-refresh, It is necessary to execute CBR refresh before and after self refresh mode according as note 23

25. For L-version, It is available to apply each 128ms and 31.2us instead of 64ms and 15.6us at note 23

26. At t_{RASS} > 100us, self refresh mode is activated, and not active at t_{RASS} < 10us, It is undefined within the range of 10us < t_{RASS} < 100us. For t_{RASS} > 10us, It is necessary to satify t_{RPS}

27. XXX : H or L [H : V_{IH}(min) <= V_{IN} <=V_{IH}(max), L : V_{IH}(min) <=V_{IN} <=V_{IH}(max)]
    ///// : Invalid Dout
    When the address, clock and input pins are not described on timing waveforms, their pins must be applied V_{IH} or V_{IL}

Timing Waveforms

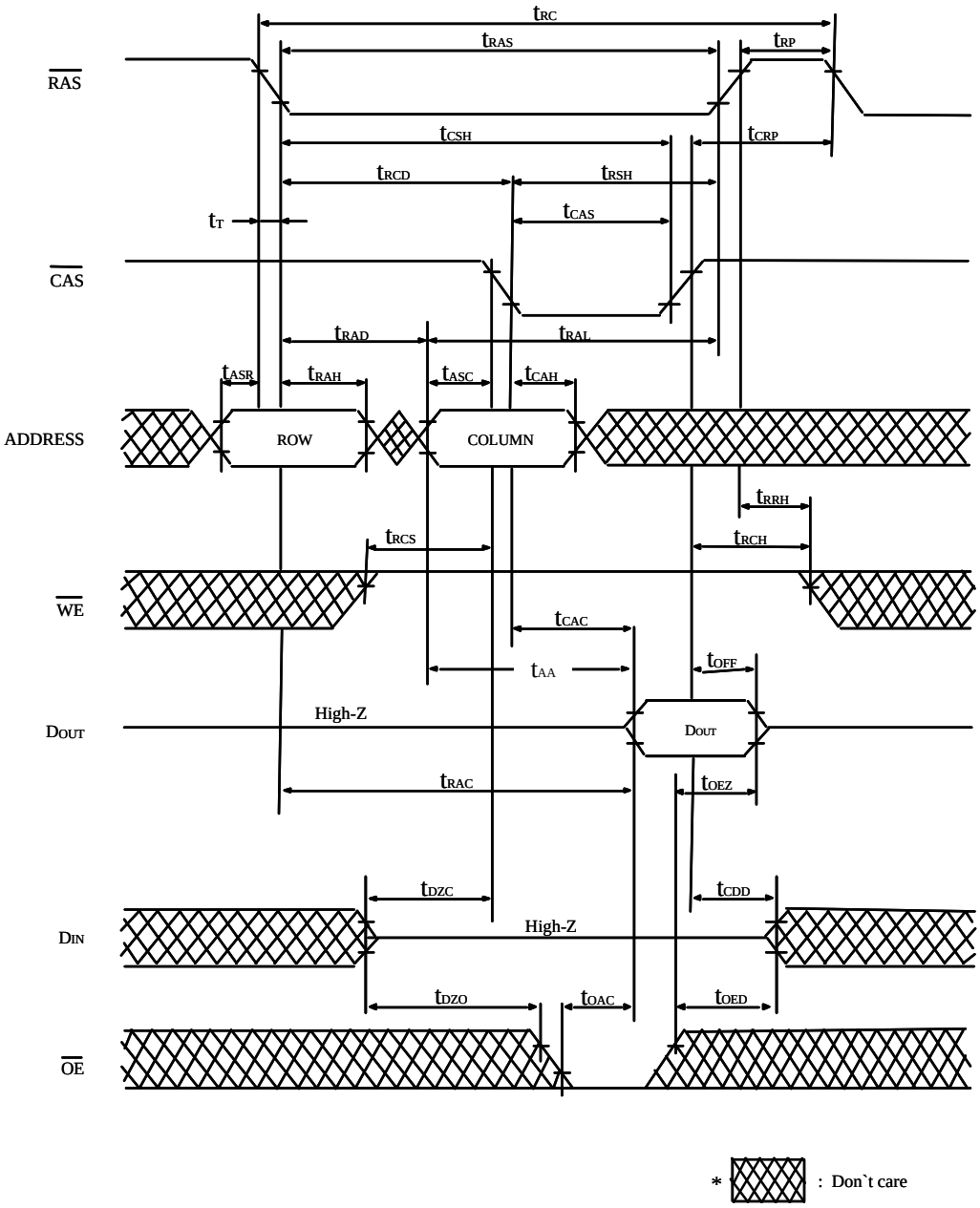


Figure 1. Read Cycle

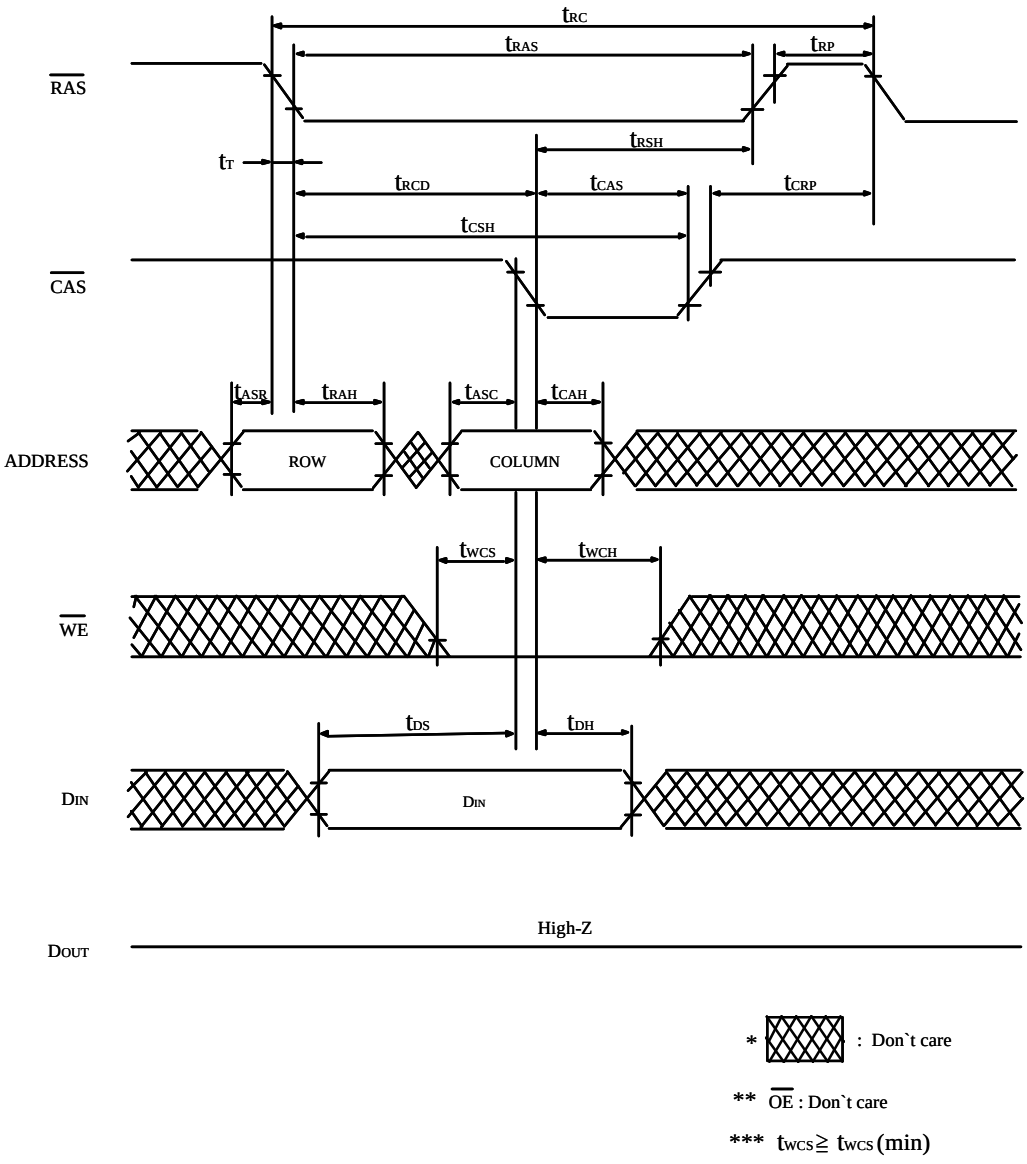


Figure 2. Early Write Cycle

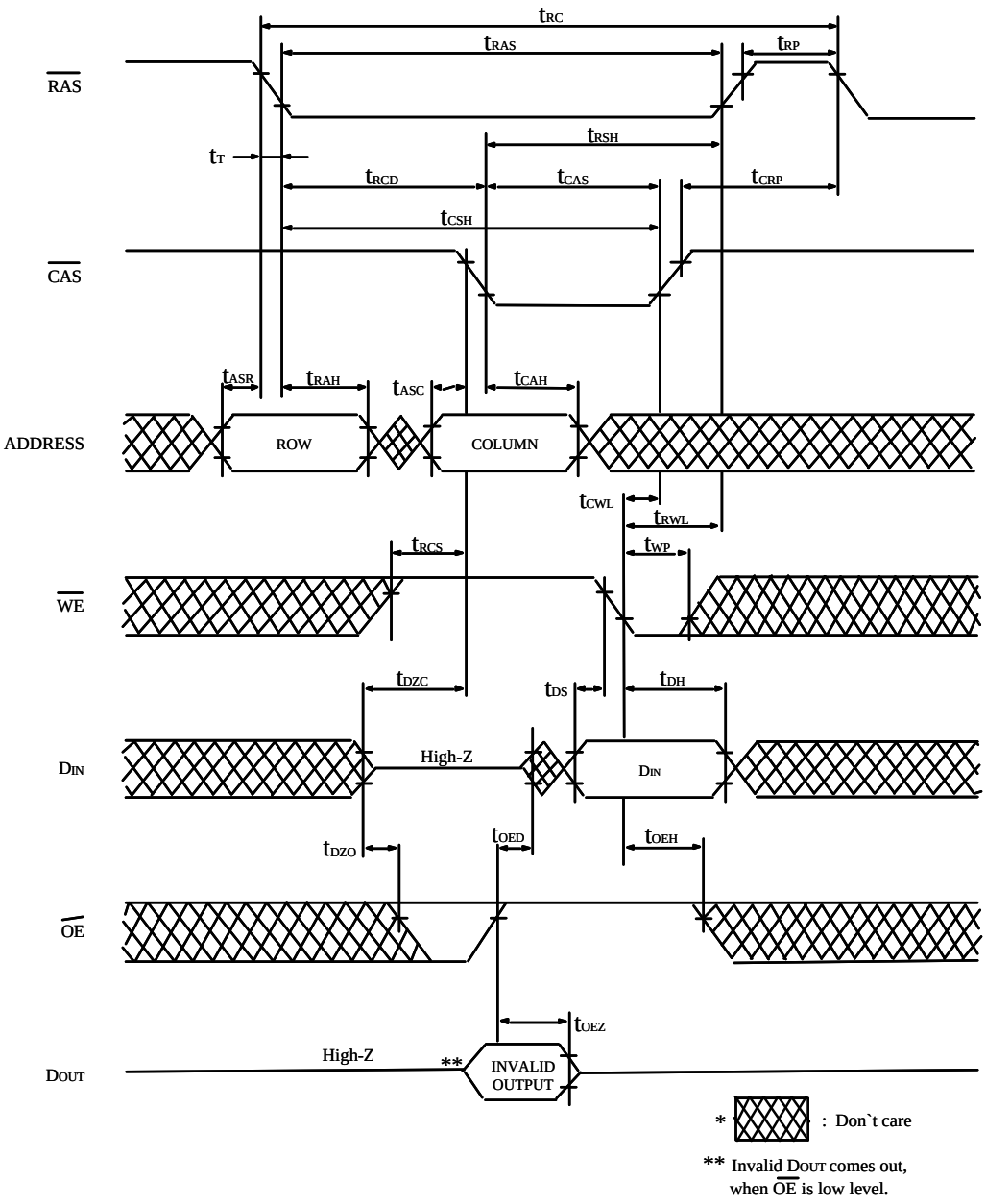


Figure 3 . Delayed Write Cycle

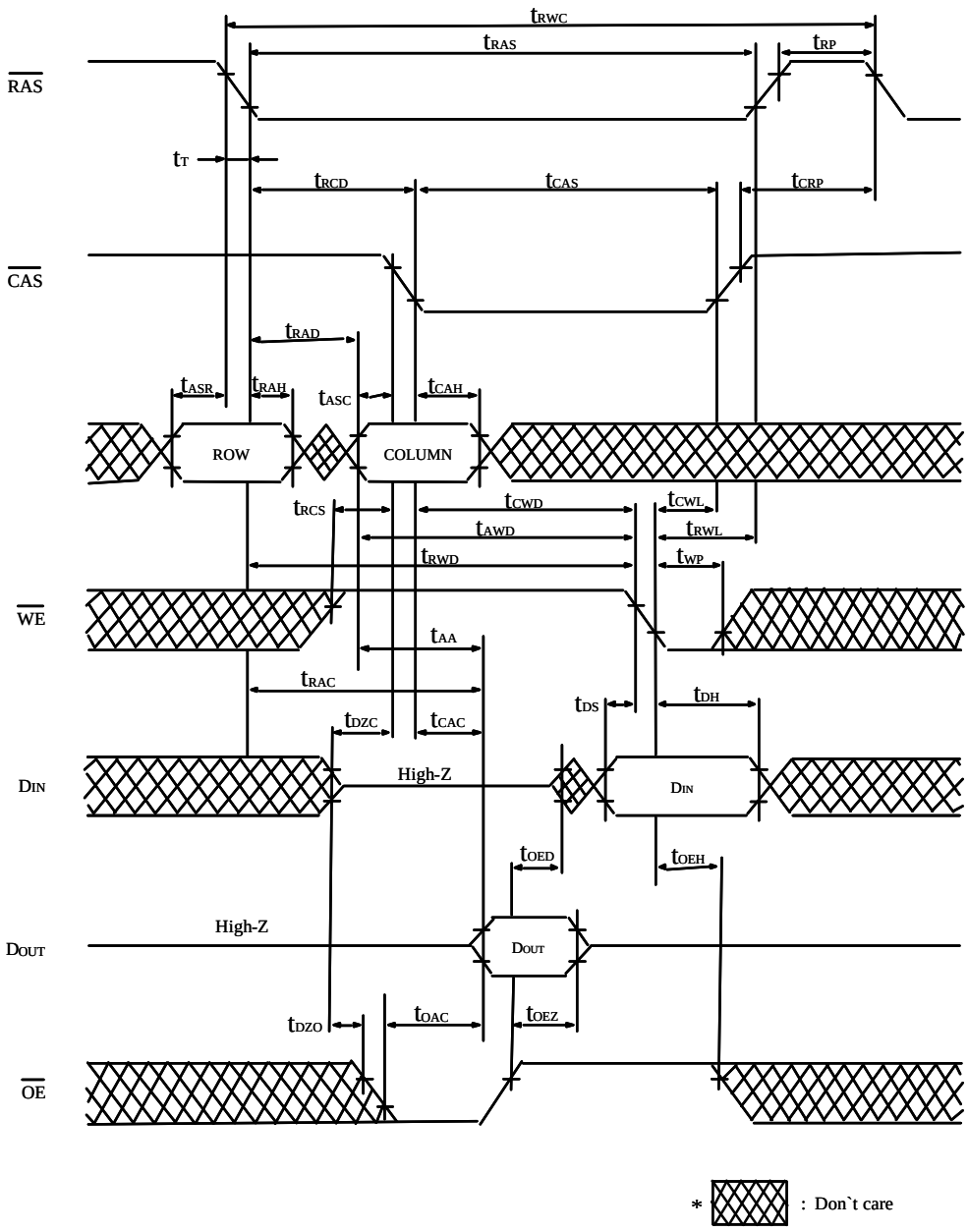


Figure 4. Read Modify Write Cycle

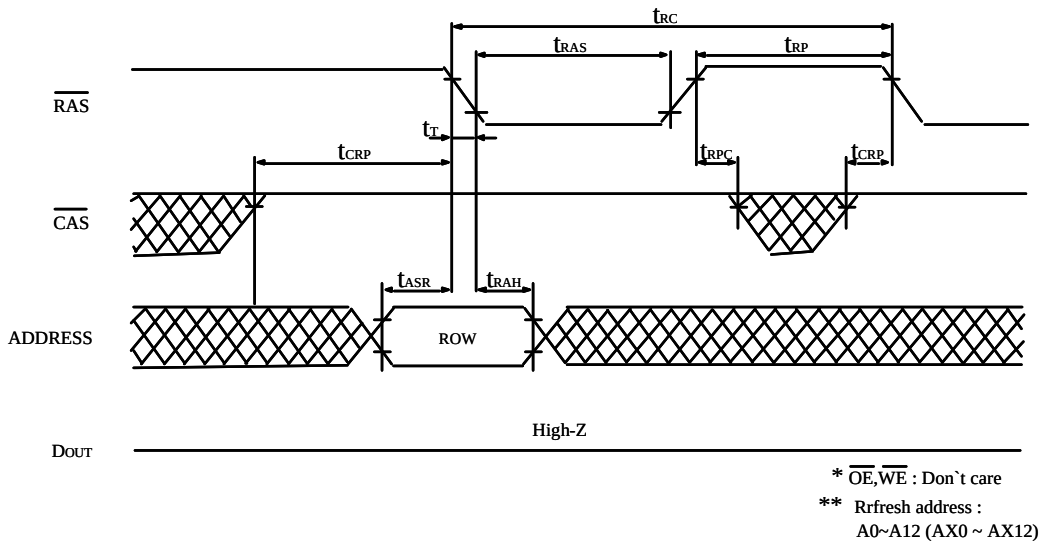


Figure 5. /RAS only Refresh Cycle

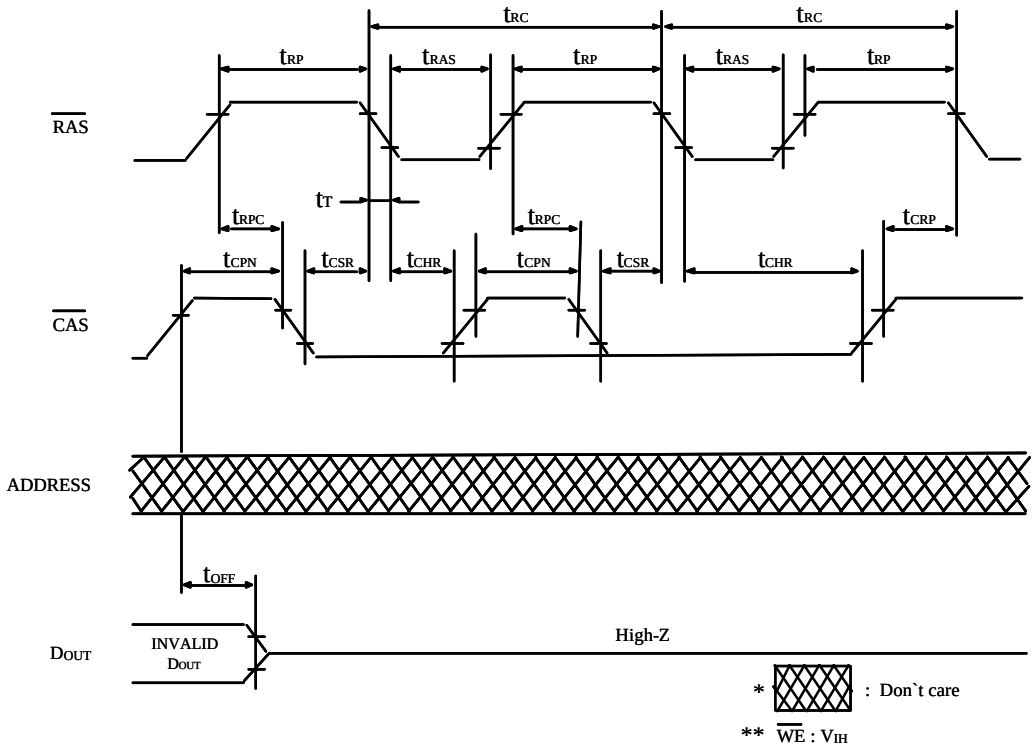


Figure 6. /CAS before /RAS Refresh Cycle

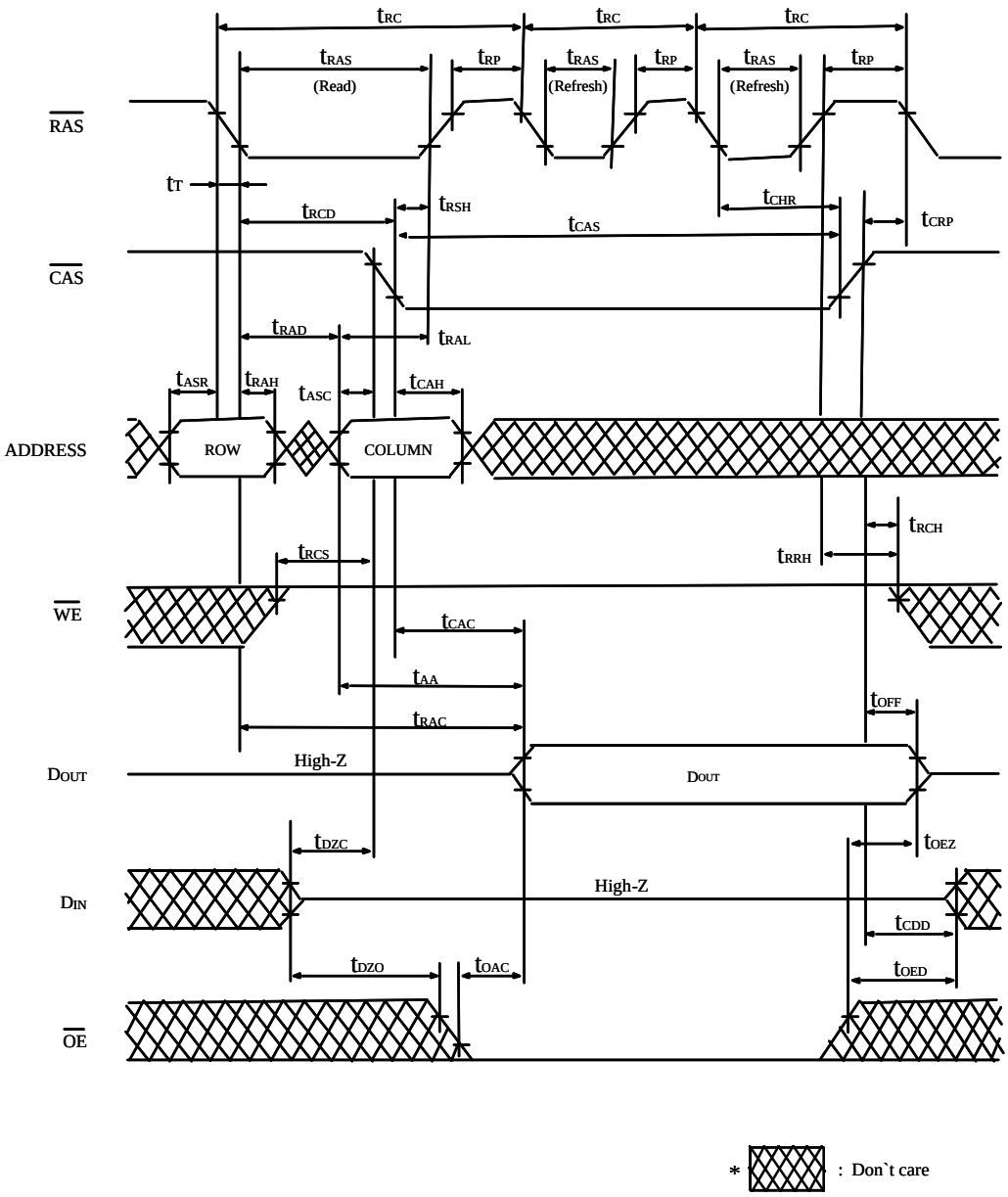


Figure 7. Hidden Refresh Cycle

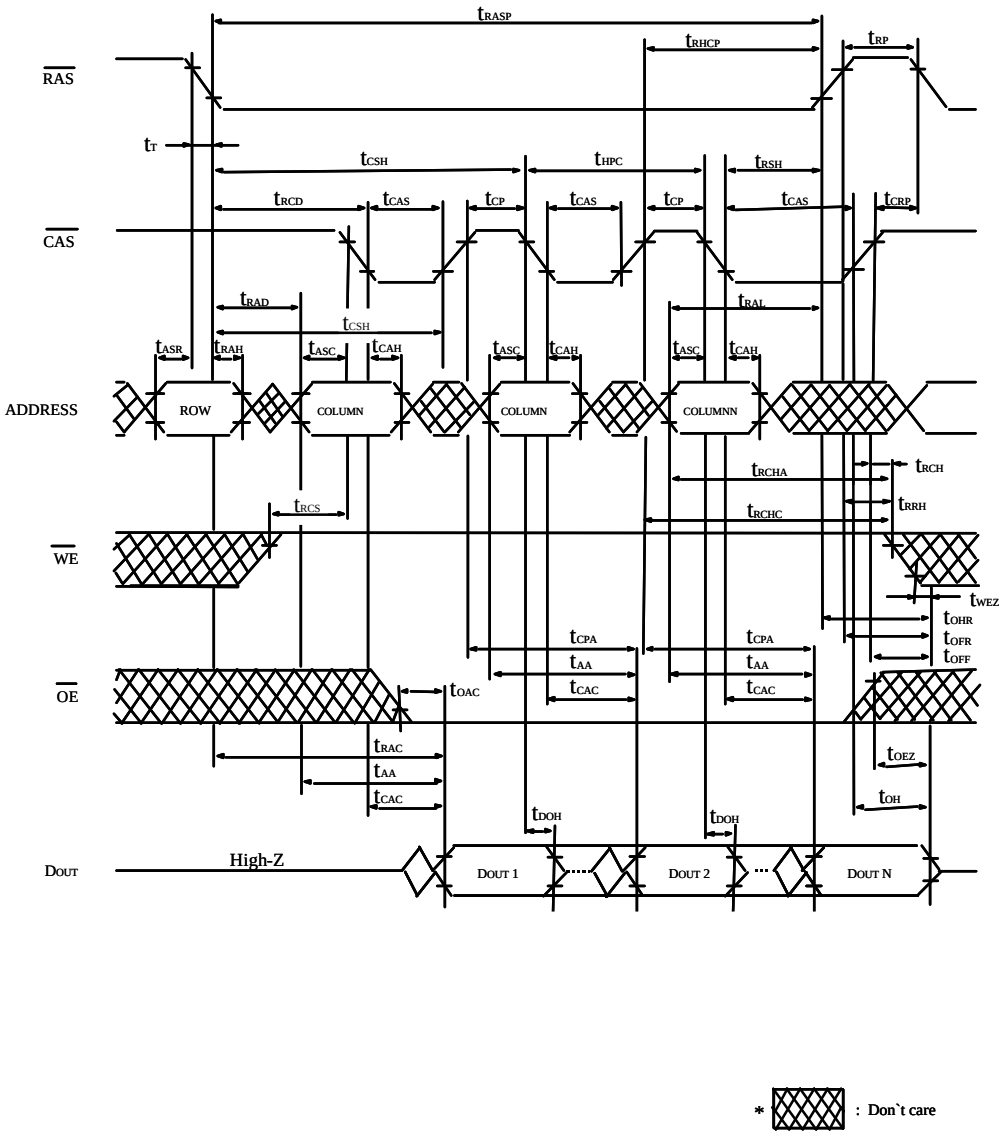


Figure 8. Extended Data Out Mode Read Cycle

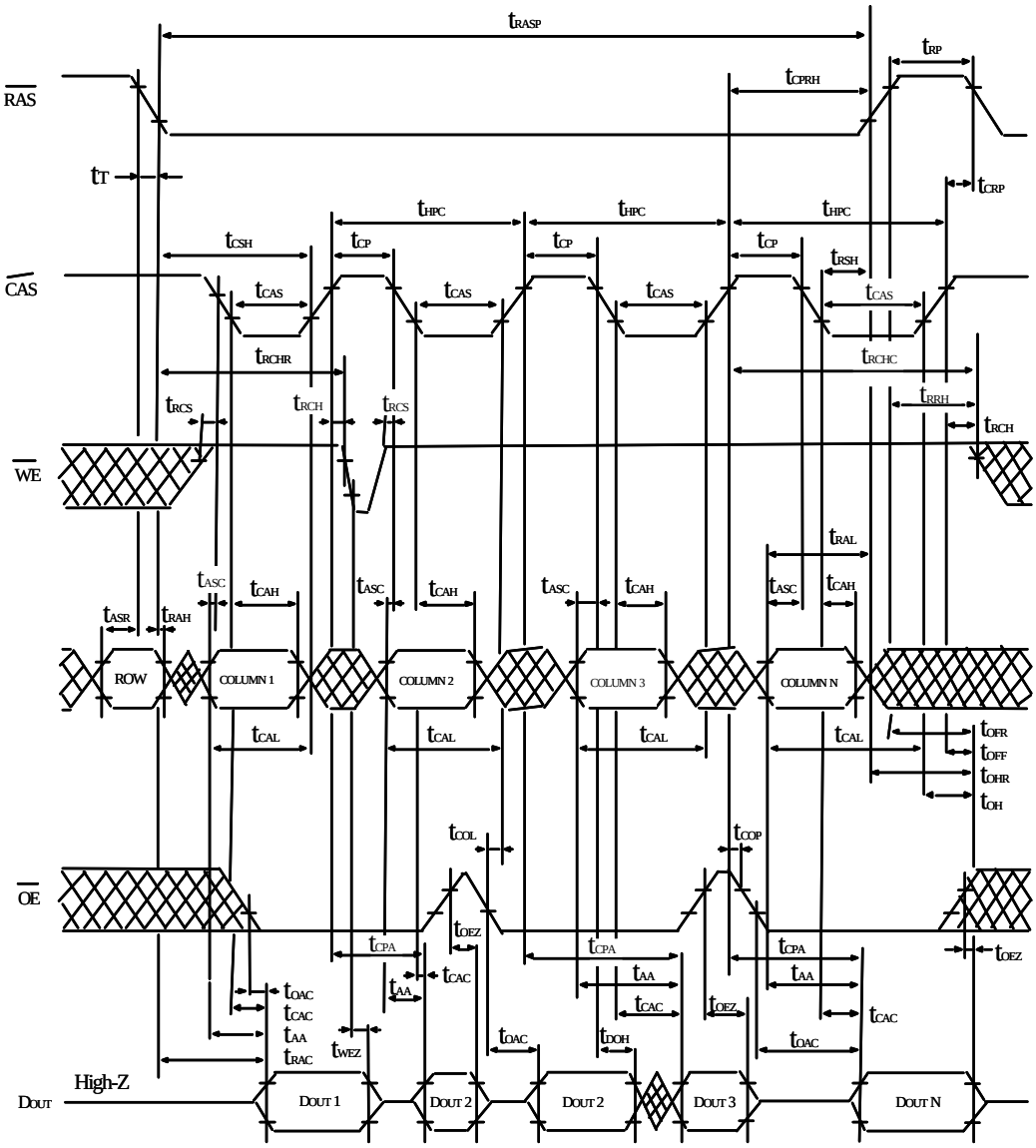


Figure 9. Extended Data Out Mode Read Cycle(/OE Control)*

* **Note** : EDO Hi-Z control by /OE or /WE. /OE rising edge disables data outputs.
When /OE goes high during /CAS high, the data will not come out until next /CAS access.
When /WE goes low during /CAS high, the data will not come out until next /CAS access.

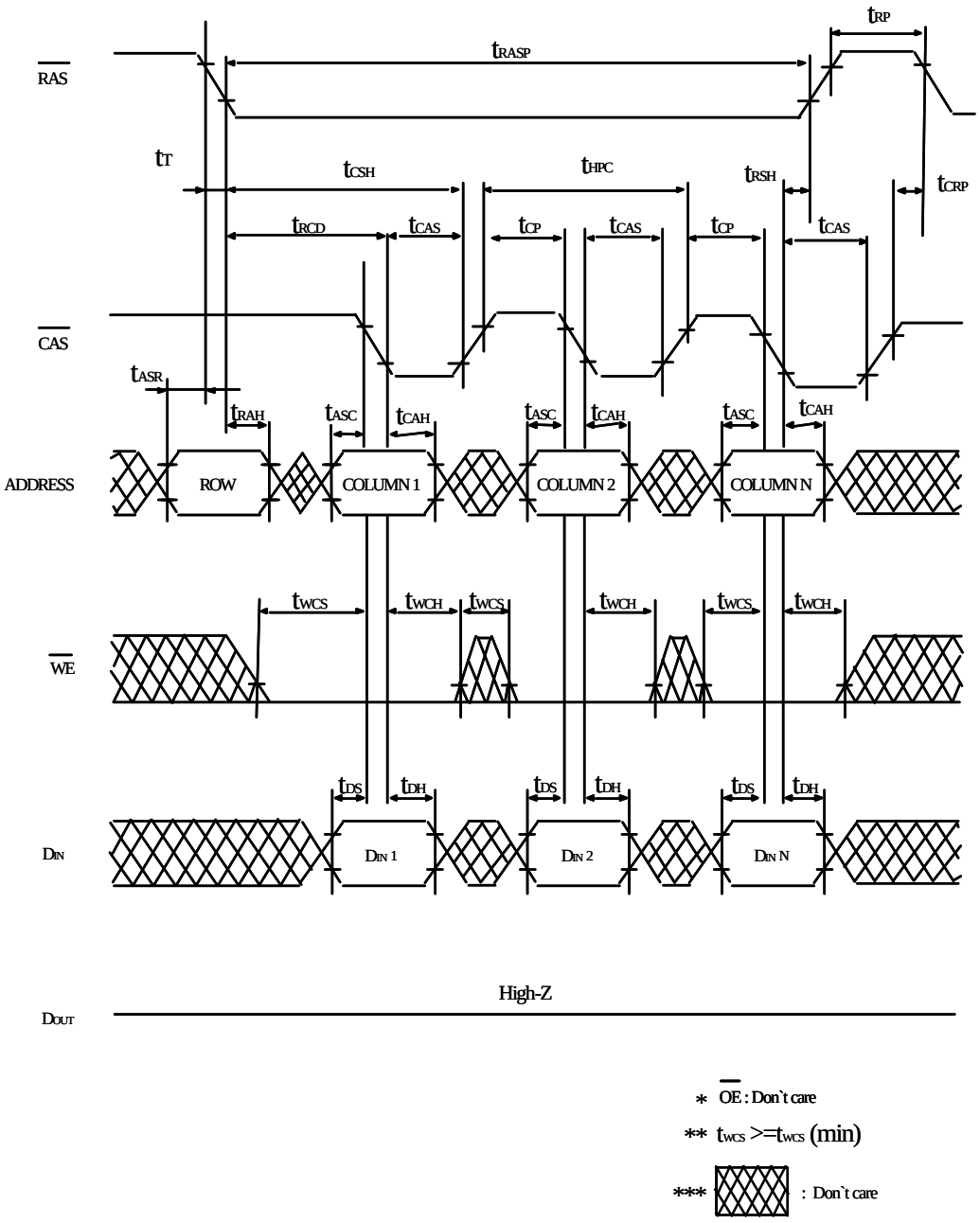


Figure 10. Extended Data Out Mode Early Write Cycle

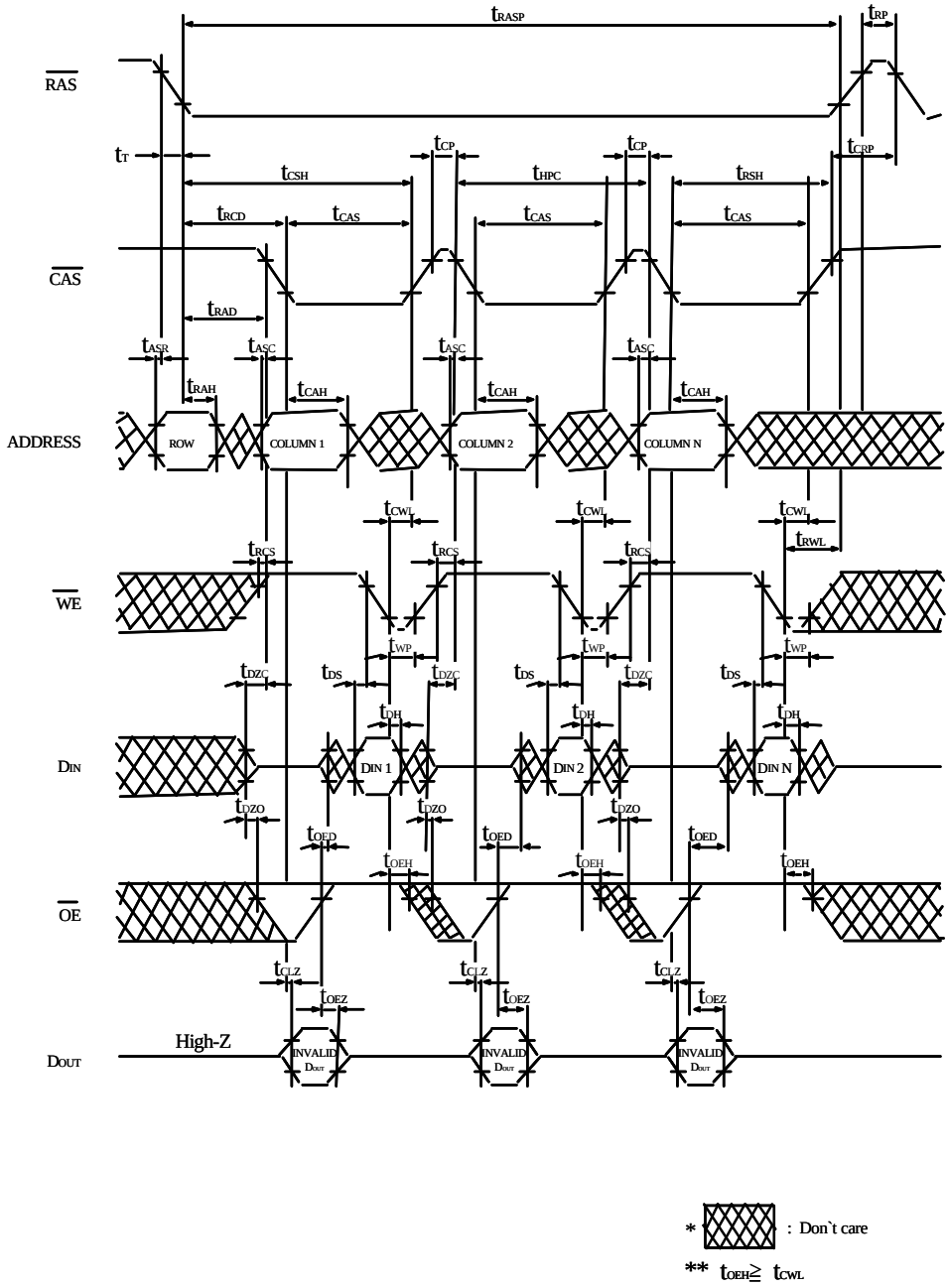


Figure 11. Extended Data Out Mode Delayed Write Cycle

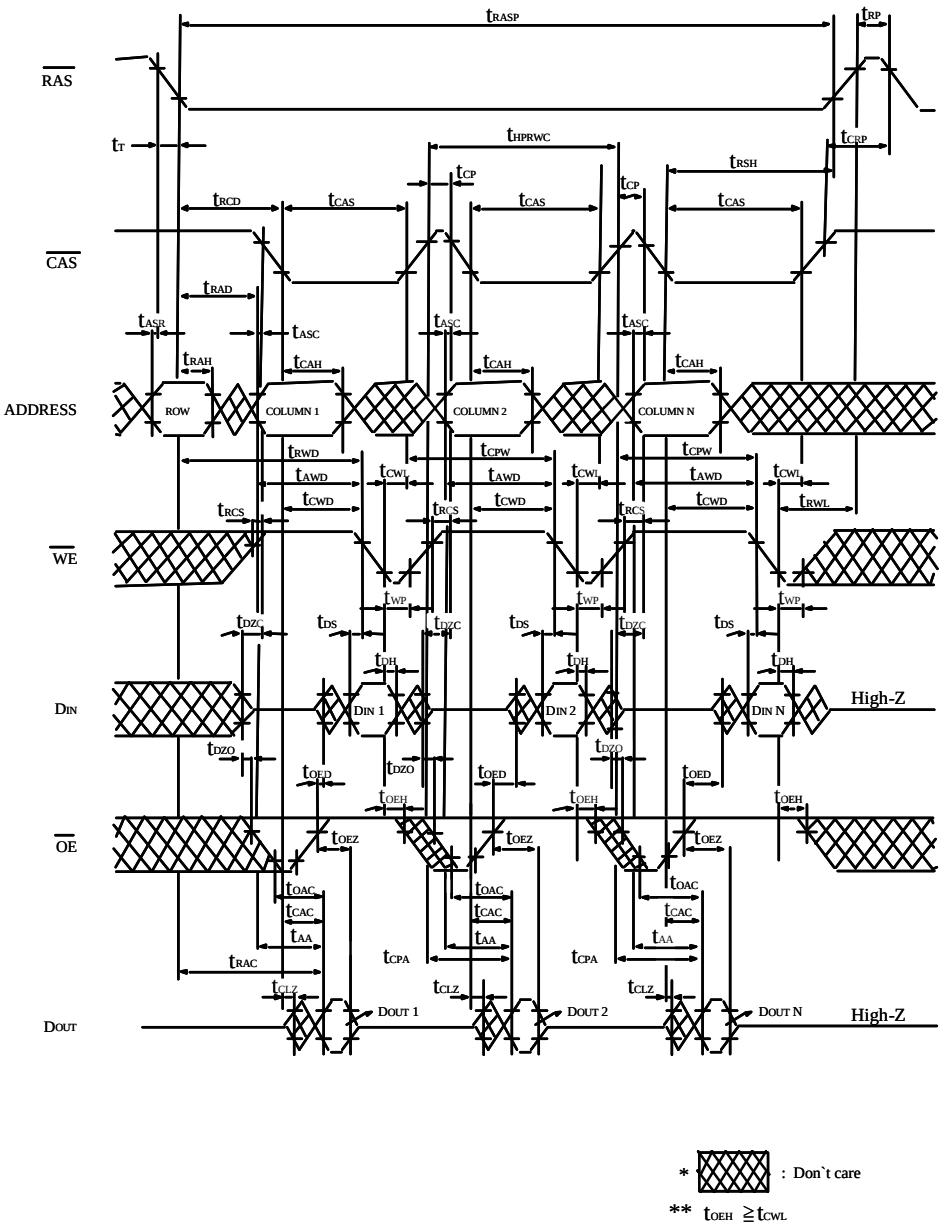


Figure 12. Extended Data Out Mode Read Modify Write Cycle

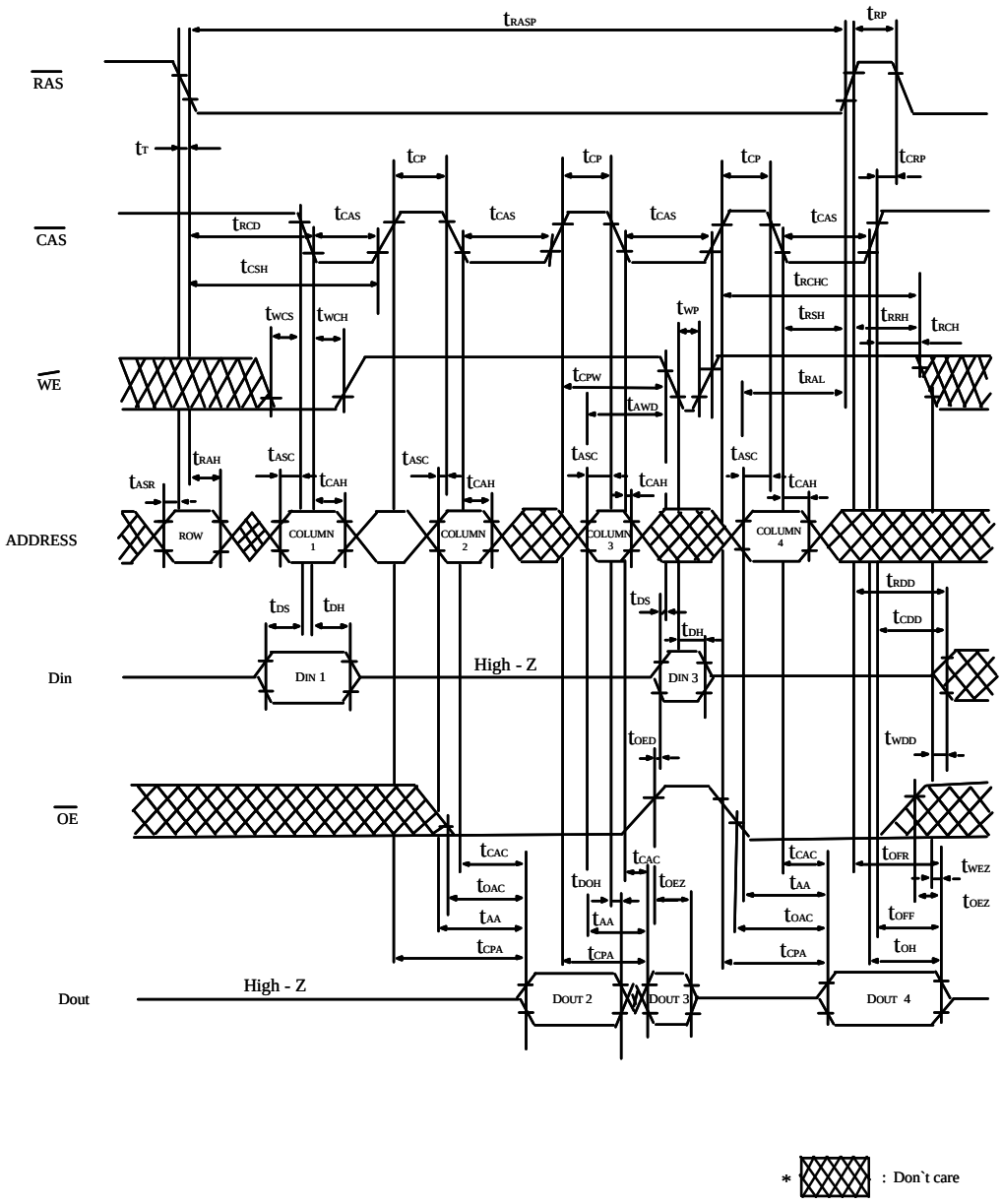


Figure 13. Extended Data Out Mode Mix Cycle (1)

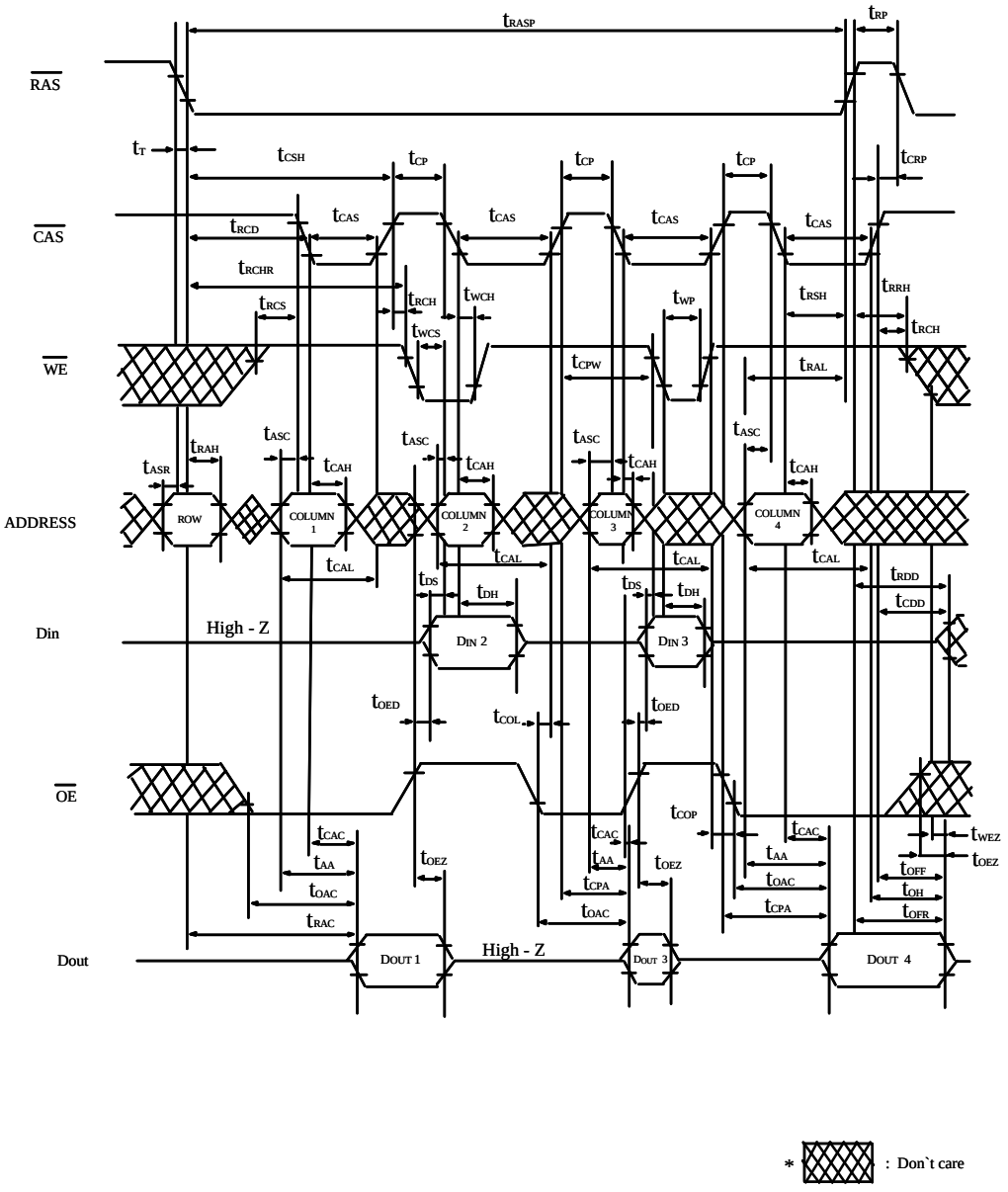


Figure 14. Extended Data Out Mode Mix Cycle(2)

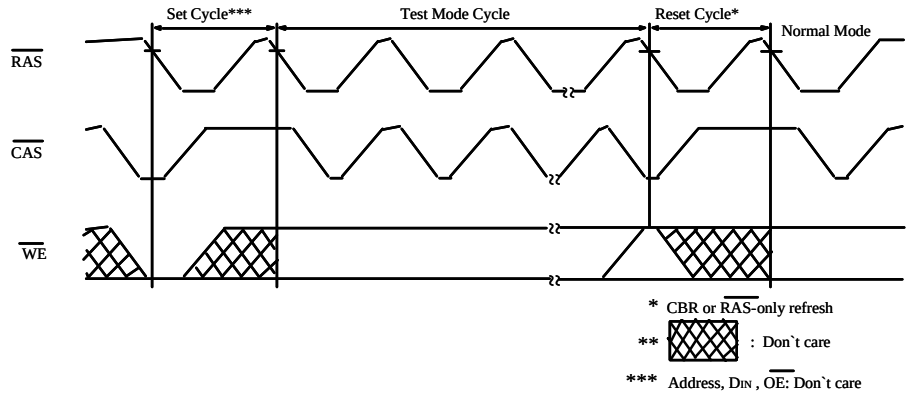


Figure 15. Test Mode Cycle

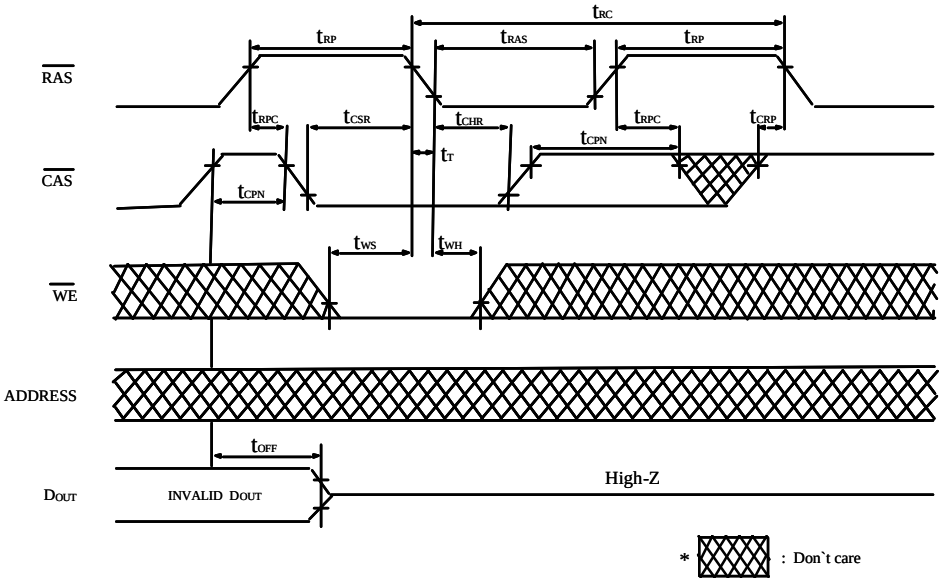


Figure 16. Test Mode Set Cycle

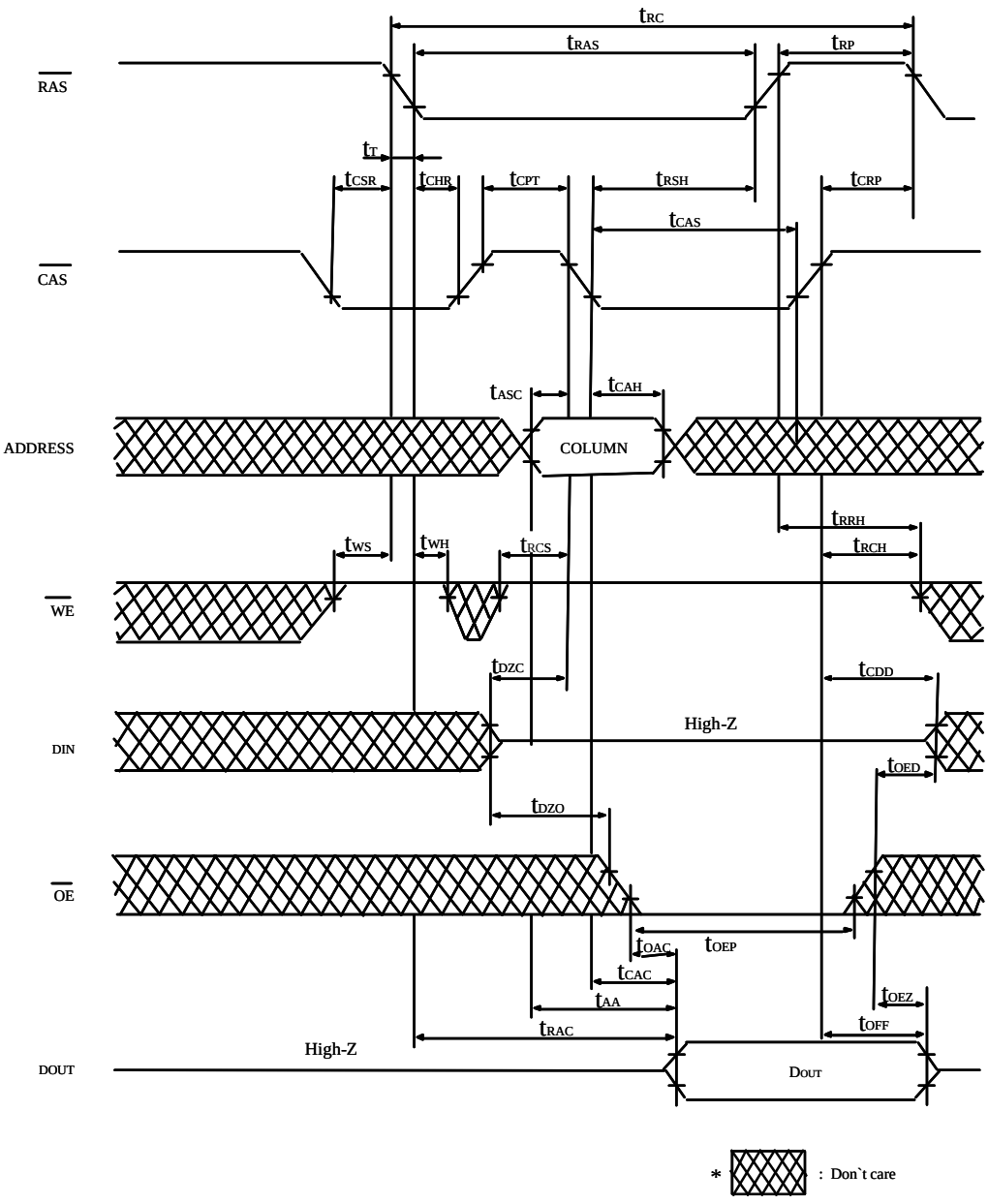


Figure 17. /CAS Before /RAS Refresh Counter Check Cycle (Read)

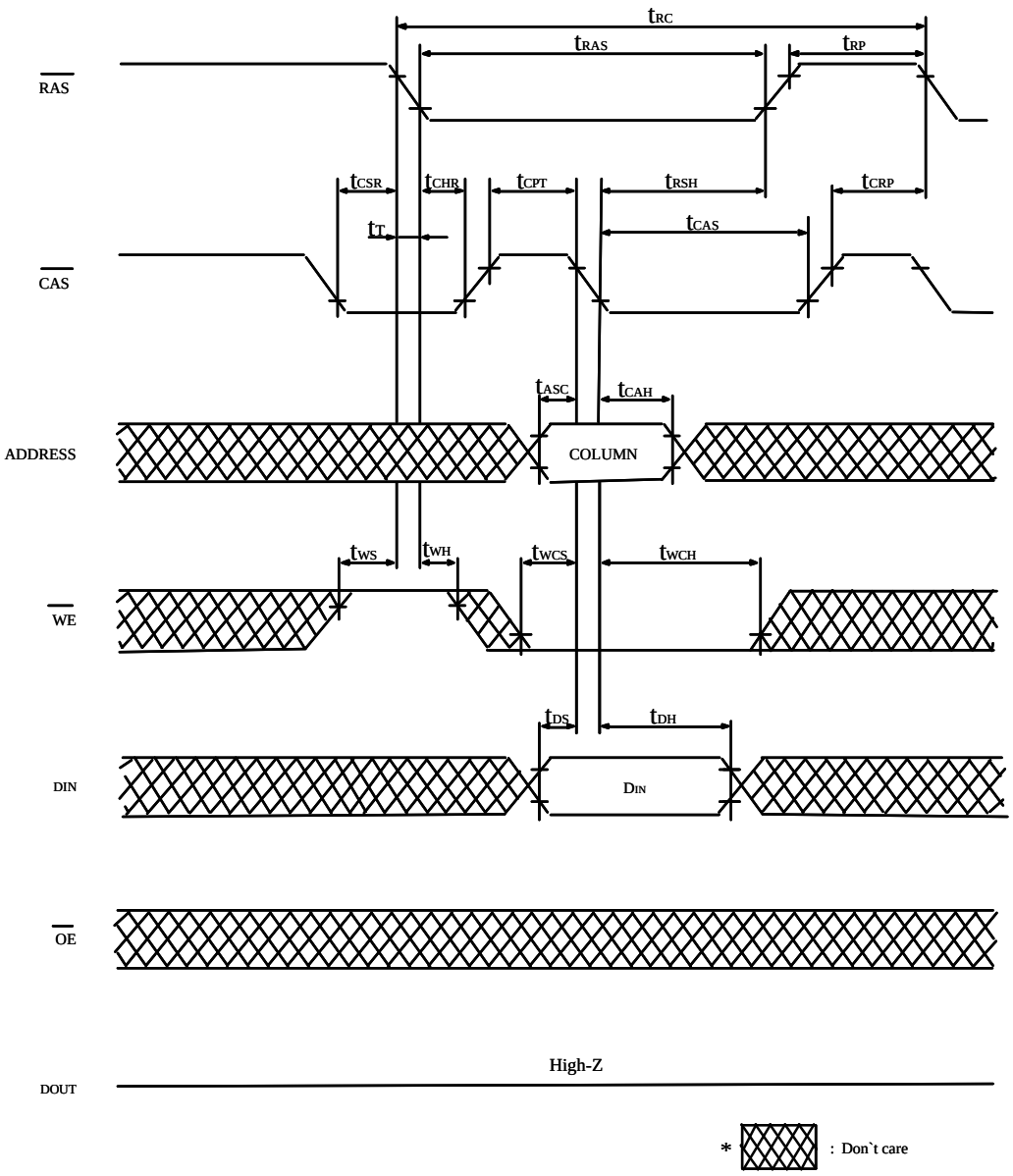
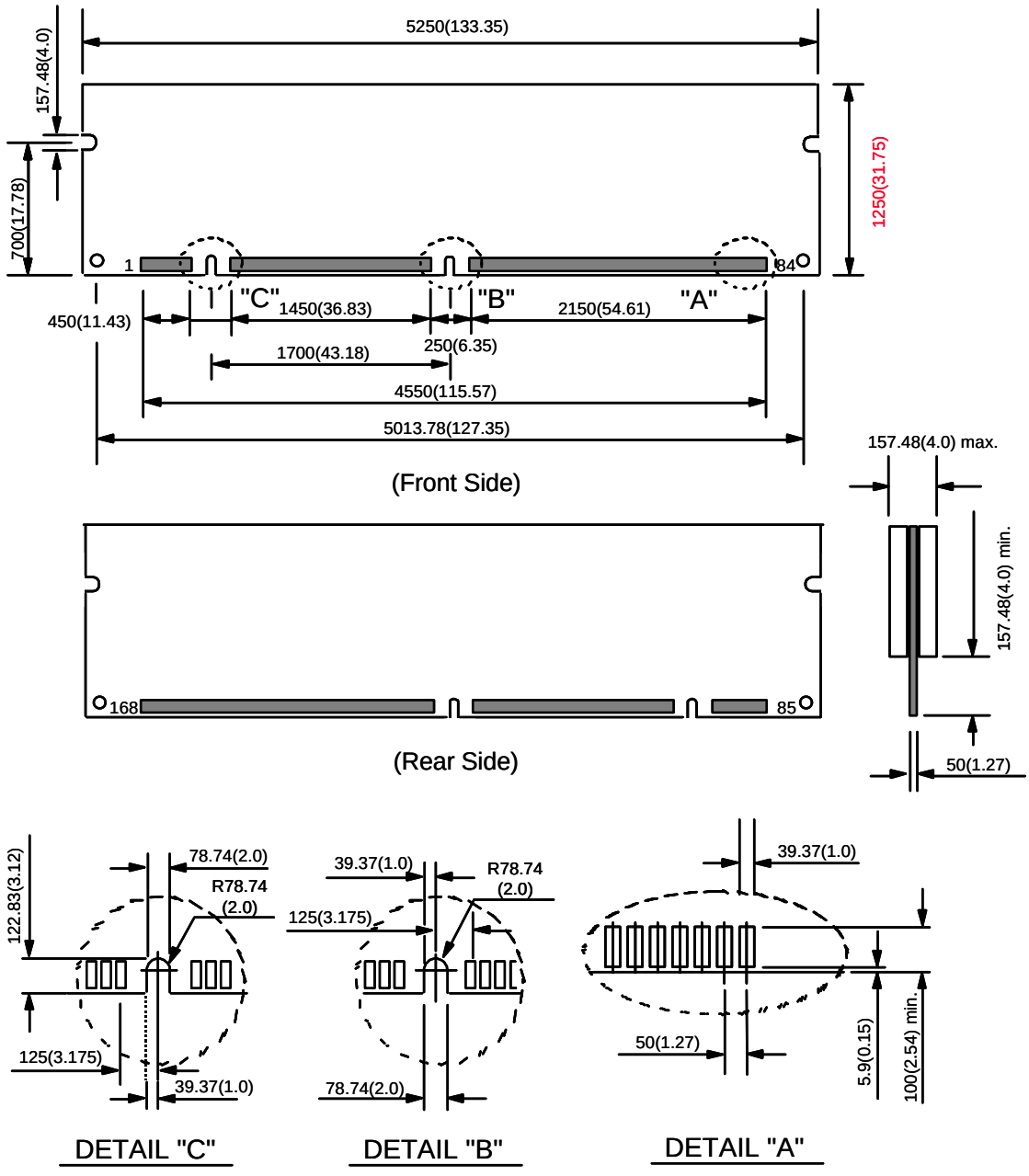


Figure 18. /CAS Before /RAS Refresh Counter Check Cycle (Write)

Package Dimension

Unit : mil (mm)
(1mm = 1/1000inches)



Note :
1. Tolerances on all dimensions +/- 5 (0.127) unless otherwise spedified
2. Thickness includes Plating and / or Metallization