



Document Title

**32K x8 bit 2.7~3.3V / 3.0~3.6V / 2.7~3.6V Low Power Slow SRAM**

Revision History

<u>Revision No</u>	<u>History</u>	<u>Draft Date</u>	<u>Remark</u>
00	Initial Merged 3.0V/3.3V SPEC	Jan.20.2000	Final
01	Revised - Marking Information Change : SOP Type - Voh Limit Change : 2.4V => 2.2V @2.7~3.6V	Feb.21.2001	Final
02	Changed Logo - HYUNDAI -> hynix - Marking Information Change	Apr.30.2001	Final

**DESCRIPTION**

The HY62K(U,V)T08081E is a high-speed, low power and 32,786 X 8-bits CMOS Static Random Access Memory fabricated using Hynix's high performance CMOS process technology. It is suitable for use in low voltage operation and battery back-up application. This device has a data retention mode that guarantees data to remain valid at the minimum power supply voltage of 2.0 volt.

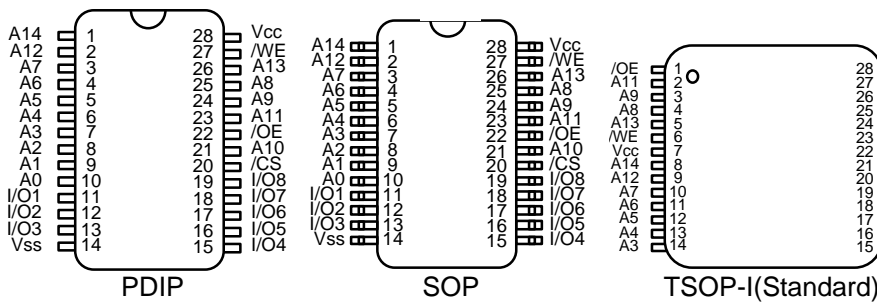
**FEATURES**

- Fully static operation and Tri-state output
- TTL compatible inputs and outputs
- Low power consumption
- Battery backup(L/LL-part)  
- 2.0V(min.) data retention
- Standard pin configuration  
- 28 pin 600mil PDIP  
- 28 pin 330mil SOP  
- 28 pin 8x13.4 mm TSOP-I (Standard)

Product No.	Voltage (V)	Speed (ns)	Operation Current(mA)	Standby Current(uA) LL-Part	Temperature (°C)
HY62KT08081E-C	2.7~3.6	70*/85/100	2	5	0~70(Normal)
HY62KT08081E-E				8	-25~85(Extended)
HY62KT08081E-I				8	-40~85(Extended)
HY62VT08081E-C	3.0~3.6	70/85/100	2	5	0~70(Normal)
HY62VT08081E-E				8	-25~85(Extended)
HY62VT08081E-I				8	-40~85(Extended)
HY62UT08081E-C	2.7~3.3	70*/85/100	2	5	0~70(Normal)
HY62UT08081E-E				8	-25~85(Extended)
HY62UT08081E-I				8	-40~85(Extended)

Note \*. Measured at 30pF test load.

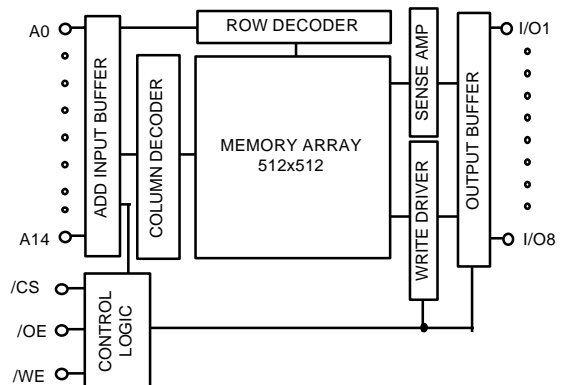
**PIN CONNECTION**



**PIN DESCRIPTION**

Pin Name	Pin Function
/CS	Chip Select
/WE	Write Enable
/OE	Output Enable
A0 ~ A14	Address Inputs
I/O1 ~ I/O8	Data Input/Output
Vcc	Power(+5.0V)
Vss	Ground

**BLOCK DIAGRAM**



**ORDERING INFORMATION**

Part No.	Vcc	Speed	Power	Temp	Package
HY62KT08081E-DPC	2.7~3.6V	70*/85/100ns	LL-part	0 to 70°C	PDIP
HY62KT08081E-DPE				-25 to 85°C	
HY62KT08081E-DPI				-40 to 85°C	
HY62KT08081E-DGC				0 to 70°C	SOP
HY62KT08081E-DGE				-25 to 85°C	
HY62KT08081E-DGI				-40 to 85°C	
HY62KT08081E-DTC				0 to 70°C	TSOP-I Standard
HY62KT08081E-DTE				-25 to 85°C	
HY62KT08081E-DTI				-40 to 85°C	
HY62VT08081E-DPC	3.0~3.6V	70/85/100ns	LL-part	0 to 70°C	PDIP
HY62VT08081E-DPE				-25 to 85°C	
HY62VT08081E-DPI				-40 to 85°C	
HY62VT08081E-DGC				0 to 70°C	SOP
HY62VT08081E-DGE				-25 to 85°C	
HY62VT08081E-DGI				-40 to 85°C	
HY62VT08081E-DTC				0 to 70°C	TSOP-I Standard
HY62VT08081E-DTE				-25 to 85°C	
HY62VT08081E-DTI				-40 to 85°C	
HY62UT08081E-DPC	2.7~3.3V	70*/85/100ns	LL-part	0 to 70°C	PDIP
HY62UT08081E-DPE				-25 to 85°C	
HY62UT08081E-DPI				-40 to 85°C	
HY62UT08081E-DGC				0 to 70°C	SOP
HY62UT08081E-DGE				-25 to 85°C	
HY62UT08081E-DGI				-40 to 85°C	
HY62UT08081E-DTC				0 to 70°C	TSOP-I Standard
HY62UT08081E-DTE				-25 to 85°C	
HY62UT08081E-DTI				-40 to 85°C	

Note \*. Measured at 30pF test load.

**ABSOLUTE MAXIMUM RATING (1)**

Symbol	Parameter	Rating	Unit
Vcc, VIN, VOUT	Power Supply, Input/Output Voltage	-0.3 to 4.6	V
TA	Operating Temperature	HY62K(U,V)T08081E-C	0 to 70
		HY62K(U,V)T08081E-E	-25 to 85
		HY62K(U,V)T08081E-I	-40 to 85
TSTG	Storage Temperature	-65 to 150	°C
Pd	Power Dissipation	1.0	W
IOUT	Data Output Current	50	mA
TSOLDER	Lead Soldering Temperature & Time	260 •10	°C•sec

Note

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is stress rating only and the functional operation of the device under these or any other conditions above those indicated in the operation of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect reliability.

**RECOMMENDED DC OPERATING CONDITIONS**

Symbol	Parameter		Min.	Typ.	Max.	Unit
Vcc	Power Supply Voltage	HY62KT08081E	2.7	3.0/3.3	3.6	V
		HY62VT08081E	3.0	3.3	3.6	V
		HY62UT08081E	2.7	3.0	3.3	V
Vss	Ground		0	0	0	V
VIH	Input High Voltage		2.2	-	Vcc+0.3	V
VIL	Input Low Voltage		-0.3(1)	-	0.4	V

Note

1. VIL = -1.5V for pulse width less than 50ns

**TRUTH TABLE**

/CS	/WE	/OE	Mode	I/O Operation
H	X	X	Standby	High-Z
L	H	H	Output Disabled	High-Z
L	H	L	Read	Data Out
L	L	X	Write	Data In

Note

1. H=VIH, L=VIL, X=Don't Care

**DC CHARACTERISTICS**

Vcc = 2.7~3.6V, TA = 0°C to 70°C (Normal)/-25°C to 85°C (Extended) /-40°C to 85°C (Industrial), unless otherwise specified.

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
ILI	Input Leakage Current	Vss ≤ VIN ≤ Vcc	-1	-	1	uA
ILO	Output Leakage Current	Vss ≤ VOUT ≤ Vcc, /CS = VIH or /OE = VIH or /WE = VIL	-1	-	1	uA
Icc	Operating Power Supply Current	/CS = VIL, VIN = VIH or VIL, I/O = 0mA	-	-	2	mA
ICC1	Average Operating Current	/CS = VIL, VIN = VIH or VIL, Min. Duty Cycle = 100%, I/O = 0mA	-	-	30	mA
ICC2	Average Operating Current	/CS = VIL, VIN = VIH or VIL, Cycle = 1us, I/O = 0mA	-	-	5	mA
ISB	TTL Standby Current (TTL Inputs)	/CS = VIH, VIN = VIH or VIL	-	-	0.3	mA
ISB1	CMOS Standby Current (CMOS Inputs)	/CS ≥ Vcc - 0.2V, 0~70 °C	-	-	5	uA
		VIN ≥ Vcc - 0.2V or -25~85 °C or	-	-	8	uA
		VIN ≤ Vss + 0.2V -40~85 °C	-	-	-	-
VOL	Output Low Voltage	IOL = 2.1mA	-	-	0.4	V
VOH	Output High Voltage	IOH = -1.0mA	2.2	-	-	V

Note : Typical values are at Vcc = 3.0/3.3V, TA = 25°C

## AC CHARACTERISTICS

V<sub>CC</sub> = 2.7~3.6V , T<sub>A</sub> = 0°C to 70°C (Normal)/-25°C to 85°C (Extended) /-40°C to 85°C (Industrial), unless otherwise specified.

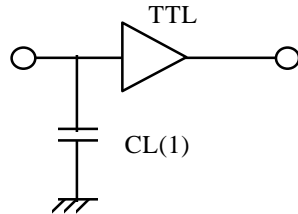
#	Symbol	Parameter	-70		-85		-10		Unit
			Min.	Max.	Min.	Max.	Min	Max.	
READ CYCLE									
1	t <sub>RC</sub>	Read Cycle Time	70	-	85	-	100	-	ns
2	t <sub>AA</sub>	Address Access Time	-	70	-	85	-	100	ns
3	t <sub>ACS</sub>	Chip Select Access Time	-	70	-	85	-	100	ns
4	t <sub>OE</sub>	Output Enable to Output Valid	-	35	-	40	-	50	ns
5	t <sub>CLZ</sub>	Chip Select to Output in Low Z	10	-	10	-	10	-	ns
6	t <sub>OLZ</sub>	Output Enable to Output in Low Z	5	-	5	-	5	-	ns
7	t <sub>CHZ</sub>	Chip Deselection to Output in High Z	0	30	0	30	0	30	ns
8	t <sub>OHZ</sub>	Out Disable to Output in High Z	0	30	0	30	0	30	ns
9	t <sub>OH</sub>	Output Hold from Address Change	10	-	10	-	15	-	ns
WRITE CYCLE									
10	t <sub>WC</sub>	Write Cycle Time	70	-	85	-	100	-	ns
11	t <sub>CW</sub>	Chip Selection to End of Write	60	-	70	-	80	-	ns
12	t <sub>AW</sub>	Address Valid to End of Write	60	-	70	-	80	-	ns
13	t <sub>AS</sub>	Address Set-up Time	0	-	0	-	0	-	ns
14	t <sub>WP</sub>	Write Pulse Width	50	-	60	-	70	-	ns
15	t <sub>WR</sub>	Write Recovery Time	0	-	0	-	0	-	ns
16	t <sub>WHZ</sub>	Write to Output in High Z	0	25	0	30	0	35	ns
17	t <sub>DW</sub>	Data to Write Time Overlap	30	-	40	-	40	-	ns
18	t <sub>DH</sub>	Data Hold from Write Time	0	-	0	-	0	-	ns
19	t <sub>OW</sub>	Output Active from End of Write	5	-	5	-	10	-	ns

**AC TEST CONDITIONS**

V<sub>CC</sub> = 2.7~3.6V, T<sub>A</sub> = 0°C to 70°C (Normal)/-25°C to 85°C (Extended) /-40°C to 85°C (Industrial), unless otherwise specified.

Parameter		Value
Input Pulse Level		0.4V to 2.2V
Input Rise and Fall Time		5ns
Input and Output Timing Reference Level		1.5V
Output Load	t <sub>CLZ</sub> ,t <sub>OLZ</sub> ,t <sub>CHZ</sub> ,t <sub>OHZ</sub> ,t <sub>WHZ</sub> ,t <sub>OW</sub>	CL = 5pF + 1TTL Load
	Others	CL = 100pF + 1TTL Load
		CL* = 30pF + 1TTL Load

**AC TEST LOADS**



Note : Including jig and scope capacitance

**CAPACITANCE**

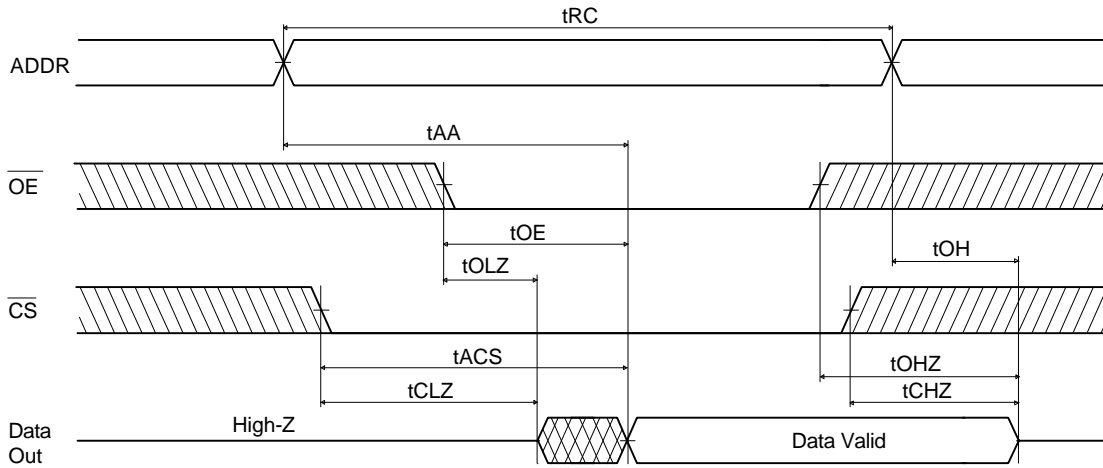
T<sub>A</sub> = 25°C, f = 1.0MHz

Symbol	Parameter	Condition	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	6	pF
C <sub>I/O</sub>	Input /Output Capacitance	V <sub>I/O</sub> = 0V	8	pF

Note : These parameters are sampled and not 100% tested

**TIMING DIAGRAM**

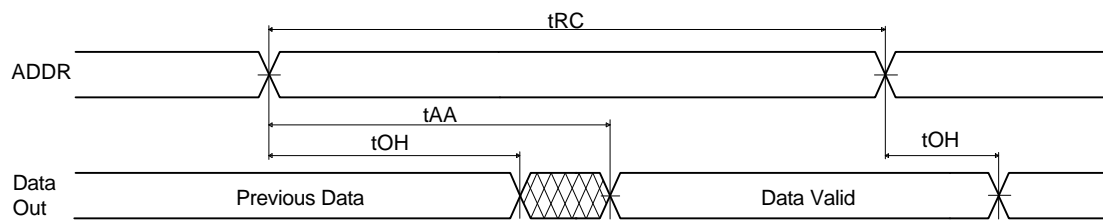
**READ CYCLE 1**



**Note(READ CYCLE):**

1.  $t_{CHZ}$  and  $t_{OHZ}$  are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition,  $t_{CHZ}$  max. is less than  $t_{CLZ}$  min. both for a given device and from device to device.
3.  $\overline{WE}$  is high for the read cycle.

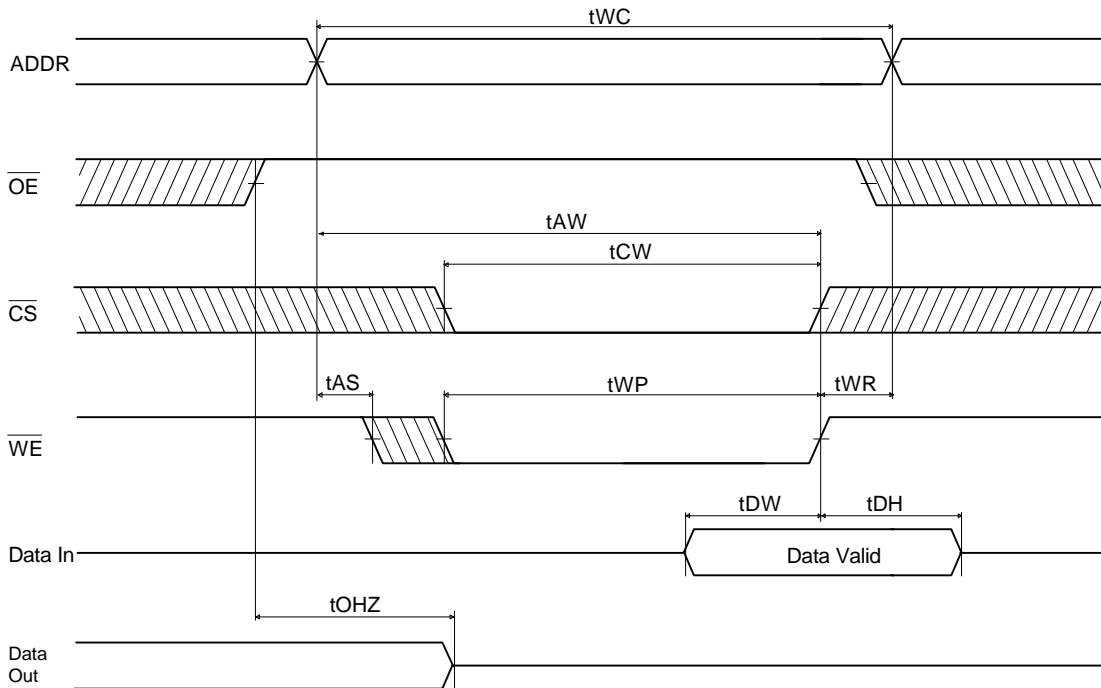
**READ CYCLE 2**



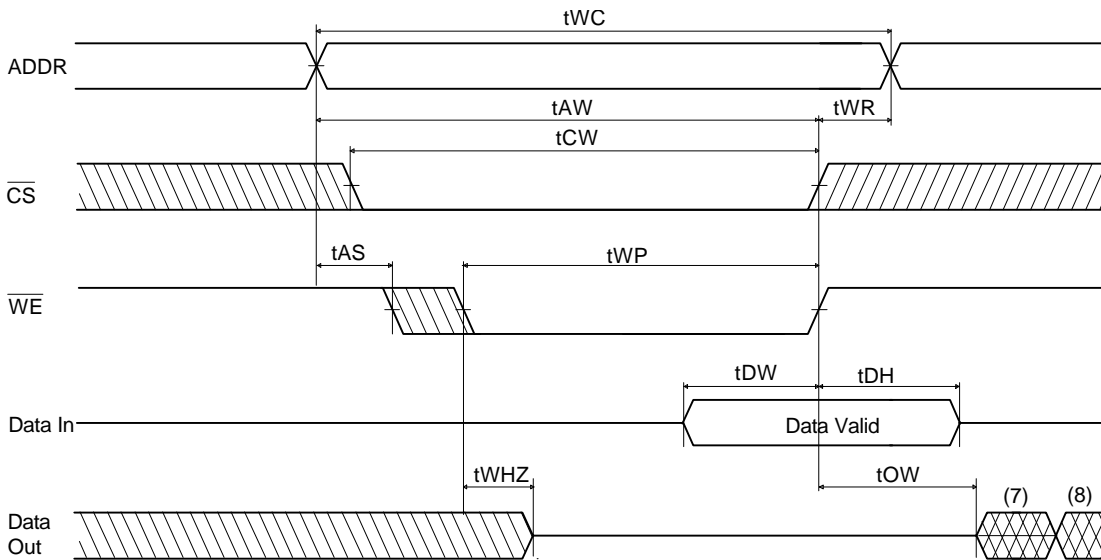
**Note(READ CYCLE):**

1.  $\overline{WE}$  is high for the read cycle.
2. Device is continuously selected  $\overline{CS} = V_{IL}$ .
3.  $\overline{OE} = V_{IL}$ .

**WRITE CYCLE 1 (/OE Clocked)**



**WRITE CYCLE 2 (/OE Low Fixed)**





Notes(WRITE CYCLE):

1. A write occurs during the overlap of a low /CS and a low /WE. A write begins at the latest transition among /CS going low and /WE going low: A write ends at the earliest transition among /CS going high and /WE going high. tWP is measured from the beginning of write to the end of write.
2. tcw is measured from the later of /CS going low to the end of write .
3. tAS is measured from the address valid to the beginning of write.
4. tWR is measured from the end of write to the address change. tWR is applied in case a write ends as /CS, or /WE going high.
5. If /OE and /WE are in the read mode during this period, and the I/O pins are in the output low-Z state, input of opposite phase of the output must not be applied because bus contention can occur.
6. If /CS goes low simultaneously with /WE going low, or after /WE going low, the outputs remain in high impedance state.
7. DOUT is the same phase of the latest written data in this write cycle.
8. DOUT is the read data of the new address.

**DATA RETENTION CHARACTERISTIC**

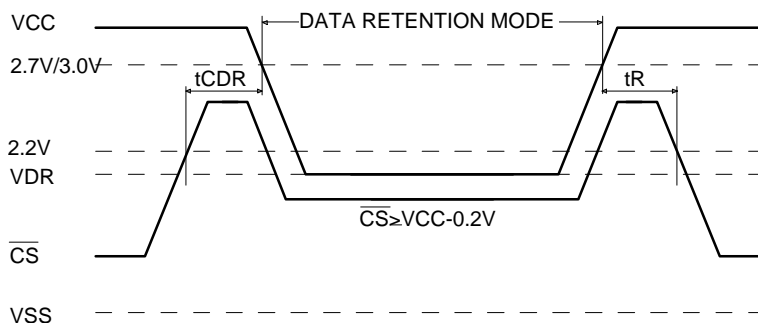
Vcc = 2.7~3.6V, TA = 0°C to 70°C (Normal)/-25°C to 85°C (Extended) /-40°C to 85°C (Industrial), unless otherwise specified.

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit	
VDR	Vcc for Data Retention	CS ≥ Vcc-0.2V, VIN ≥ Vcc-0.2V or VIN ≤ Vss+0.2V	2.0	-	3.6	V	
ICDDR	Data Retention Current	Vcc=3.0V, /CS ≥ Vcc - 0.2V, VIN ≥ Vcc - 0.2V or VIN ≤ Vss + 0.2V	0~70°C	-	0.5	5	uA
			-25~85°C or -40~85°C	-	0.5	8	uA
tCDR	Chip Deselect to Data Retention Time	See Data Retention	0	-	-	ns	
tR	Operating Recovery Time	Timing Diagram	tRC(2)	-	-	ns	

Notes

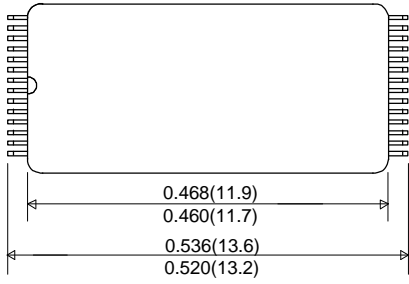
1. Typical values are under the condition of TA = 25°C.
2. tRC is read cycle time.

**DATA RETENTION TIMING DIAGRAM**





28pin 8x13.4mm Thin Small Outline Package Standard(T)



UNIT : INCH(mm) <sup>MAX.</sup>  
<sub>MIN.</sub>

