HY51V(S)65163HG/HGL

4M x 16Bit EDO DRAM

PRELIMINARY

DESCRIPTION

This familiy is a 64Mbit dynamic RAM organized 4,194,304 x 16bit configuration with Extended Data Out mode CMOS DRAMs. Extended data out mode is a kind of page mode which is useful for the read operation. The advanced circuit and process allow this device to achieve high performance and low power dissipation. Features are access time(45ns or 50ns) and refresh cycle(4K ref) and power consumption (Normal or low power with self refresh).

Advanced CMOS process as well as circuit techniques for wide operating margins allow this device to achieve high speed access and high reliability

FEATURES

- Extended data out operation
- Read-modify-write capability
- Multi-bit parallel test capability
- LVTTL(3.3V) compatible inputs and outputs
- /RAS only, CAS-before-/RAS, Hidden and self refresh(L-version) capability
- JEDEC standard pinout
  50pin plastic SOJ/TSOP-II(400mil)
- Single power supply of 3.3V +/- 10%
- Battery back up operation(L-version)

- **Fast access time and cycle time**

Part No	tRAC	tAA	tCAC	tRC	tHPC
HY51V(S)65163HG/HGL-45	45ns	23ns	12ns	74ns	17ns
HY51V(S)65163HG/HGL-5	50ns	25ns	13ns	84ns	20ns
HY51V(S)65163HG/HGL-6	60ns	30ns	15ns	104ns	25ns

- **Power dissipation**

	45ns	50ns	60ns
Active	468mW	432mW	396mW
Standby	1.8mW(CMOS level Max) 0.72mW (L-version : Max)		

- **Refresh cycle**

Part No	Ref	Normal	L-part
HY51V65163HG*	4K Ref	64ms	
HY51V65163HGL*	4K Ref		128ms

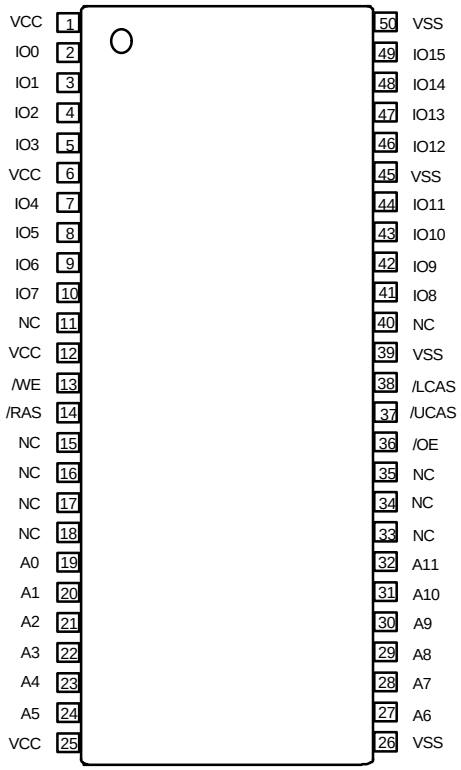
*** : /RAS only, CBR and hidden refresh**

ODERING INFORMATION

Part Number	Access Time	Package
HY51V(S)65163HG/HG(L)J-45 HY51V(S)65163HG/HG(L)J-5 HY51V(S)65163HG/HG(L)J-6	45ns 50ns 60ns	400mil 50pin SOJ
HY51V(S)65163HG/HG(L)T-45 HY51V(S)65163HG/HG(L)T-5 HY51V(S)65163HG/HG(L)T-6	45ns 50ns 60ns	400mil 50pin TSOP-II

(S) : Self refresh, (L) : Low power

PIN CONFIGURATION



50 Pin Plastic SOJ / TSOP-II

PIN DESCRIPTION

Pin	Function
/RAS	Row Address Strobe
/UCAS, /LCAS	Column Address Strobe
/WE	Write Enable
/OE	Output Enable
A0-A11	Address Inputs
A0-A11	Refresh Address Inputs
I/O 0- I/O15	Data Input / Output
Vcc	Power (3.3V)
Vss	Ground
NC	No connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Ambient Temperature	T_A	0 ~ 70	^oC
Storage Temperature	T_{STG}	-55 ~ 125	^oC
Voltage on Any Pin relative to V_{SS}	V_T	-0.5 ~ Vcc + 0.5 (Max 4.6V)	V
Voltage on V_{CC} relative to V_{SS}	V_{CC}	-0.5 ~ 4.6	V
Short Circuit Output Current	I_{OUT}	50	mA
Power Dissipation	P_T	1	W

Note : Operation at above absolute maximum rating can adversely affect device reliability.

Recommended DC OPERATING CONDITIONS (T_A=0 to 70 ^oC)

Parameter	Symbol	Min	Typ.	Max	Unit	Note
Power Supply Voltage	V_{CC}	3.0	3.3	3.6	V	1,2
Power Supply Voltage	V_{SS}	0	0	0	V	2
Input High Voltage	V_{IH}	2.0	-	V_{CC} + 0.3	V	1
Input Low Voltage	V_{IL}	-0.3	-	0.8	V	1

Note : All voltages are referenced to Vss

1. 6.0V at pulse width 10ns which is measured at Vcc
2. -0.1V at pulse width 10ns which is measured at Vss

DC CHARACTERISTICS (Vcc = 3.3V +/- 10%, TA=0 to 70°C)

Symbol	Parameter		Min	Max	Unit	Note
VOH	Output Level Output Level voltage(Iout= -2mA)		2.4	Vcc	V	
VOL	Output Level Output Level voltage(Iout=2mA)		0	0.4	V	
ICC1	Operating current (tRC = tRC min)	45ns	-	130	mA	1, 2
		50ns	-	120		
		60ns	-	110		
ICC2	Standby current (TTL interface) Power supply standby current (/RAS, /UCAS,/LCAS=VIH, Dout = High-Z)		-	1	mA	
ICC3	/RAS only refresh current (tRC= tRC min)	45ns	-	130	mA	2
		50ns	-	120		
		60ns	-	110		
ICC4	Extended data out page mode current (/RAS=VIL, /CAS, Address cycling : tHPC=tHPC min)	45ns	-	100	mA	1, 3
		50ns	-	90		
		60ns	-	80		
ICC5	CMOS interface (/RAS, /UCAS, /LCAS >= Vcc-0.2V, Dout = High-Z)		-	0.5	mA	
	Standby current (L-version)		-	200	uA	4
ICC6	/CAS-before-/RAS refresh current (tRC=tRC min)	45ns	-	130	mA	
		50ns	-	120		
		60ns	-	110		
ICC7	Battery back up operating current (standby with CBR) (tRC=31.25us, tRAS=300ns, Dout=High-Z)		-	350	uA	4, 5
ICC8	Standby current (CMOS) Power supply standby current /RAS=VIH, /UCAS./LCAS=VIL, Dout=Enable)		-	5	mA	1
ICC9	Self refresh current (/RAS, /UCAS, /LCAS <=0.2V, Dout=High-Z)		-	350	uA	5
II(L)	Input leakage current, Any input (0V<= Vin<=Vcc)		-5	5	uA	
IO(L)	Output leakage current, (Dout is disabled, 0V<= Vout<=Vcc)		-5	5	uA	

Note :

1. Icc depends on output load condition when the device is selected, Icc(max) is specified at the output open condition
2. Address can be changed once or less while RAS=VIL
3. Measured with one sequential address change per EDO cycle, tHPC
4. VIH>=Vcc-0.2V, 0V<=VIL<=0.2V
5. L-Version

CAPACITANCE (Vcc=3.3V +/-10%, TA=25°C)

Parameter	Symbol	Min.	Max	Unit	Note
Input capacitance (Address)	CI1	-	5	pF	1
Input capacitance (Clocks)	CI2	-	5	pF	1
Output capacitance (Data-in, Data-out)	CI/O	-	7	pF	1, 2

Note : 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. /RAS, /UCAS and /LCAS = V_{IH} to disable D_{out}

AC CHARACTERISTICS (Vcc=3.3V +/-10%, TA=0~70C, Note 1, 2, 19,20)

Test Condition

- Input rise and fall times = 2ns
- Input level : V_{IL}/V_{IH} = 0.0 / 0.3V
- Input timing reference level : V_{IL}/V_{IH} = 0.8/2.0V
- Output timing reference level : V_{OL}/V_{OH}=0.8/0.2V
- Output load : 1 TTL gate + C_L (100pF) including scope and jig

Read, Write, Read-modify-Write and Refresh Cycles

Parameter	Symbol	-45		-50		-60		Unit	Note
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	74	-	84	-	104	-	ns	
/RAS precharge time	tRP	25	-	30	-	40	-	ns	
/CAS precharge time	tCP	7	-	8	-	10	-	ns	24
/RAS pulse width	tRAS	45	10,000	50	10,000	60	10,000	ns	
/CAS pulse width	tCAS	7	10,000	8	10,000	10	10,000	ns	
Row address set-up time	tASR	0	-	0	-	0	-	ns	
Row address hold time	tRAH	7	-	8	-	10	-	ns	
Column address set-up time	tASC	0	-	0	-	0	-	ns	21
Column address hold time	tCAH	7	-	8	-	10	-	ns	21
/RAS to /CAS delay time	tRCD	11	33	12	37	14	45	ns	3
/RAS to Column address delay time	tRAD	9	22	10	25	12	30	ns	4
/RAS hold time	tRSH	12	-	13	-	15	-	ns	
/CAS hold time	tCSH	38	-	40	-	42	-	ns	
/CAS to /RAS precharge time	tCRP	5	-	5	-	5	-	ns	22

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Parameter	Symbol	-45		-50		-60		Unit	Note
		Min	Max	Min	Max	Min	Max		
/OE to Din delay time	tODD	12	-	13	-	15	-	ns	5
/OE delay time from Din	tDZO	0	-	0	-	0	-	ns	6
/CAS delay time from Din	tDZC	0	-	0	-	0	-	ns	6
Transition time (Rise and Fall)	tT	2	50	2	50	2	50	ns	7
Refresh period	tREF	-	64	-	64	-	64	ms	4K Ref.
Refresh period (L-version)		-	128	-	128	-	128	ms	4K Ref.

Read Cycles

Parameter	Symbol	-45		-50		-60		Unit	Note
		Min	Max	Min	Max	Min	Max		
Access time from /RAS	tRAC	-	45	-	50	-	60	ns	8, 9
Access time from /CAS	tCAC	-	12	-	13	-	15	ns	9,10,17
Access time from column address	tAA	-	23	-	25	-	30	ns	9,11,17
Access time from /OE	tOAC	-	12	-	13	-	15	ns	9
Read command set-up time	tRCS	0	-	0	-	0	-	ns	21
Read command hold time to /CAS	tRCH	0	-	0	-	0	-	ns	12,22
Read command hold time to /RAS	tRRH	0	-	0	-	0	-	ns	12
Column address to /RAS lead time	tRAL	23	-	25	-	30	-	ns	
Column address to /CAS lead time	tCAL	15	-	15	-	18	-	ns	
Output buffer turn off delay time from /CAS	tOFF	-	12	-	13	-	15	ns	13,26
Output buffer turn off delay time from /OE	tOEZ	-	12	-	13	-	15	ns	13
/CAS to Din delay time	tCDD	12	-	13	-	15	-	ns	5
/RAS to Din delay time	tRDD	12	-	13	-	15	-	ns	
/WE to Din delay time	tWDD	12	-	13	-	15	-	ns	
Output buffer turn off delay time from /RAS	tOFR	-	12	-	13	-	15	ns	13,26
Output buffer turn off delay time from /WE	tWEZ	-	12	-	13	-	15	ns	13
Output data hold time	tOH	3	-	3	-	3	-	ns	26
Output data hold time from /RAS	tOHR	3	-	3	-	3	-	ns	26
Read command hold time from /RAS	tRCHR	45	-	50	-	60	-	ns	
Output data hold time from /OE	tOHO	3	-	3	-	3	-	ns	
/CAS to output in low-Z	tCLZ	0	-	0	-	0	-	ns	

Write Cycles

Parameter	Symbol	-45		-50		-60		Unit	Note
		Min	Max	Min	Max	Min	Max		
Write command set-up time	tWCS	0	-	0	-	0	-	ns	14,21
Write command hold time	tWCH	7	-	8	-	10	-	ns	21
Write command pulse width	tWP	7	-	8	-	10	-	ns	
Write command to /RAS lead time	tRWL	12	-	13	-	15	-	ns	
Write command to /CAS lead time	tCWL	7	-	8	-	10	-	ns	23
Data-in set-up time	tDS	0	-	0	-	0	-	ns	15, 23
Data-in hold time	tDH	7	-	8	-	10	-	ns	15, 23

Read-Modify-Write Cycles

Parameter	Symbol	-45		-50		-60		Unit	Note
		Min	Max	Min	Max	Min	Max		
Read-modify-write cycle time	tRWC	101	-	116	-	140	-	ns	
/RAS to /WE delay time	tRWD	63	-	67	-	79	-	ns	14
/CAS to /WE delay time	tCWD	30	-	30	-	34	-	ns	14
Column address to /WE delay time	tAWD	40	-	42	-	49	-	ns	14
/OE hold time from /WE	tOEH	12	-	13	-	15	-	ns	

Refresh cycles

Parameter	Symbol	-45		-50		-60		Unit	Note
		Min	Max	Min	Max	Min	Max		
/CAS set-up time (/CAS-before-/RAS Refresh Cycle)	tCSR	5	-	5	-	5	-	ns	21
/CAS hold time (/CAS-before-/RAS Refresh Cycle)	tCHR	7	-	8	-	10	-	ns	22
/WE set-up time (/CAS-before-/RAS Refresh Cycle)	tWRP	0	-	0	-	0	-	ns	
/WE hold time (/CAS-before-/RAS Refresh Cycle)	tWRH	7	-	8	-	10	-	ns	
/RAS precharge to /CAS hold time (/CAS-before-/RAS Refresh Cycle)	tRPC	5	-	5	-	5	-	ns	21

Extended Data Out Mode Cycles

Parameter	Symbol	-45		-50		-60		Unit	Note
		Min	Max	Min	Max	Min	Max		
EDO page mode cyle time	tHPC	17	-	20	-	25	-	ns	25
Write pulse width during /CAS precharge	tWPE	7	-	8	-	10	-	ns	
EDO mode /RAS pulse width	tRASP	-	100K	-	100K	-	100K	ns	16
Access time from /CAS precharge	tACP	-	28	-	28	-	35	ns	9,17,22
/RAS hold time from /CAS precharge	tRHCP	26	-	28	-	35	-	ns	
/CAS hold time referred /OE	tCOL	7	-	8	-	10	-	ns	
/CAS to /OE set-up time	tCOP	5	-	5	-	5	-	ns	
Read command hold time from /CAS precharge	tRCHP	26	-	28	-	35	-	ns	
Output data hold time from /CAS low	tDOH	3	-	3	-	3	-	ns	9,27
/OE precharge time	tOEP	7	-	8	-	10	-	ns	

EDO Page Mode Read-Modify-Write Cycle

Parameter	Symbol	-45		-50		-60		Unit	Note
		Min	Max	Min	Max	Min	Max		
EDO read-modify-write cycle time	tHPRWC	57	-	57	-	68	-	ns	
EDO page mode read-modify-write cycle /CAS precharge to /WE delay time	tCPW	45	-	45	-	54	-	ns	14,22

Self Refresh Cycle (L-Version)

Parameter	Symbol	-45		-50		-60		Unit	Note
		Min	Max	Min	Max	Min	Max		
/RAS pulse width (self refresh)	tRASS	100	-	100	-	100	-	us	31
/RAS precharge time (self refresh)	tRPS	90	-	90	-	110	-	ns	31
/CAS hold time (self refresh)	tCHS	-50	-	-50	-	-50	-	ns	23

Notes :

1. AC measurements assume t_T = 2ns

2. AC initial pause of 200us is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing /RAS-only refresh or /CAS-before-/RAS refresh)

3. Operation with the t_{RCD}(max) limit insures that t_{RAC}(max) can be met, t_{RCD}(max) is specified as a reference point only : if t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.

4. Operation with the t_{RAD}(max) limit insures that t_{RAC}(max) can be met, t_{RAD}(max) is specified as a reference point only : if t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled exclusively by t_{AA}.

5. Either t_{ODD} or t_{CDD} must be satisfied.

6. Either t_{DZO} or t_{DZC} must be satisfied.

7. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals, also transition times are measured between V_{IH}(min) and V_{IL}(max)

8. Assumes that t_{RCD}<=t_{RCD}(max) and t_{RAD}<=t_{RAD}(max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown

9. Measured with a load circuit equivalent to 1 TTL loads and 100pF.

10. Assumes that t_{RCD}>=t_{RCD}(max) and t_{RCD} + t_{CAC}(max) >= t_{RAD} + t_{AA}(max)

11. Assumes that t_{RAD}>=t_{RAD}(max) and t_{RCD} + t_{CAC}(max) <= t_{RAD} + t_{AA}(max)

12. Either t_{RCH} of t_{RRH} must be satified for a read cycles

13. t_{OFF}(max), t_{OEZ}(max), t_{OFR}(max) and t_{WEZ}(max) define the time at which the outputs achieve the open circuit condition and is not referenced to output voltage levels

14 t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPW} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only : If t_{WCS} >=t_{WCS}(min), the cycle is an early write cycle and the data out pin will remain open circuit(high impedance) throughout the entire cycle : If t_{RWD}>=t_{RWD}(min), t_{CWD}>=t_{CWD}(min), t_{AWD}>=t_{AWD}(min), the cycle is a read-modify-write and the data output will contain data read from the selected cell : if neither of the above sets of conditions is satified, the condition of the data out (at access time) is indeterminate.

15. t_{DS} and t_{DH} are refered to /UCAS and /LCAS leading edge in early write cycles and to /WE leading edge in delayed write or read-modify-write cycles

16. t_{RASP} defineds /RAS pulse width in extended data out mode cycles

17. Access time is determined by the longest among t_{AA}, t_{CAC} and t_{ACP}

18 In delaying write or read-modify-write cycles, /OE must disable output buffer prior to applying data to the device.

19. When output buffers are enabled once, sustain the low impedence state until valid data is obtained. when output buffer is turned on and off within a very short time, generally it causes large Vcc/Vss line noise, which causes to degrade V_{IH} min / V_{IL} max level

20. When both /UCAS and /LCAS go low at the same time, all 16 bit data are written into the device. /UCAS and /LCAS cannot be staggered within the same write / read cycles

21. t_{ASC}, t_{CAH}, t_{RCS}, t_{WCS}, t_{WCH}, t_{CSR} and t_{RPC} are determined by the earlier falling edge of /UCAS or /LCAS

22. t_{CRP}, t_{CHR}, t_{RCH},t_{ACP} and t_{CPW} are determined by the later rising edge of /UCAS or /LCAS

23. t_{CWL}, t_{DH}, t_{DS} and t_{CHS} should be satified by the both /UCAS and /LCAS

24. t_{CP} is determined by the time that both /UCAS and /LCAS are high

25. t_{HPC}(min) can be achieved during a series of EDO mode early write cycles or EDO mode read cycels If both write and read operation are mixed in a EDO mode, /RAS cycle[EDO mode mix cycle (1)(2)] minimum value of /CAS cycle t_{HPC}[t_{CAS} + t_{CP} + 2t_T] become greater than the specified t_{HPC}(min) value. The value of CAS cycle time of mixed EDO page mode is shown in EDO page mode mix cycle (1) and (2)

26. Data output turns off and becomes high impedance from later rising edge of /RAS and /CAS. Hold time and turn off time are specified by the timing specifications of later rising edge of /RAS and /CAS between t_{OHR} and t_{OH} and between t_{OFR} and t_{OFF}

27. t_{DOH} defines the time at which the output level go cross, V_{OL}=0.8V, V_{OH}=2.0V of output timing reference level.

28. Before and after self refresh mode, execute CBR refresh to all refresh addresses in or within 64ms period on the condition a) and b) below
    a) Enter self refresh mode within 15.6us after either burst refresh or distributed refresh at equal interval to all refresh addresses are completed.
    b) Start burst refresh or distributed refresh at equal interval to all refresh addresses within 15.6us after exiting from self refresh mode

29. In case of entering from /RAS-only-refresh, It is necessary to execute CBR refresh before and after self refresh mode according as note 28

30. For L-version, It is available to apply each 128ms and 31.2us instead of 64ms and 15.6us at note 28

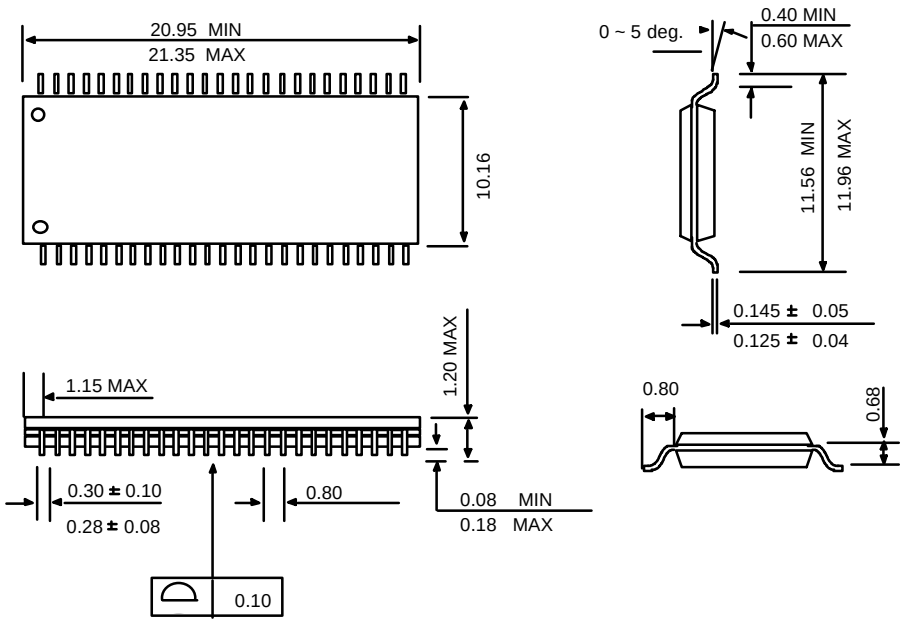
31. At t_{RASS} > 100us, self refresh mode is activated, and not active at t_{RASS} < 10us, It is undefined within the range of 10us < t_{RASS} < 100us. For t_{RASS} > 10us, It is necessary to satify t_{RPS}

32. XXX : H or L [H : V_{IH}(min) <= V_{IN} <=V_{IH}(max), L : V_{IH}(min) <=V_{IN} <=V_{IH}(max)]
    ///// : Invalid Dout
    When the address, clock and input pins are not described on timing waveforms, their pins must be applied V_{IH} or V_{IL}

PACKAGE INFORMATION

400mil 50pin TSOP- II Dimension

Unit: mm



Dimension including the plating thickness

Base material dimension