GM71V65163C
GM71VS65163CL

4,196,304 WORDS x 16 BIT
MOS DYNAMIC RAM

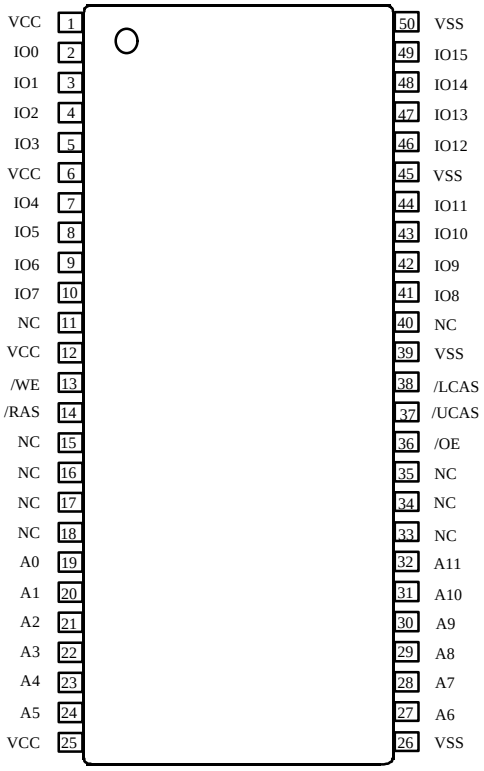
Description

The GM71V(S)65163C/CL is the new generation dynamic RAM organized 4,196,304 words by 16 bits. The GM71V(S)65163C/CL utilizes advanced CMOS Silicon Gate Process Technology as well as advanced circuit techniques for wide operating margins, both internally and to the system user. System oriented features include single power supply of 3.3V+/-10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

The GM71V(S)65163C/CL offers Extended Data Out(EDO) Mode as a high speed access mode.

Pin Configuration

50 SOJ / TSOP-II



(Top View)

Features

* 4,196,304 Words x 16 Bit
* Extended Data Out (EDO) Mode Capability
* Fast Access Time & Cycle Time

(Unit: ns)

	t_{RAC}	t_{AA}	t_{CAC}	t_{RC}	t_{HPC}
GM71V(S)65163C/CL-5	50	25	13	90	20
GM71V(S)65163C/CL-6	60	30	15	110	25

*Power dissipation
- Active : 540mW/504mW(MAX)
- Standby : 1.8 mW (CMOS level : MAX)
0.54mW (L-Version : MAX)

*EDO page mode capability
*Access time : 50ns/60ns (max)
*Refresh cycles
- $\overline{RAS}$ only Refresh
4096 cycles/64 ms (GM71V65163C)
4096 cycles/128ms (GM71VS65163CL)(L_Version)
*CBR & Hidden Refresh
4096 cycles/64 ms (GM71V65163C)
4096 cycles/128 ms (GM71VS65163CL)(L-Version)
*4 variations of refresh
-$\overline{RAS}$-only refresh
-$\overline{CAS}$-before-$\overline{RAS}$ refresh
-Hidden refresh
-Self refresh (L-Version)
*Single Power Supply of 3.3V+/-10 % with a built-in VBB generator
*Battery Back Up Operation (L-Version)

Pin Description

Pin	Function	Pin	Function
A0-A11	Address Inputs	$\overline{WE}$	Write Enable
A0-A11	Refresh Address Inputs	I/O0 - I/O15	Data Input / Output
$\overline{RAS}$	Row Address Strobe	V_{CC}	Power (+3.3V)
$\overline{UCAS}$,$\overline{LCAS}$	Column Address Strobe	V_{SS}	Ground
$\overline{OE}$	Output Enable	NC	No Connection

Ordering Information

Type No.	Access Time	Package
GM71V(S)65163C/CLJ-5 GM71V(S)65163C/CLJ-6	50ns 60ns	400 Mil 50Pin Plastic SOJ
GM71V(S)65163C/CLT-5 GM71V(S)65163C/CLT-6	50ns 60ns	400 Mil 50Pin Plastic TSOP II

Absolute Maximum Ratings*

Symbol	Parameter	Rating	Unit
T_{STG}	Storage Temperature (Plastic)	-55 to 125	C
V_T	Voltage on any Pin Relative to V_{SS}	-0.5 to V_{CC} + 0.5 (MAX ; 4.6V)	V
V_{CC}	Voltage on V_{CC} Relative to V_{SS}	-0.5 to 4.6	V
I_{OUT}	Short Circuit Output Current	50	mA
P_T	Power Dissipation	1.0	W

*Note : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

Recommended DC Operating Conditions (T_A = 0 ~ 70C)

Symbol	Parameter	Min	Typ	Max	Unit	Notes
V_{CC}	Supply Voltage	3.0	3.3	3.6	V	1,2
V_{SS}	Supply Voltage	0	0	0	V	2
V_{IH}	Input High Voltage	2.0	-	Vcc+0.3	V	1
V_{IL}	Input Low Voltage	-0.3	-	0.8	V	1
T_A	Ambient Temperature under Bias	0	-	70	C	

DC Electrical Characteristics: (V_{CC} = 3.3V+/-10%, T_A = 0 ~ 70C)

Symbol	Parameter		Min	Max	Unit	Note
V_{OH}	Output Level Output Level Voltage (I_{OUT} = -2mA)		2.4	V_{CC}	V	
V_{OL}	Output Level Output Level Voltage (I_{OUT} = 2mA)		0	0.4	V	
I_{CC1}	Operating Current (t_{RC} = t_{RC} min)	50ns	-	150	mA	1,2
		60ns	-	140		
I_{CC2}	Standby Current (TTL interface) Power Supply Standby Current (RAS, UCAS,LCAS= V_{IH}, D_{OUT} = High-Z)		-	2	mA	
I_{CC3}	RAS-Only Refresh Current (t_{RC} = t_{RC} min)	50ns	-	150	mA	2
		60ns	-	140		
I_{CC4}	Extended Data Out page Mode Current (RAS = V_{IL}, CAS, Address Cycling: t_{HPC} = t_{HPC} min)	50ns	-	120	mA	1,3
		60ns	-	110		
I_{CC5}	CMOS interface (RAS, UCAS,LCAS>=V_{CC}-0.2V, D_{OUT} = High-Z)		-	0.5	mA	
	Standby Current(L_Version)		-	300	uA	4
I_{CC6}	CAS-before-RAS Refresh Current (t_{RC} = t_{RC} min)	50ns	-	150	mA	
		60ns	-	140		
I_{CC7}	Battery Back Up Operating Current(Standby with CBR) (tRC=31.25us,,tRAS=300ns,Dout=High-Z)		-	500	uA	4, 5
I_{CC8}	Standby Current (CMOS) Power Supply Standby Current RAS = V_{IH},UCAS, LCAS = V_{IL}, D_{OUT} = Enable		-	5	mA	1
I_{CC9}	Self Refresh Current (RAS,UCAS,LCAS <=0.2V,Dout=High-Z)		-	400	uA	5
$I_{I(L)}$	Input Leakage Current, Any Input (0V<=V_{IN}<=Vcc)		-5	5	uA	
$I_{O(L)}$	Output Leakage Current (D_{OUT} is Disabled, 0V<=V_{OUT}<=Vcc)		-5	5	uA	

Note: 1. I_{CC} depends on output load condition when the device is selected. $I_{CC(max)}$ is specified at the output open condition.
2. Address can be changed once or less while RAS = V_{IL}.
3. Measured with one sequential address change per EDO cycle, t_{HPC}.
4. V_{IH}>=V_{CC}-0.2V, 0V<=V_{IL}<=0.2V
5. L-Version

Capacitance (V_{CC} = 3.3V+/-10%, T_A = 25C)

Symbol	Parameter	Typ	Max	Unit	Note
C_{I1}	Input Capacitance (Address)	-	5	pF	1
C_{I2}	Input Capacitance (Clocks)	-	7	pF	1
$C_{I/O}$	Output Capacitance (Data-in,Data-Out)	-	7	pF	1, 2

Note: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{RAS}$, $\overline{UCAS}$ and $\overline{LCAS}$ = V_{IH} to disable D_{OUT}.

AC Characteristics (V_{CC} = 3.3V+/-10%, T_A = 0 ~ 70C, Notes 1, 2,19,20)

Test Conditions

Input rise and fall times : 2ns
Input level : V_{IL}/V_{IH} = 0.0/3.0V
Input timing reference levels : V_{IL}/V_{IH} = 0.8/2.0V
Output timing reference levels : V_{OL}/V_{OH} = 0.8/2.0V
Output load : 1 TTL gate+C_L (100pF)
(Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Symbol	Parameter	GM71V(S)65163C/CL-5		GM71V(S)65163C/CL-6		Unit	Notes
		Min	Max	Min	Max		
t_{RC}	Random Read or Write Cycle Time	84	-	104	-	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	30	-	40	-	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	8	-	10	-	ns	24
t_{RAS}	$\overline{RAS}$ Pulse Width	50	10000	60	10000	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	8	10000	10	10000	ns	
t_{ASR}	Row Address Set-up Time	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	8	-	10	-	ns	
t_{ASC}	Column Address Set-up Time	0	-	0	-	ns	21
t_{CAH}	Column Address Hold Time	8	-	10	-	ns	21
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	12	37	14	45	ns	3
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	10	25	12	30	ns	4
t_{RSH}	$\overline{RAS}$ Hold Time	13	-	15	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	35	-	40	-	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	-	5	-	ns	22
t_{ODD}	$\overline{OE}$ to D_{IN} Delay Time	13	-	15	-	ns	5
t_{DZO}	$\overline{OE}$ Delay Time from D_{IN}	0	-	0	-	ns	6
t_{DZC}	$\overline{CAS}$ Delay Time from D_{IN}	0	-	0	-	ns	6
t_T	TransitionTime (Rise and Fall)	2	50	2	50	ns	7
t_{REF}	Refresh Period	-	64	-	64	ms	4096 cycles
	Refresh Period (L-Version)	-	128	-	128	ms	4096 cycles

Read Cycles

Symbol	Parameter	GM71V(S)65163C/CL-5		GM71V(S)65163C/CL-6		Unit	Notes
		Min	Max	Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	-	50	-	60	ns	8,9
t_{CAC}	Access Time from $\overline{CAS}$	-	13	-	15	ns	9,10,17
t_{AA}	Access Time from Column Address	-	25	-	30	ns	9,11,17
t_{OAC}	Access Time from $\overline{OE}$	-	13	-	15	ns	9
t_{RCS}	Read Command Set-up Time	0	-	0	-	ns	21
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	-	0	-	ns	12,22
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	0	-	0	-	ns	12
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	25	-	30	-	ns	
t_{CAL}	Column Address to $\overline{CAS}$ Lead Time	15	-	18	-	ns	
t_{OFF}	Output Buffer Turn-off Delay Time from $\overline{CAS}$	-	13	-	15	ns	13,26
t_{OEZ}	Output Buffer Turn-off Delay Time from $\overline{OE}$	-	13	-	15	ns	13
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	13	-	15	-	ns	5
t_{RDD}	$\overline{RAS}$ to D_{IN} Delay Time	13	-	15	-	ns	
t_{WDD}	$\overline{WE}$ to D_{IN} Delay Time	13	-	15	-	ns	
t_{OFR}	Output Buffer Turn-off Delay Time from $\overline{RAS}$	-	13	-	15	ns	13,26
t_{WEZ}	Output Buffer Turn-off Delay Time from $\overline{WE}$	-	13	-	15	ns	13
t_{OH}	Output Data Hold Time	3	-	3	-	ns	26
t_{OHR}	Output Data Hold Time from $\overline{RAS}$	3	-	3	-	ns	26
t_{RCHR}	Read Command Hold Time from $\overline{RAS}$	50	-	60	-	ns	
t_{OHO}	Output data hold time from $\overline{OE}$	3	-	3	-	ns	
t_{CLZ}	$\overline{CAS}$ to Output in Low - Z	0	-	0	-	ns	

Write Cycles

Symbol	Parameter	GM71V(S)65163C/CL-5		GM71V(S)65163C/CL-6		Unit	Notes
		Min	Max	Min	Max		
t_{WCS}	Write Command Set-up Time	0	-	0	-	ns	14,21
t_{WCH}	Write Command Hold Time	8	-	10	-	ns	21
t_{WP}	Write Command Pulse Width	8	-	10	-	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	13	-	15	-	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	8	-	10	-	ns	23
t_{DS}	Data-in Set-up Time	0	-	0	-	ns	15,23
t_{DH}	Data-in Hold Time	8	-	10	-	ns	15,23

Read-Modify-Write Cycles

Symbol	Parameter	GM71V(S)65163C/CL-5		GM71V(S)65163C/CL-6		Unit	Notes
		Min	Max	Min	Max		
t_{RWC}	Read-Modify-Write Cycle Time	116	-	140	-	ns	
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	67	-	79	-	ns	14
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	30	-	34	-	ns	14
t_{AWD}	Column Address to $\overline{WE}$ Delay Time	42	-	49	-	ns	14
t_{OEH}	$\overline{OE}$ Hold Time from $\overline{WE}$	13	-	15	-	ns	

Refresh Cycles

Symbol	Parameter	GM71V(S)65163C/CL-5		GM71V(S)65163C/CL-6		Unit	Notes
		Min	Max	Min	Max		
t_{CSR}	$\overline{CAS}$ Set-up Time ($\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle)	5	-	5	-	ns	21
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle)	8	-	10	-	ns	22
t_{WRP}	$\overline{WE}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle)	0	-	0	-	ns	
t_{WRH}	$\overline{WE}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle)	8	-	10	-	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	5	-	5	-	ns	21

Extended Data Out Mode Cycles

Symbol	Parameter	GM71V(S)65163C/CL-5		GM71V(S)65163C/CL-6		Unit	Notes
		Min	Max	Min	Max		
t_{HPC}	EDO Page Mode Cycle Time	20	-	25	-	ns	25
t_{WPE}	Write pulse width during $\overline{CAS}$ Precharge	8	-	10	-	ns	
t_{RASP}	EDO Mode $\overline{RAS}$ Pulse Width	-	100000	-	100000	ns	16
t_{ACP}	Access Time from $\overline{CAS}$ Precharge	-	28	-	35	ns	9,17,22
t_{RHCP}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	28	-	35	-	ns	
t_{COL}	$\overline{CAS}$ Hold Time Referred $\overline{OE}$	8	-	10	-	ns	
t_{COP}	$\overline{CAS}$ to $\overline{OE}$ set-up Time	5	-	5	-	ns	
t_{RCHP}	Read Command Hold Time from $\overline{CAS}$ Precharge	28	-	35	-	ns	
t_{DOH}	Output Data Hold Time from $\overline{CAS}$ Low	3	-	3	-	ns	9,27
t_{OEP}	$\overline{OE}$ Precharge Time	8	-	10	-	ns	

EDO Page Mode Read-Modify-Write cycle

Symbol	Parameter	GM71V(S)65163C/CL-5		GM71V(S)65163C/CL-6		Unit	Notes
		Min	Max	Min	Max		
t_{HPRWC}	EDO Read-Modify-Write Cycle Time	57	-	68	-	ns	
t_{CPW}	EDO Page Mode Read-Modify-Write Cycle $\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time	45	-	54	-	ns	14,22

Self Refresh Cycles (L_Version)

Symbol	Parameter	GM71V(S)65163C/CL-5		GM71V(S)65163C/CL-6		Unit	Notes
		Min	Max	Min	Max		
t_{RASS}	$\overline{RAS}$ Pulse Width(Self-Refresh)	100	-	100	-	us	31
t_{RPS}	$\overline{RAS}$ Precharge Time(Self-Refresh)	90	-	110	-	us	31
t_{CHS}	$\overline{CAS}$ Hold Time(Self-Refresh)	-50	-	-50	-	us	23

Notes:

1. AC measurements assume t_T = 2ns.
2. AC initial pause of 200us is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$-only refresh or $\overline{CAS}$-before-$\overline{RAS}$ refresh)
3. Operation with the t_{RCD}(max) limit insures that t_{RAC}(max) can be met, t_{RCD}(max) is specified as a reference point only: if t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
4. Operation with the t_{RAD}(max) limit insures that t_{RAC}(max) can be met, t_{RAD}(max) is specified as a reference point only: if t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled exclusively by t_{AA}.
5. Either t_{ODD} or t_{CDD} must be satisfied.
6. Either t_{DZO} or t_{DZC} must be satisfied.
7. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH}(min) and V_{IL} (max).
8. Assumes that t_{RCD}<=t_{RCD}(max) and t_{RAD}<=t_{RAD}(max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
9. Measured with a load circuit equivalent to 1 TTL loads and 100 pF.
10. Assumes that t_{RCD}>=t_{RCD}(max) and t_{RCD} + t_{CAC}(max) >=t_{RAD} + t_{AA}(max).
11. Assumes that t_{RAD} >=t_{RAD} (max) and t_{RCD} + t_{CAC}(max)<=t_{RAD} + t_{AA}(max).
12. Either t_{RCH} or t_{RRH} must be satisfied for a read cycles.
13. t_{OFF}(max), t_{OEZ}(max), t_{OFR}(max) and t_{WEZ}(max) define the time at which the outputs achieve the open circuit condition and is not referenced to output voltage levels.
14. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD}, and t_{CPW} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if t_{WCS} >=t_{WCS}(min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle: if t_{RWD}>=t_{RWD}(min), t_{CWD}>=t_{CWD}(min), t_{AWD}>=t_{AWD}(min) and t_{CPW}>=t_{CPW}(min), the cycle is a read-modify-write and the data output will contain data read from the selected cell: if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
15. t_{DS} and t_{DH} are referred to $\overline{UCAS}$ and $\overline{LCAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.
16. t_{RASP} defines $\overline{RAS}$ pulse width in extended data out mode cycles.
17. Access time is determined by the longest among t_{AA}, t_{CAC} and t_{ACP}.
18. In delayed write or read-modify-write cycles, $\overline{OE}$ must disable output buffer prior to applying data to the device.
19. When output buffers are enabled once, sustain the low impedance state until valid data is obtained. When output buffer is turned on and off within a very short time, generally it causes large V_{CC}/V_{SS} line noise, which causes to degrade V_{IH} min/V_{IL} max level.
20. When both $\overline{UCAS}$ and $\overline{LCAS}$ go low at the same time, all 16-bit data are written into the device. $\overline{UCAS}$ and $\overline{LCAS}$ cannot be staggered within the same write/read cycles.
21. t_{ASC}, t_{CAH}, t_{RCS}, t_{WCS}, t_{WCH}, t_{CSR} and t_{RPC} are determined by the earlier falling edge of $\overline{UCAS}$ or $\overline{LCAS}$.
22. t_{CRP}, t_{CHR}, t_{RCH}, t_{ACP} and t_{CPW} are determined by the later rising edge of $\overline{UCAS}$ or $\overline{LCAS}$.

23. t_{CWL}, t_{DH}, t_{DS} and t_{CHS} should be satisfied by the both $\overline{UCAS}$ and $\overline{LCAS}$.
24. t_{CP} is determined by the time that both UCAS and LCAS are high.
25. t_{HPC}(min) can be achieved during a series of EDO mode early write cycles or EDO mode read cycles. If both write and read operation are mixed in a EDO mode, $\overline{RAS}$ cycle { EDO mode mix cycle (1),(2) } minimum value of $\overline{CAS}$ cycle t_{HPC}(t_{CAS} + t_{CP} + 2t_T) becomes greater than the specified t_{HPC}(min) value. The value of CAS cycle time of mixed EDO page mode is shown in EDO page mode mix cycle (1) and (2).
26. Data output turns off and becomes high impedance from later rising edge of $\overline{RAS}$ and $\overline{CAS}$. Hold time and turn off time are specified by the timing specifications of later rising edge of $\overline{RAS}$ and $\overline{CAS}$ between t_{OHR} and t_{OH}, and between t_{OFR} and t_{OFF}.
27. t_{DOH} defines the time at which the output level go cross. V_{OL}=0.8V, V_{OH}=2.0V of output timing reference level.
28. Before and after self refresh mode, execute CBR refresh to all refresh addresses in or within 64ms period on the condition a and b below.

    a. Enter self refresh mode within 15.6us after either burst refresh or distributed refresh at equal interval to all refresh addresses are completed.

    b. Start burst refresh or distributed refresh at equal interval to all refresh addressed within 15.6us after exiting from self refresh mode.
29. In case of entering from $\overline{RAS}$-only-refresh, it is necessary to execute CBR refresh before and after self refresh mode according as note 28.
30. For L_Version, it is available to apply each 128§ Â and 31.2us instead of 64§ Âand 15.6us at note 28.
31. At t_{RASS} > 100 us , self refresh mode is activated, and not active at t_{RASS} <10us. It is undefined within the range of 10 us < t_{RASS} < 100 us . for t_{RASS} > 10 us , it is necessary to satisfy t_{RPS}.
32. XXX: H or L (H : V_{IH}(min)<=V_{IN}<=V_{IH}(max), L: V_{IH}(min)<=V_{IN}<=V_{IH}(max))

    ///////: Invalid Dout

    When the address, clock and input pins are not described on timing waveforms, their pins must be applied V_{IH} or V_{IL}.

TSOP-II 50 PIN Package Dimension