

# HD14160B, HD14161B HD14162B, HD14163B

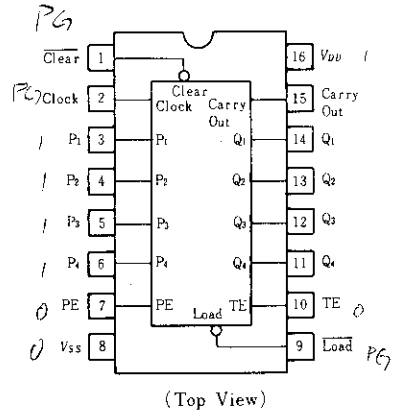
- HD14160B.....Decade Counter with Asynchronous Clear
- HD14161B.....4-bit Binary Counter with Asynchronous Clear
- HD14162B.....Decade Counter with Synchronous Clear
- HD14163B.....4-bit Binary Counter with Synchronous Clear

The HD14160B to HD14163B are synchronous programmable counters and functionally equivalent to the 74160 to 74163 TTL counters. Two are synchronous programmable decade counters with asynchronous and synchronous clear inputs respectively (HD14160B, HD14162B). The other two are synchronous programmable 4-bit binary counters with the asynchronous and synchronous clear respectively (HD14161B, HD14163B).

## ■ FEATURES

- Internal Look-Ahead for Fast Counting
- Carry Output for N-bit Cascading
- Synchronously Programmable
- Synchronous Counting
- Load Control Line
- Synchronous or Asynchronous Clear Positive Edge Clocked

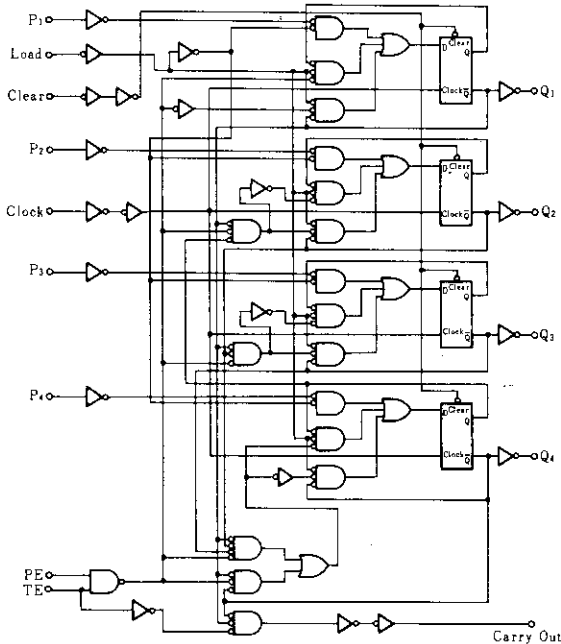
## ■ PIN ARRANGEMENT



## ■ LOGIC DIAGRAM

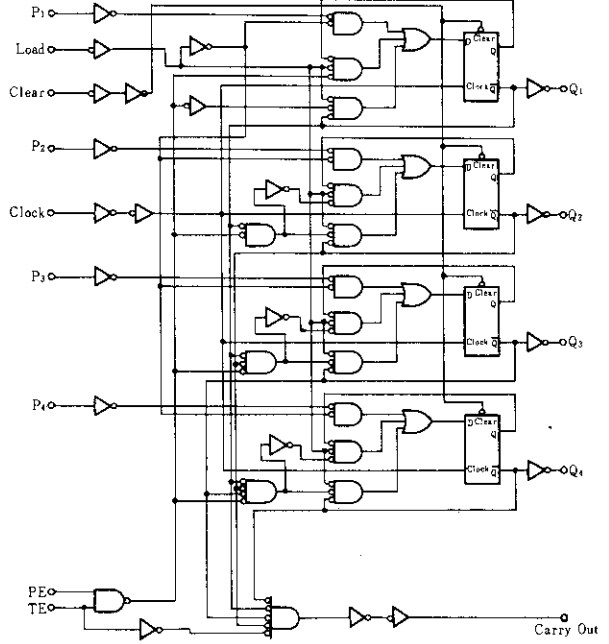
### ● HD14160B, HD14162B

(Clear is synchronous for HD14162B)



### ● HD14161B, HD14163B

(Clear is Synchronous for HD14163B)

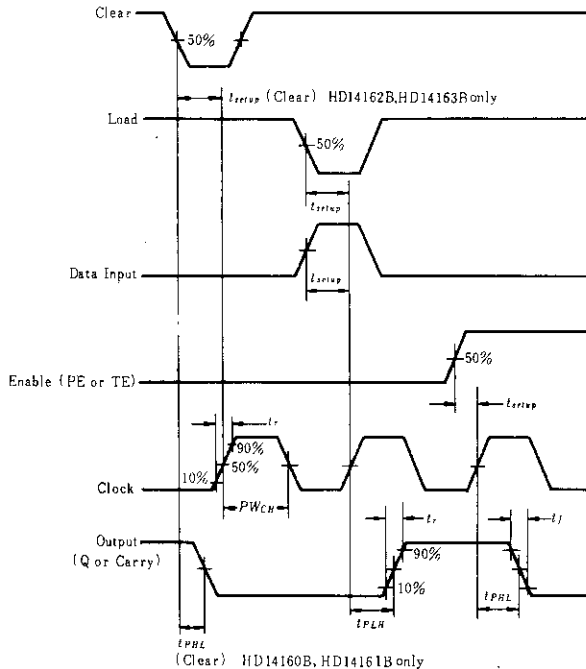


**ELECTRICAL CHARACTERISTICS**

Characteristic	Symbol	Test Conditions	-40°C		25°C			85°C		Unit	
			min	max	min	typ	max	min	max		
Output Voltage	$V_{OL}$	$V_{DD}$ (V)									
		5.0		0.05	—	0	0.05	—	0.05	V	
		10	$V_{in}=V_{DD}$ or 0	—	0.05	—	0	0.05	—		0.05
	15		—	0.05	—	0	0.05	—	0.05		
	$V_{OH}$	5.0		4.95	—	4.95	5.0	—	4.95	V	
		10	$V_{in}=0$ or $V_{DD}$	9.95	—	9.95	10	—	9.95		
15			14.95	—	14.95	15	—	14.95			
Input Voltage	$V_{IL}$	5.0	$V_{out}=4.5$ or $0.5V$	—	1.5	—	2.25	1.5	—	1.5	V
		10	$V_{out}=9.0$ or $1.0V$	—	3.0	—	4.50	3.0	—	3.0	
		15	$V_{out}=13.5$ or $1.5V$	—	4.0	—	6.75	4.0	—	4.0	
	$V_{IH}$	5.0	$V_{out}=0.5$ or $4.5V$	3.5	—	3.5	2.75	—	3.5	—	V
		10	$V_{out}=1.0$ or $9.0V$	7.0	—	7.0	5.50	—	7.0	—	
		15	$V_{out}=1.5$ or $13.5V$	11.0	—	11.0	8.25	—	11.0	—	
Output Drive Current	$I_{OH}$	5.0	$V_{OH}=2.5V$	-2.5	—	-2.1	-4.2	—	-1.7	—	mA
		5.0	$V_{OH}=4.6V$	-0.52	—	-0.44	-0.88	—	-0.36	—	
		10	$V_{OH}=9.5V$	-1.3	—	-1.1	-2.25	—	-0.9	—	
		15	$V_{OH}=13.5V$	-3.6	—	-3.0	-8.8	—	-2.4	—	
	$I_{OL}$	5.0	$V_{OL}=0.4V$	0.52	—	0.44	0.88	—	0.36	—	mA
		10	$V_{OL}=0.5V$	1.3	—	1.1	2.25	—	0.9	—	
15		$V_{OL}=1.5V$	3.6	—	3.0	8.8	—	2.4	—		
Input Current	$I_{in}$	15		—	$\pm 0.3$	—	$\pm 0.0001$	$\pm 0.3$	—	$\pm 1.0$	$\mu A$
Input Capacitance	$C_{in}$	—	$V_{in}=0$	—	—	—	5.0	7.5	—	—	pF
Quiescent Current	$I_{DD}$	5.0	Zero Signal, per Package	—	20	—	0.005	20	—	150	$\mu A$
		10		—	40	—	0.010	40	—	300	
		15		—	80	—	0.015	80	—	600	
Total Supply Current*	$I_T$	5.0	Dynamic $+I_{DD}$ ,	—	—	—	0.56	—	—	—	$\mu A$
		10	per Gate, $C_L=50pF$	—	—	—	1.1	—	—	—	
		15	$f=1kHz$	—	—	—	1.9	—	—	—	

\* To calculate total supply current at frequency other than 1kHz.  
 @ $V_{DD}=5.0V$   $I_T=(0.56\mu A/kHz)f+I_{DD}$ , @ $V_{DD}=10V$   $I_T=(1.1\mu A/kHz)f+I_{DD}$ , @ $V_{DD}=15V$   $I_T=(1.9\mu A/kHz)f+I_{DD}$

**DYNAMIC SIGNAL WAVEFORMS**

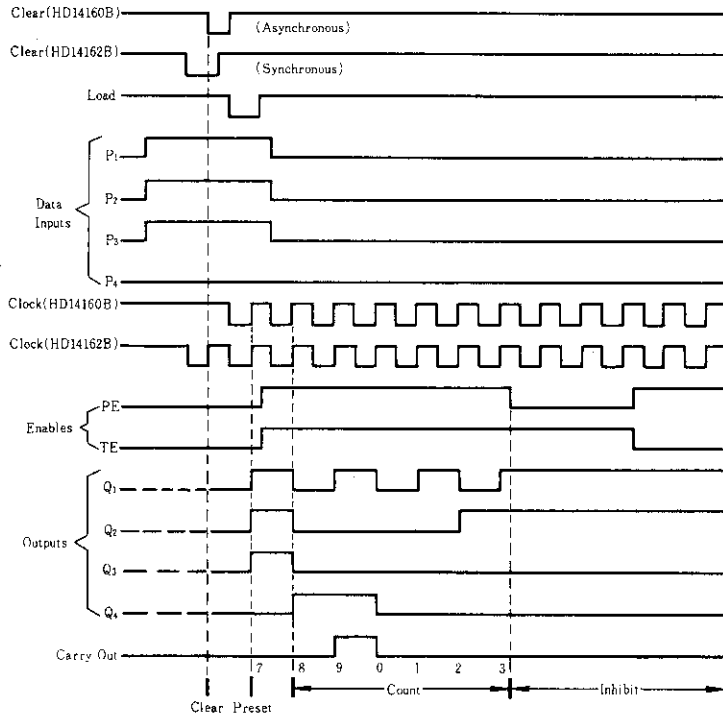


■ SWITCHING CHARACTERISTICS ( $C_L=50\text{pF}$ ,  $T_a=25^\circ\text{C}$ )

Characteristic		Symbol	$V_{DD}$ (V)	min	typ	max	Unit
Output Rise Time		$t_r$	5.0	—	100	200	ns
			10	—	50	100	
			15	—	40	80	
Output Fall Time		$t_f$	5.0	—	100	200	ns
			10	—	50	100	
			15	—	40	80	
Propagation Delay Time	Clock to Q	$t_{PLH}$ $t_{PHL}$	5.0	—	350	700	ns
			10	—	150	300	
			15	—	100	200	
	Clock to Carry Out		5.0	—	440	880	
			10	—	185	370	
			15	—	125	250	
	TE to Carry Out		5.0	—	300	600	
			10	—	130	260	
			15	—	90	180	
	Clear to Q (HD14160B, HD14161B only)		5.0	—	155	310	
			10	—	55	110	
			15	—	35	70	
Setup Time	Data to Clock	$t_{setup}$	5.0	320	160	—	ns
			10	130	65	—	
			15	90	45	—	
	Load to Clock		5.0	600	300	—	
			10	260	130	—	
			15	180	90	—	
	Enable to Clock (PE or TE)		5.0	420	210	—	
			10	170	85	—	
			15	120	60	—	
	Clear to Clock (HD14162B, HD14163B only)		5.0	310	155	—	
			10	110	55	—	
			15	70	35	—	
Clock Pulse Width		$PW_{CH}$	5.0	250	125	—	ns
			10	100	50	—	
			15	70	35	—	
Clock Rise Time		$t_r$	5.0	—	—	15	$\mu\text{s}$
			10	—	—	15	
			15	—	—	15	
Clock Frequency		$PRF$	5.0	—	2.0	1.0	MHz
			10	—	5.0	2.5	
			15	—	8.0	4.0	

■ TIMING DIAGRAM

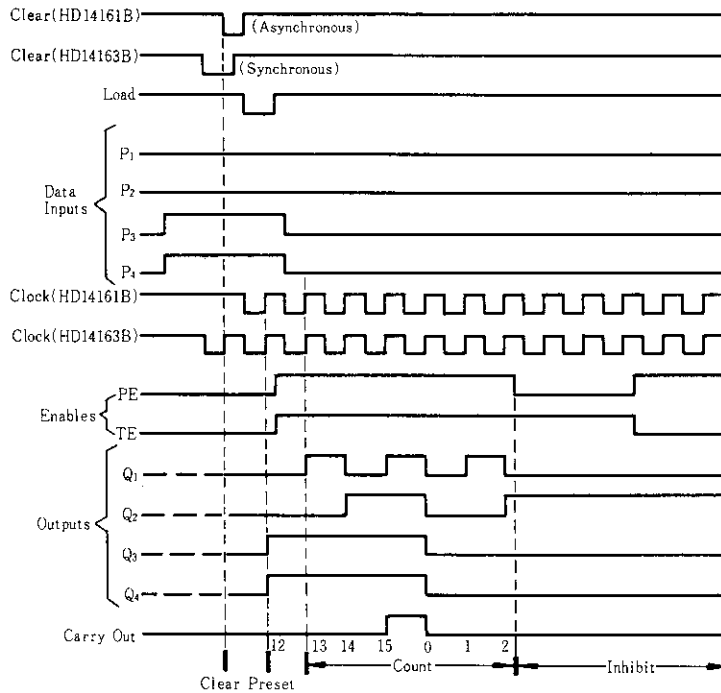
● HD14160B, HD14162B



Sequence illustrated in waveforms :

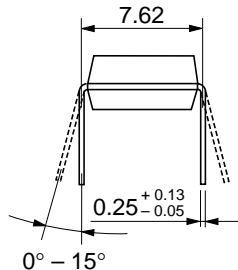
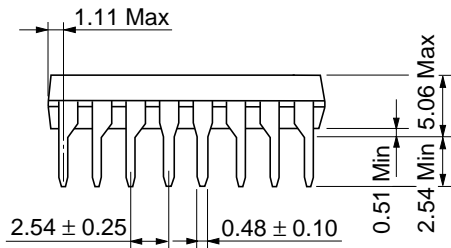
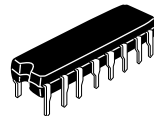
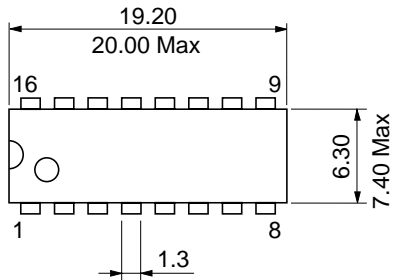
1. Clear outputs to zero.
2. Preset to BCD seven.
3. Count to eight, nine, zero, one, two, and three.
4. Inhibit

● HD14161B, HD14163B



Sequence illustrated in waveforms :

1. Clear outputs to zero.
2. Preset to binary twelve.
3. Count to thirteen, fourteen, fifteen, zero, one, and two.
4. Inhibit



Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	1.07 g

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# HITACHI

## Hitachi, Ltd.

Semiconductor & Integrated Circuits.  
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan  
Tel: Tokyo (03) 3270-2111 Fax: (03) 3270-5109

URL      North America      : <http://semiconductor.hitachi.com/>  
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## For further information write to:

Hitachi Semiconductor  
(America) Inc.  
179 East Tasman Drive,  
San Jose, CA 95134  
Tel: <1> (408) 433-1990  
Fax: <1> (408) 433-0223

Hitachi Europe GmbH  
Electronic components Group  
Dornacher Straße 3  
D-85622 Feldkirchen, Munich  
Germany  
Tel: <49> (89) 9 9180-0  
Fax: <49> (89) 9 29 30 00

Hitachi Europe Ltd.  
Electronic Components Group.  
Whitebrook Park  
Lower Cookham Road  
Maidenhead  
Berkshire SL6 8YA, United Kingdom  
Tel: <44> (1628) 585000  
Fax: <44> (1628) 778322

Hitachi Asia Pte. Ltd.  
16 Collyer Quay #20-00  
Hitachi Tower  
Singapore 049318  
Tel: 535-2100  
Fax: 535-1533

Hitachi Asia Ltd.  
Taipei Branch Office  
3F, Hung Kuo Building, No.167,  
Tun-Hwa North Road, Taipei (105)  
Tel: <886> (2) 2718-3666  
Fax: <886> (2) 2718-8180

Hitachi Asia (Hong Kong) Ltd.  
Group III (Electronic Components)  
7/F., North Tower, World Finance Centre,  
Harbour City, Canton Road, Tsim Sha Tsui,  
Kowloon, Hong Kong  
Tel: <852> (2) 735 9218  
Fax: <852> (2) 730 0281  
Telex: 40815 HITEC HX

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