FUJITSU SEMICONDUCTOR
DATA SHEET

DS07-13712-4E

16-Bit Proprietary Microcontroller

CMOS

F²MC-16LX MB90470 Series

MB90473/474/477/478/F474L/F474H

■ DESCRIPTIONS

The FUJITSU MB90470 Series is a 16-bit general-purpose microcontroller designed for consumer products and other process control applications requiring high-speed and real-time processing.

The F²MC-16LX CPU core instruction set retains the AT architecture of the F²MC*1 family, with additional instructions for use with high-level languages, expanded addressing mode, enhanced multiply and divide instructions, and full bit processing. Also included is a built-in 32-bit accumulator for long-word processing.

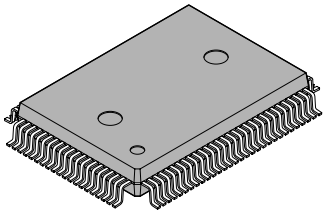
Peripheral resources built into the MB90470 series include 8/16-bit PPG, expanded I/O serial interface, UART, 10-bit A/D converter, 16-bit input-output timer, 8/16-bit up-counter, PWC timer, I²C*2 interface, DTP/external interrupt, chip select, and 16-bit reload timer.

*1 : F²MC is an abbreviation for FUJITSU Flexible Microcontroller, and is a registered trademark of FUJITSU, Ltd.

*2 : I²C license :
This product includes licensing of Philips I²C patents if used by the customer in an I²C system subject to the I²C standard specifications established by Philips.

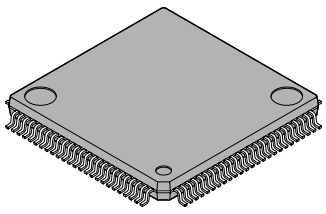
■ PACKAGES

100-pin plastic QFP



(FPT-100P-M06)

100-pin plastic LQFP



(FPT-100P-M05)

FUJITSU

■ FEATURES

- **Clocks**
  Minimum instruction execution time :
  50.0 ns at 5 MHz base oscillation with 4 × multiplier (internal operation at 20 MHz/3.3 V ± 0.3 V)
  62.5 ns at 4 MHz base oscillation with 4 × multiplier (internal operation at 16 MHz/3.0 V ± 0.3 V)
  Uses PLL clock multiplier.
- **Maximum memory size**
  16 Mbytes
- **Instruction set optimized for control applications**
  Handles bit, byte, word, long-word data
  23 standard addressing modes
  32-bit accumulator for enhanced high-precision calculation
  Signed multiply-divide and expanded RETI instructions
- **Instruction system compatible with high-level language (C) multitasking**
  System stack pointer
  Instruction set correlation and barrel shift instructions
- **Non-multi bus or multi-bus compatible**
- **Program patch function (for two address pointers)**
- **Improved execution speed**
  4-byte queue
- **Powerful interrupt functions**
  8 external interrupt functions with 8-level programmable priority
- **Data transfer functions (μDMA or Extended intelligent I/O service)**
  16 channels maximum
  μDMA maximum assured operation frequency : 16 MHz
  Extended intelligent I/O service maximum assured operation frequency : 20 MHz
- **Built-in ROM**
  Flash versions : 256 KB, Mask ROM versions : 128 KB/256 KB
- **Built-in RAM**
  10 KB/16 KB
- **General purpose ports**
  84 ports maximum
  (includes 16 ports with input pull-up resistance setting, 14 ports with output open drain setting)
- **A/D converter**
  RC sequential comparator type, 8 channels
  10-bit resolution, conversion time 4.65 μs (at 20 MHz operation)
- **I²C interface**
  1 channel
- **μPG**
  1 channel
- **UART**
  1 channel
- **I/O expansion serial interface (SIO)**
  2 channels
- **8/16-bit up/down timer**
  1 channel
- **16-bit PWC**
  3 channels (including 2-channel input comparison function)

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- **16-bit reload timer**
  1 channel (8-bit × 2-channel, 16-bit × 1-channel mode switching function provided)
- **16-bit input-output timer**
  2-channel input capture, 6-channel output compare, 1-channel free run timer
- **2 built-in clock generator systems**
- **Low power modes**
  Stop, sleep, CPU intermittent mode, watch mode, etc.
- **Package options**
  QFP100/LQFP100
- **Process**
  CMOS technology
- **Supply voltage**
  Can operate on 3 V single supply systems (with 5 V interface provided by some pins with 3/5 V dual-supply capability)

■ PRODUCT LINEUP

Parameter \ Part number		MB90F474L	MB90F474H	MB90473	MB90474
ROM capacity		FLASH 256 KB	FLASH 256 KB	MASKROM 128 KB	MASKROM 256 KB
RAM capacity		16 KB	16 KB	10 KB	16 KB
CPU functions		Basic instructions : 351 Instruction bit length : 8-bit, 16-bit Instruction length : 1 byte to 7 bytes Data bit length : 1-bit, 8-bit, 16-bit Minimum instruction execution time : 62.5 ns (with 16 MHz machine clock)			
Ports		General purpose input/output ports : 84 Max General purpose input/output ports (CMOS output) General purpose input/output ports (built-in pull-up resistance) General purpose input/output ports (N-ch open drain)			
UART		Stop-start synchronized : 1 channel			
8/16-bit PPG timer		8-bit 6-channel/16-bit 3-channel			
8/16-bit up-down counter/timer		Two 8-bit up-down counters with 6 event input pins Two 8-bit reload/compare registers			
16-bit input/output timers	16-bit free-run timer	Channel : 1 Overflow interrupt			
	Output compare (OCU)	Channels : 6 Pin input source : from compare register match signal			
	Input capture (ICU)	Channels : 2 Register rewritten from pin input (rising/falling/both edges)			
DTP/external interrupt circuit		External interrupt pins : 8 channels (set to edge or level correlation)			
I/O expansion serial interface		2-channel, built-in			
I^2C interface		1-channel, built-in			
Time base timer		18-bit counter Interrupt cycle : 1.0 ms, 4.1 ms, 16.4 ms, 131.1 ms (minimum times, at base oscillator frequency 4 MHz)			
A/D converter		Conversion accuracy : 8/10-bit switchable Single conversion mode (converts selected channel 1 time only) Scan conversion mode (converts multiple consecutive channels, programmable up to 8 channels) Continuous conversion mode (converts selected channels continuously) Stop conversion mode (converts selected channel, stops and repeats)			
Watchdog timer		Reset interval : 3.58 ms, 14.33 ms, 57.23 ms, 458.75 ms (minimum times, at base oscillator frequency 4 MHz)			
Low power (standby) modes		Sleep, stop, CPU intermittent, watch mode			
Process		CMOS			
Notes		Flash model, low voltage version (f = 10 MHz or less at V_{CC} = 2.4 V)	Flash model, high voltage version (f = 20 MHz)	Mask version	Mask version
Emulator dedicated power supply		—	—	—	—

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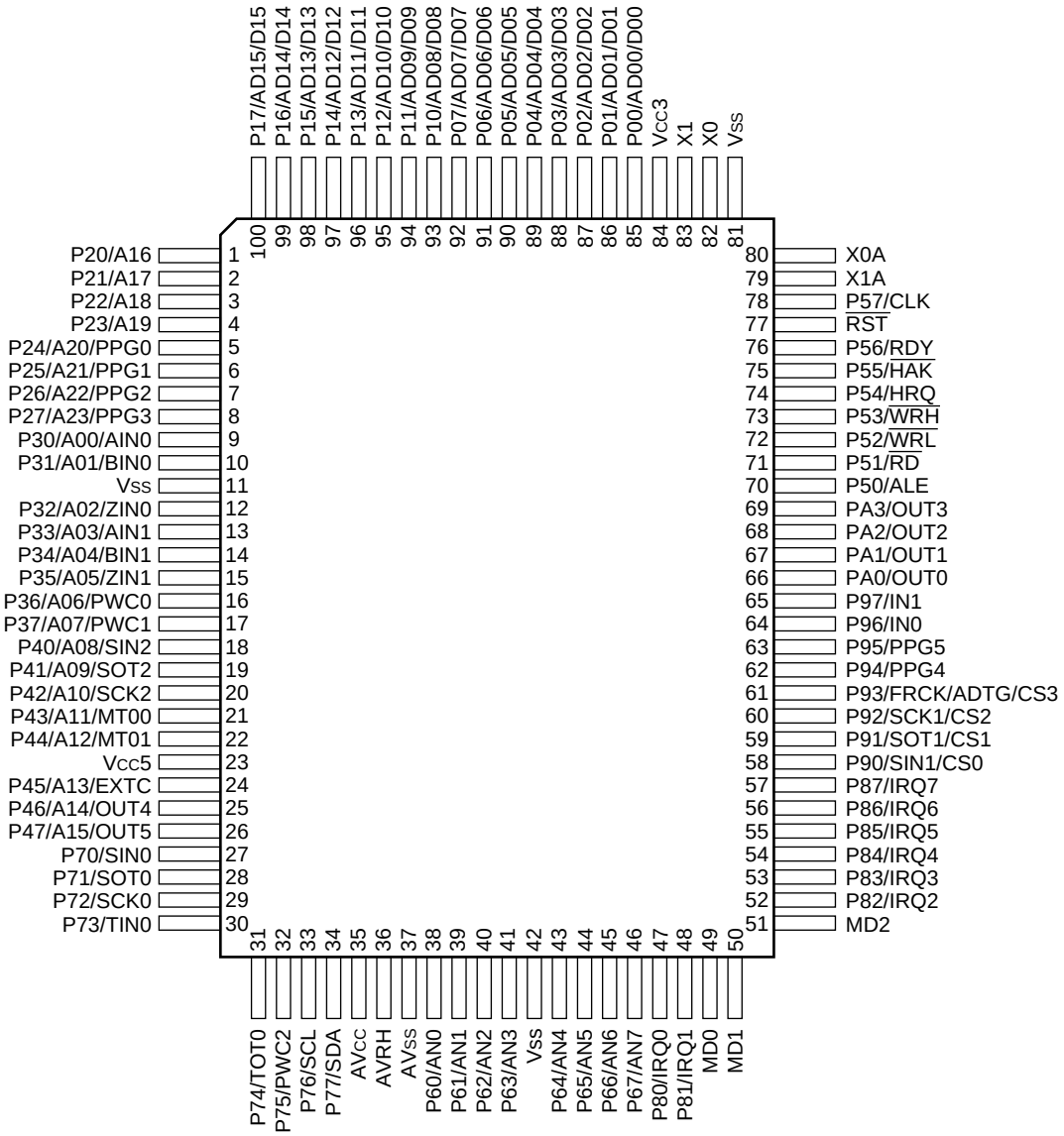
Parameter \ Part number		MB90477	MB90478	MB90V470B
ROM capacity		MASKROM 256 KB	MASKROM 256 KB	—
RAM capacity		8 KB	8 KB	16 KB
CPU functions		Basic instructions : 351 Instruction bit length : 8-bit, 16-bit Instruction length : 1 byte to 7 bytes Data bit length : 1-bit, 8-bit, 16-bit Minimum instruction execution time : 50 ns (with 20 MHz machine clock)		
Ports		General purpose input/output ports : 84 Max General purpose input/output ports (CMOS output) General purpose input/output ports (built-in pull-up resistance) General purpose input/output ports (N-ch open drain)		
UART		Stop-start synchronized : 1 channel		
8/16-bit PPG timer		8-bit 6-channel/16-bit 3-channel		
8/16-bit up-down counter/timer		Two 8-bit up-down counters with 6 event input pins Two 8-bit reload/compare registers		
16-bit input/output timers	16-bit free-run timer	Channel : 1 Overflow interrupt		
	Output compare (OCU)	Channels : 6 Pin input source : from compare register match signal		
	Input capture (ICU)	Channels : 2 Register rewritten from pin input (rising/falling/both edges)		
DTP/external interrupt circuit		External interrupt pins : 8 channels (set to edge or level correlation)		
I/O expansion serial interface		2-channel, built-in		
I^2C interface		1-channel, built-in		
Time base timer		18-bit counter Interrupt cycle : 1.0 ms, 4.1 ms, 16.4 ms, 131.1 ms (minimum times, at base oscillator frequency 4 MHz)		
A/D converter		Conversion accuracy : 8/10-bit switchable Single conversion mode (converts selected channel 1 time only) Scan conversion mode (converts multiple consecutive channels, programmable up to 8 channels) Continuous conversion mode (converts selected channels continuously) Stop conversion mode (converts selected channel, stops and repeats)		
Watchdog timer		Reset interval : 3.58 ms, 14.33 ms, 57.23 ms, 458.75 ms (minimum times, at base oscillator frequency 4 MHz)		
Low power (standby) modes		Sleep, stop, CPU intermittent, watch mode		
Process		CMOS		
Notes		Mask version	Mask version without I^2C built-in interface	EVA function User pin
Emulator dedicated power supply		—	—	Included

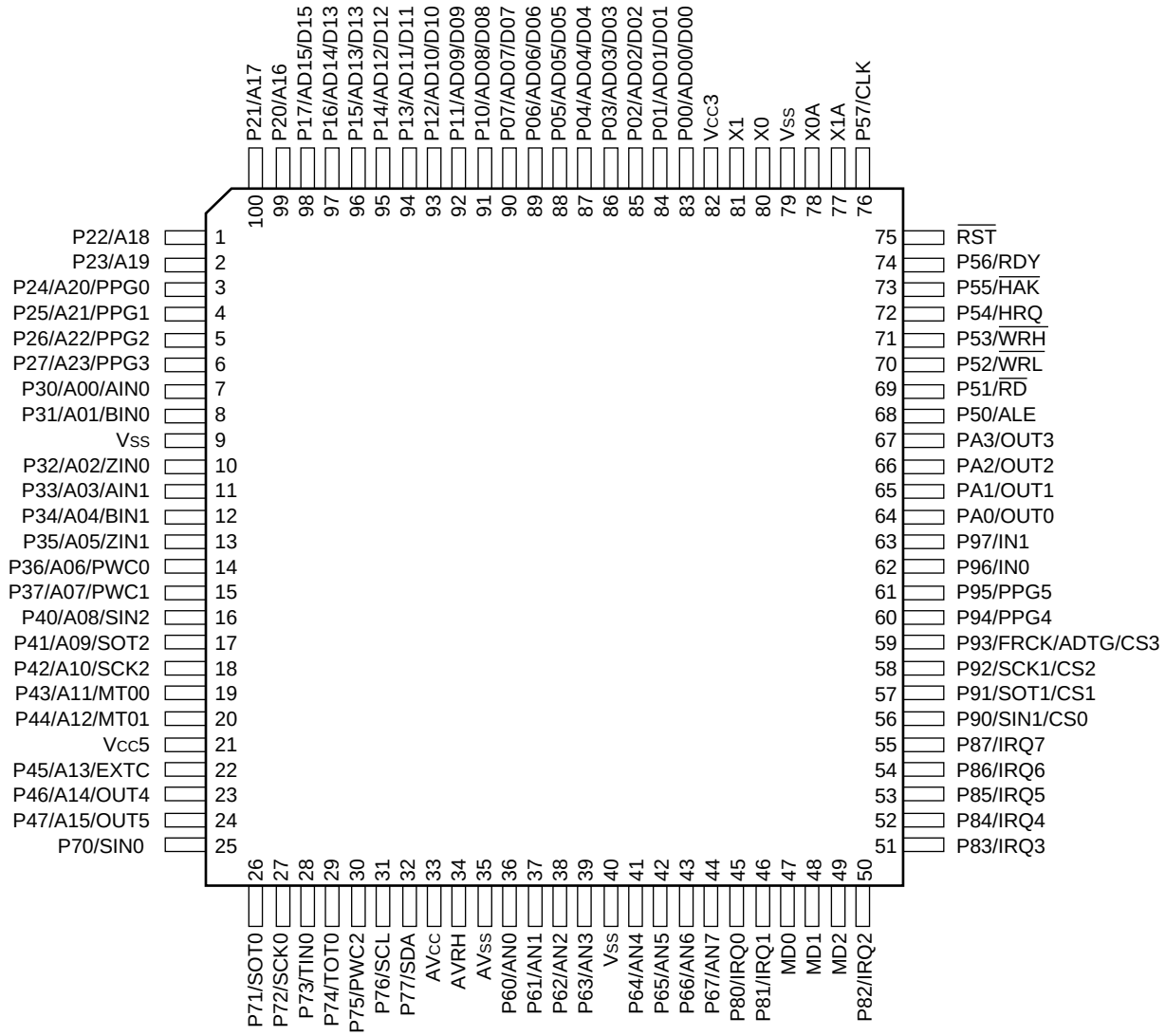
■ PIN ASSIGNMENTS

(TOP VIEW)



(FPT-100P-M06)

(TOP VIEW)



(FPT-100P-M05)

■ PIN DESCRIPTION

Pin no.		Pin name	Circuit type	Description
LQFP	QFP			
80	82	X0	A	Oscillator pin
81	83	X1	A	Oscillator pin
78	80	X0A	A	32 kHz oscillator pin
77	79	X1A	A	32 kHz oscillator pin
75	77	$\overline{\text{RST}}$	B	Reset input pin
83 to 90	85 to 92	P00 to P07	C (CMOS)	General purpose input/output ports. Set the pull-up resistance setting register (RDR0) to add pull-up resistance (RD00-RD07 = “1”) . (Not valid when set for output)
		AD00 to AD07		In multiplex mode, these pins function as external address/ data bus lower input/output pins.
		D00 to D07		In non-multiplex mode, these pins function as external data bus lower output pins.
91 to 98	93 to 100	P10 to P17	C (CMOS)	General purpose input/output ports. Set the pull-up resistance setting register (RDR1) to add pull-up resistance (RD10-RD17 = “1”) . (Not valid when set for output)
		AD08 to AD15		In multiplex mode, these pins function as external address/ data bus higher input/output pins.
		D08 to D15		In non-multiplex mode, these pins function as external data bus higher output pins.
99 100 1 2	1 to 4	P20 to P23	E (CMOS/H)	General purpose input/output ports. In external bus mode, pins for which the corresponding bit in the external address output control register (HACR) is “1” function as the general purpose input/output ports.
		A16 to A19		In multiplex mode, pins for which the corresponding bit in the external address output control register (HACR) is “0” function as the upper address output pins (A16 to A19) .
		A16 to A19		In non-multiplex mode, pins for which the corresponding bit in the external address output control register (HACR) is “0” function as the upper address output pins (A16 to A19) .
3 to 6	5 to 8	P24 to P27	E (CMOS/H)	General purpose input/output ports. In external bus mode, pins for which the corresponding bit in the external address output control register (HACR) is “1” function as the general purpose input/output ports.
		A20 to A23		In multiplex mode, pins for which the corresponding bit in the external address output control register (HACR) is “0” function as the upper address output pins (A20 to A23) .
		A20 to A23		In non-multiplex mode, pins for which the corresponding bit in the external address output control register (HACR) is “0” function as the upper address output pins (A20 to A23) .
		PPG0 to PPG3		PPG timer output pins.

(Continued)

LQFP : FPT-100P-M05 package
QFP : FPT-100P-M06 package

Pin no.		Pin name	Circuit type	Description
LQFP	QFP			
7	9	P30	E (CMOS/H)	General purpose input/output port.
		A00		In non-multibus bus mode, this pin functions as an external address pin.
		AIN0		8/16-bit up-down timer input pin. (ch0)
8	10	P31	E (CMOS/H)	General purpose input/output port.
		A01		In non-multibus bus mode, this pin functions as an external address pin.
		BIN0		8/16-bit up-down timer input pin. (ch0)
10	12	P32	E (CMOS/H)	General purpose input/output port.
		A02		In non-multibus bus mode, this pin functions as an external address pin.
		ZIN0		8/16-bit up-down timer input pin. (ch0)
11	13	P33	E (CMOS/H)	General purpose input/output port.
		A03		In non-multibus bus mode, this pin functions as an external address pin.
		AIN1		8/16-bit up-down timer input pin. (ch1)
12	14	P34	E (CMOS/H)	General purpose input/output port.
		A04		In non-multibus bus mode, this pin functions as an external address pin.
		BIN1		8/16-bit up-down timer input pin. (ch1)
13	15	P35	E (CMOS/H)	General purpose input/output port.
		A05		In non-multibus bus mode, this pin functions as an external address pin.
		ZIN1		8/16-bit up-down timer input pin. (ch1)
14 15	16 17	P36, P37	E (CMOS/H)	General purpose input/output ports.
		A06, A07		In non-multibus bus mode, this pin functions as an external address pin.
		PWC0, PWC1		Functions as PWC input pin.
16	18	P40	G (CMOS/H)	General purpose input/output port.
		A08		In non-multibus bus mode, this pin functions as an external address pin.
		SIN2		Single serial I/O input pin
17	19	P41	F (CMOS)	General purpose input/output port.
		A09		In non-multibus bus mode, this pin functions as an external address pin.
		SOT2		Single serial I/O output pin

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LQFP : FPT-100P-M05 package
QFP : FPT-100P-M06 package

Pin no.		Pin name	Circuit type	Description
LQFP	QFP			
18	20	P42	G (CMOS/H)	General purpose input/output port.
		A10		In non-multibus bus mode, this pin functions as an external address pin.
		SCK2		Single serial I/O clock input/output pin
19 20	21 22	P43, P44	F (CMOS)	General purpose input/output ports.
		A11, A12		In non-multibus bus mode, this pin functions as an external address pin.
		MT00, MT01		µPG input pins
22	24	P45	G (CMOS/H)	General purpose input/output ports.
		A13		In non-multibus bus mode, this pin functions as an external address pin.
		EXTC		µPG input pin
23 24	25 26	P46, P47	F (CMOS)	General purpose input/output ports.
		A14, A15		In non-multibus bus mode, this pin functions as an external address pin.
		OUT4/OUT5		Output compare event output pins
68	70	P50	D (CMOS)	General purpose input/output port. In external bus mode, this pin functions as the ALE pin
		ALE		In external bus mode, this pin functions as the address load enable signal (ALE) pin
69	71	P51	D (CMOS)	General purpose input/output port. In external bus mode, this pin functions as the $\overline{RD}$ pin.
		$\overline{RD}$		In external bus mode, this pin functions as the read strobe output ($\overline{RD}$) pin.
70	72	P52	D (CMOS)	General purpose input/output port. In external bus mode, this pin functions as the $\overline{WRL}$ pin when the WRE bit in the EPCR register is set to “1”.
		$\overline{WRL}$		In external bus mode, this pin functions as the lower data write strobe output ($\overline{WRL}$) pin. When the WRE bit in the EPCR register is set to “0”,this pin functions as a general purpose input/output port.
71	73	P53	D (CMOS)	General purpose input/output port. In external bus mode with 16-bit bus width, this pin functions as the $\overline{WRH}$ pin when the WRE bit in the EPCR register is set to “1”.
		$\overline{WRH}$		In external bus mode with 16-bit bus width, this pin functions as the higher data write strobe output ($\overline{WRH}$) pin. When the WRE bit in the EPCR register is set to “0”,this pin functions as a general purpose input/output port.

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LQFP : FPT-100P-M05 package
QFP : FPT-100P-M06 package

Pin no.		Pin name	Circuit type	Description
LQFP	QFP			
72	74	P54	D (CMOS)	General purpose input/output port. In external bus mode, this pin functions as the HRQ pin when the HDE bit in the EPCR register is set to “1”.
		HRQ		In external bus mode, this pin functions as the hold request input (HRQ) pin. When the HDE bit in the EPCR register is set to “0”,this pin functions as a general purpose input/output port.
73	75	P55	D (CMOS)	General purpose input/output port. In external bus mode, this pin functions as the $\overline{\text{HAK}}$ pin when the HDE bit in the EPCR register is set to “1”.
		$\overline{\text{HAK}}$		In external bus mode, this pin functions as the hold acknowledge output ($\overline{\text{HAK}}$) pin. When the HDE bit in the EPCR register is set to “0”,this pin functions as a general purpose input/output port.
74	76	P56	D (CMOS)	General purpose input/output port. In external bus mode, this pin functions as the DRY pin when the RYE bit in the EPCR register is set to “1”.
		RDY		In external bus mode, this pin functions as the external ready input (RDY) pin. When the RYE bit in the EPCR register is set to “0”,this pin functions as a general purpose input/output port.
76	78	P57	D (CMOS)	General purpose input/output port. In external bus mode, this pin functions as the CLK pin when the CKE bit in the EPCR register is set to “1”.
		CLK		In external bus mode, this pin functions as the machine cycle clock output (CLK) pin. When the CKE bit in the EPCR register is set to “0”,this pin functions as a general purpose input/output port.
36 to 39	38 to 41	P60 to P63	H (CMOS)	General purpose input/output ports.
		AN0 to AN3		Analog input pins.
41 to 44	43 to 46	P64 to P67	H (CMOS)	General purpose input/output ports.
		AN4 to AN7		Analog input pins.
25	27	P70	G (CMOS/H)	General purpose input/output port.
		SIN0		UART data input pin.
26	28	P71	F (CMOS)	General purpose input/output port.
		SOT0		UART data output pin.
27	29	P72	G (CMOS/H)	General purpose input/output port.
		SCK0		UART clock input pin.
28	30	P73	G (CMOS/H)	General purpose input/output port.
		TIN0		16-bit reload timer event input pin.
29	31	P74	F (CMOS)	General purpose input/output port.
		TOT0		16-bit reload timer output pin.

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LQFP : FPT-100P-M05 package
QFP : FPT-100P-M06 package

Pin no.		Pin name	Circuit type	Description
LQFP	QFP			
30	32	P75	G (CMOS/H)	General purpose input/output port.
		PWC2		PWC input pin.
31	33	P76	I (NMOS/H)	General purpose input/output port.
		SCL		I^2C interface data input/output pin. During I^2C interface operation, the port output should be set to High-Z level.
32	34	P77	I (NMOS/H)	General purpose input/output port.
		SDA		I^2C interface clock input/output pin. During I^2C interface operation, the port output should be set to High-Z level.
45 46	47 48	P80, P81	E (CMOS/H)	General purpose input/output ports.
		IRQ0, IRQ1		External interrupt input pins.
50 to 55	52 to 57	P82 to P87	E (CMOS/H)	General purpose input/output ports.
		IRQ2 to IRQ7		External interrupt input pins.
56	58	P90	E (CMOS/H)	General purpose input/output port.
		SIN1		Single serial I/O data input pin.
		CS0		Chip select 0.
57	59	P91	D (CMOS)	General purpose input/output port.
		SOT1		Single serial I/O data output pin.
		CS1		Chip select 1.
58	60	P92	E (CMOS/H)	General purpose input/output port.
		SCK1		Single serial I/O clock input/output pin.
		CS2		Chip select 2.
59	61	P93	E (CMOS/H)	General purpose input/output port.
		FRCK		In free run timer operation, this pin functions as the external clock input pin.
		ADTG		In A/D converter operation, this pin functions as the external trigger input pin.
		CS3		Chip select 3.
60	62	P94	D (CMOS)	General purpose input/output port.
		PPG4		PPG timer output pin.
61	63	P95	D (CMOS)	General purpose input/output port.
		PPG5		PPG timer output pin.
62	64	P96	E (CMOS/H)	General purpose input/output port.
		IN0		Functions as input capture ch 0 trigger input.

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LQFP : FPT-100P-M05 package
QFP : FPT-100P-M06 package

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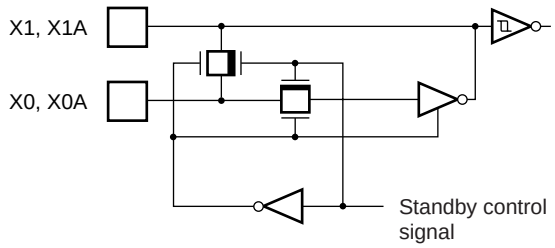
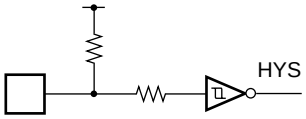
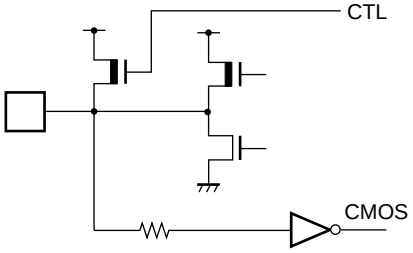
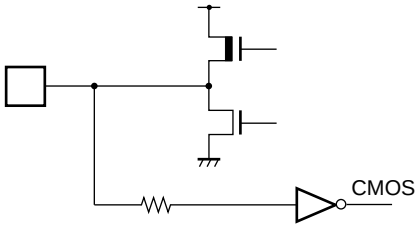
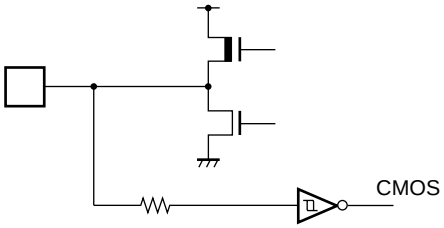
Pin no.		Pin name	Circuit type	Description
LQFP	QFP			
63	65	P97	E (CMOS/H)	General purpose input/output port.
		IN1		Functions as input capture ch 1 trigger input.
64 to 67	66 to 69	PA0 to PA3	D (CMOS)	General purpose input/output ports.
		OUT0 to OUT3		Output compare event output pins.
33	35	AV_{CC}	—	A/D converter power supply pin.
34	36	AVRH	—	A/D converter external reference power pin.
35	37	AV_{SS}	—	A/D converter power supply pin.
47 to 49	49 to 51	MD0 to MD2	J (CMOS/H)	Input pins for specifying operating mode.
82	84	$V_{CC}3$	—	3.3 V ± 0.3 V power supply pin ($V_{CC}3$) .
21	23	$V_{CC}5$	—	3.3 V ± 0.3 V/5.0 V ± 0.5 V dual power supply pin ($V_{CC}5$) .
9 40 79	11 42 81	V_{SS}	—	Power supply input pins (GND) .

LQFP : FPT-100P-M05 package
QFP : FPT-100P-M06 package

Notes :
- For use as a 3.3 V single supply device, apply the same voltage to the $V_{CC}3$ and $V_{CC}5$ power supply pins.
- For use with a dual power supply, apply the respective voltages to the $V_{CC}3$ and $V_{CC}5$ power supply pins.
- In use with a dual power supply, a total of 32 pins (P20/A16 to P27/A23/PPG3, P30/A00/AIN0 to P37/A07/PWC1, P40/A08/SIN2 to P47/A15/OUT5 and P70/SIN0 to P77/SDA) can be used in a 5 V interface. Note that all other pins must be used in 3 V interface.
- In use with a dual power supply, it is not possible to turn on only the 5 V or the 3 V power supply independently. Always turn on both power supplies simultaneously. (It is recommended that the 3 V power to the MB90470 series be turned on first.)

■ I/O CIRCUIT TYPES

Type	Circuit	Remarks
A		Oscillator feedback resistance : X1,X0 1 MΩ approx. X1A,X0A 10 MΩ approx. Includes standby control
B		Hysteresis with pull-up resistance Input resistance 50 kΩ approx.
C		Includes input pull-up resistance control CMOS level input/output Resistance : 50 kΩ approx.
D		CMOS level input/output
E		Hysteresis input CMOS level input/output

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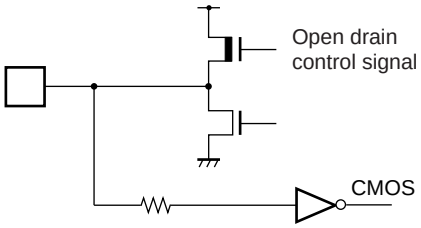
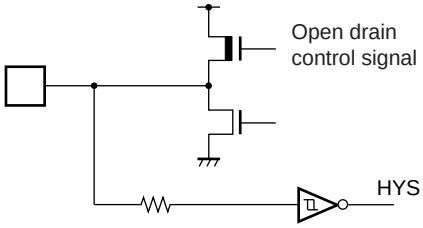
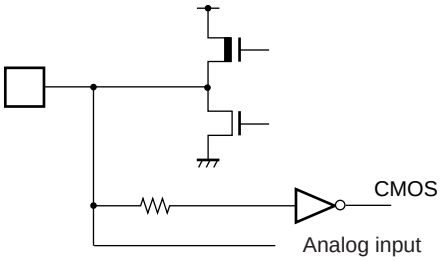
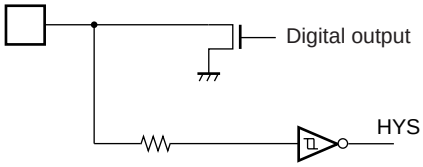
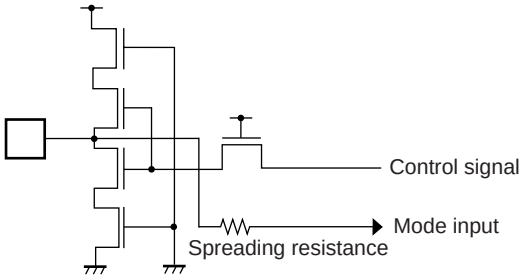
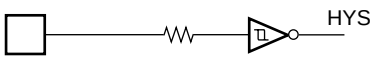
Type	Circuit	Remarks
F		CMOS level input/output Includes open drain control
G		CMOS level output Hysteresis input Includes open drain control
H		CMOS level input/output Analog input
I		Hysteresis input N-ch open drain output
J	(Flash model) 	Flash model CMOS level input Includes high voltage control for FLASH test
	(Mask version) 	Mask version Hysteresis input port

■ HANDLING DEVICES

(1) Strictly observe maximum rated voltages (prevent latchup)

When CMOS integrated circuit devices are subjected to applied voltages higher than V_{CC} at input and output pins other than medium- and high-withstand voltage pins, or to voltages lower than V_{SS}, or when voltages in excess of rated levels are applied between V_{CC} and V_{SS}, a phenomenon known as latchup can occur. In a latchup condition, supply current can increase dramatically and may destroy semiconductor elements. In using semiconductor devices, always take sufficient care to avoid exceeding maximum ratings.

Also care must be taken when power to analog systems is switched on or off, to ensure that the analog power supply (AV_{CC}, AVRH) and analog input do not exceed the digital power supply (V_{CC}) .

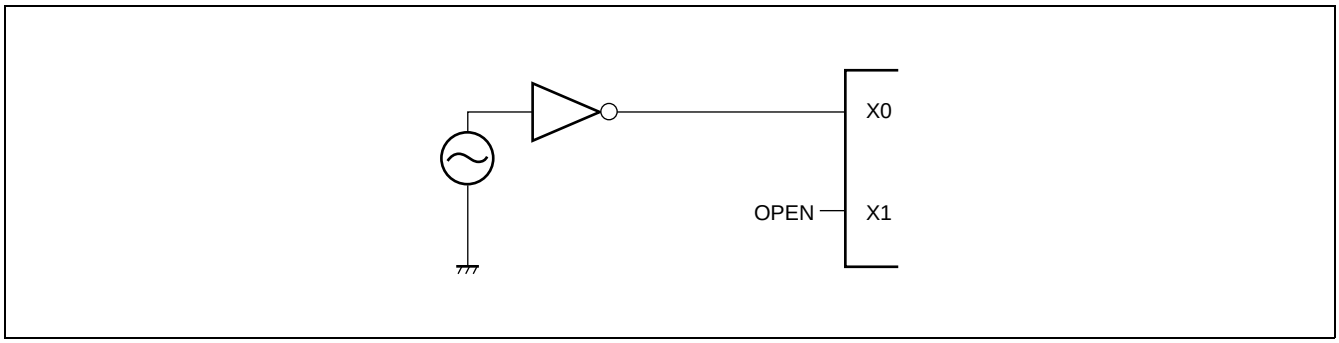
(2) Treatment of unused pins

If unused input pins are left open, abnormal operation or latchup may cause permanent damage to the semiconductor. Any such pins should be pulled up or pulled down through resistance of at least 2 kΩ.

Also any unused input/output pins should be left open in output status, or if set to input status should be treated in the same way as input pins.

(3) Precautions for use of external clock signals

Even when an external clock is used, a stabilization period is required following a power-on reset or release from sub clock mode or stop mode. Also, when an external clock is used 20 MHz should be used as a guideline for an upper frequency limit.
The following figure shows a sample use of external clock signals.



(4) Power supply pins

When using multiple V_{CC}/V_{SS} sources, always make sure to design devices with external connections of all power supply pins to supply or ground elements, in order to prevent latchup, reduce unwanted radiation, and prevent abnormal strobe signal operation due to rise in ground level, as well as to maintain total rated output current. In addition, care must be given to connecting the V_{CC} and V_{SS} pins of this device to a current source with as little impedance as possible. It is recommended that a bypass capacitor of 1.0 μF be connected between V_{CC} and V_{SS} as close to the pins as possible.

(5) Crystal oscillator circuits

Abnormal operation of this device can result from noise in the proximity of the X0/X1 and X0A/X1A pins. For stable operation, it is strongly recommended that the printed circuit artwork provide capacitors placed as close as possible between the X0/X1, X0A/X1A and crystal oscillator (or ceramic oscillator) as well as ground, and be wired so as to avoid crossing other wiring wherever possible.

(6) Precautions for use of external oscillators (crystals)

The target value for the upper limit of oscillator (crystals) frequencies should be 20 MHz. Also, when operating at internal frequencies of 16 MHz, the PLL multiplier should be used.

(7) Proper power-on/off sequence

The A/D converter power (AV_{CC}, AVRH) and analog input (AN0 to AN7) must be turned on after the digital power supply (V_{CC}) is turned on. The A/D converter power (AV_{CC}, AVRH) and analog input (AN0 to AN7) must be shut off before the digital power supply (V_{CC}) is shut off. Care should be taken that AVRH does not exceed AV_{CC}. Even when pins used as analog input pins are doubled as input ports, be sure that the input voltage does not exceed AV_{CC}.

Note : $V_{CC} = V_{CC}3 = V_{CC}5$

(8) Treatment of A/D converter power supply pins

Even if the A/D converter is not used, pins should be connected so that AV_{CC} = AVRH = V_{CC}, and AV_{SS} = V_{SS}.

(9) Power-on procedures

In order to prevent abnormal operation of the internal built-in step-down circuits, voltage rise during power-on should be attained within 50 µs (0.2 V to 2.7 V) .

(10) Stable power supply

Even within the operating range of the V_{CC} supply voltage, rapid changes in supply voltage may cause abnormal operation. As a basis for stable operation, it is recommended that voltage variation be restricted in order to limit V_{CC} ripple fluctuations (P-P values) to 10% at commercial frequencies of 50 Hz to 60 Hz, and transient fluctuations to 0.1 V/ms at instantaneous points such as power switching.

(11) Precautions for use of two power supplies

The MB90470 series usually uses the 3-V power supply as the main power source. With $V_{CC}3$ = 3 V and $V_{CC}5$ = 5 V, however, it can interface with P20/A16 to P27/A23/PPG3, P30/A00/AIN0 to P37/A07/PWC1, P40/A08/SIN2 to P47/A15/OUT5, P70/SIN0 to P77/SDA for the 5-V power supply separetely from the 3-V power supply at all operation mode.

(Caution) The analog power supply for the A/D converter (AV_{CC}, AV_{SS} etc.) can only operate with the 3 V system.

(12) Crystal oscillator circuits during power-saving operation

When the power supply is lower than 2.0 V, the external crystal oscillator may not operate even when power is on. For this reason, the use of an external clock signal is recommended.

(13) Caution : low-voltage flash models (2.4 V to 3.6 V/10 MHz) do not have security functions

(14) Treatment of unused input pins

N.C. (internally connected) pins should always be left open.

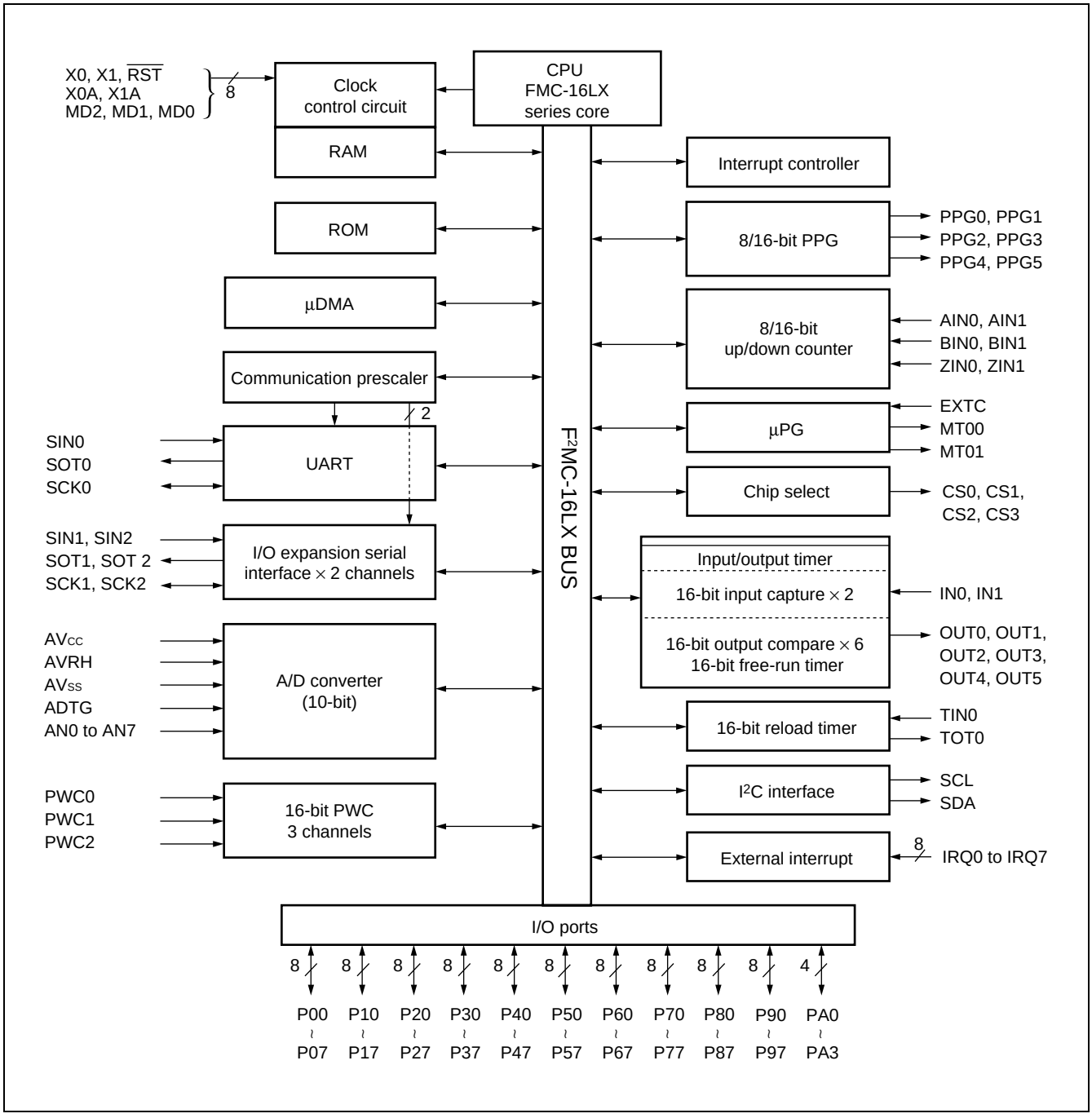
(15) When the dual-supply MB90470 series is used as a 1-supply device, use connections so that X0A = V_{SS}, and X1A = Open.

(16) For serial writing to flash memory, always make sure that the operating voltage V_{CC} is between 3.13 V and 3.6 V.
For normal writing to flash memory, always make sure that the operating voltage V_{CC} is between 3.0 V and 3.6 V.

(17) Caution on Operations during PLL Clock Mode

If the PLL clock mode is selected, the microcontroller attempt to be working with the self-oscillating circuit even when there is no external oscillator or external clock input is stopped. Performance of this operation, however, cannot be guaranteed.

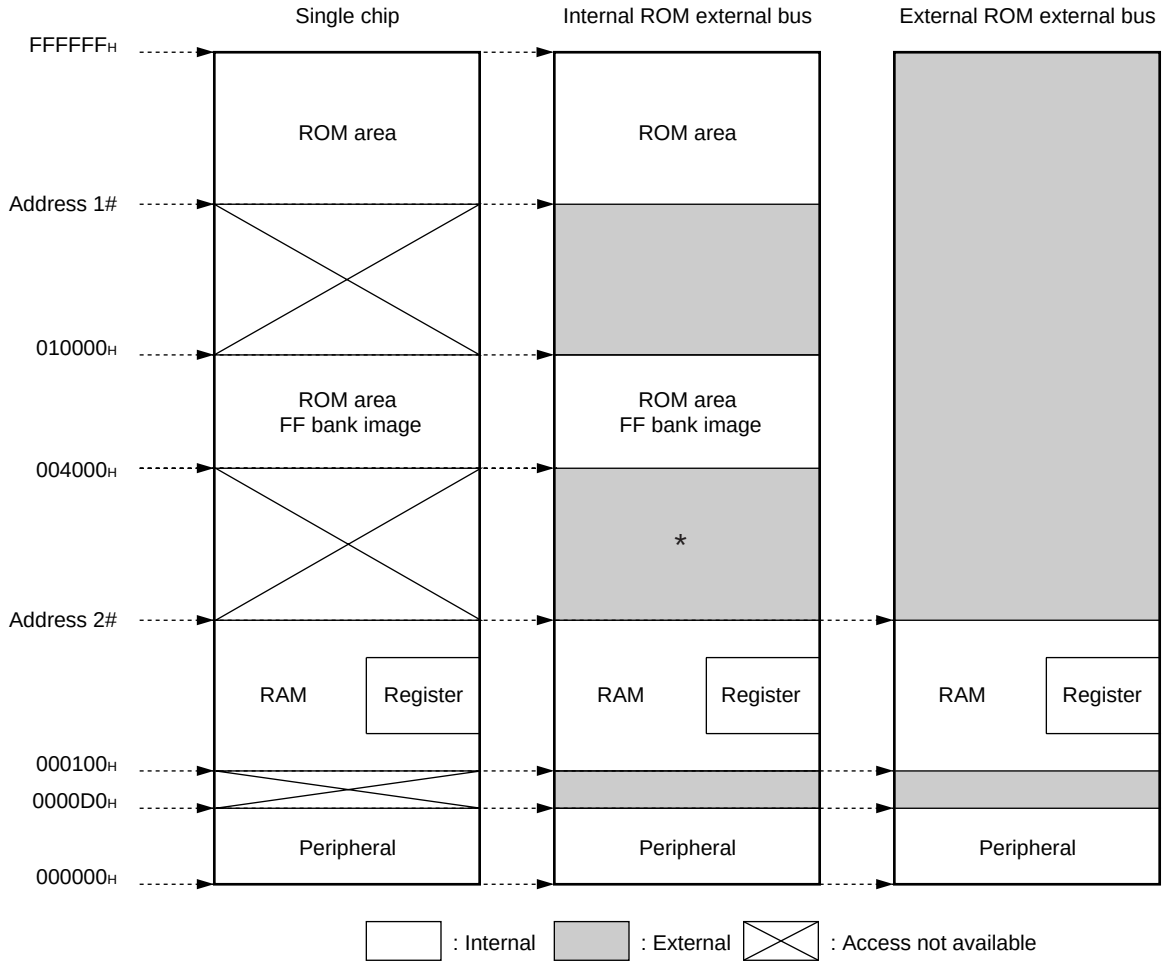
■ BLOCK DIAGRAM



P00 to P07 (8 pins) : Input pull-up resistance setting register provided.
P10 to P17 (8 pins) : Input pull-up resistance setting register provided.
P40 to P47 (8 pins) : Open drain setting register provided.
P70 to P75 (6 pins) : Open drain setting register provided.
P76, P77 (2 pins) : Open drain

Note : In the above diagram, I/O ports are shown sharing pin numbers with the built-in function blocks. However pins may not be used as I/O ports when they are in use as pins for build-in function modules.

■ MEMORY MAP



* : In models where address 2# coincides with 004000H, there is no external area.

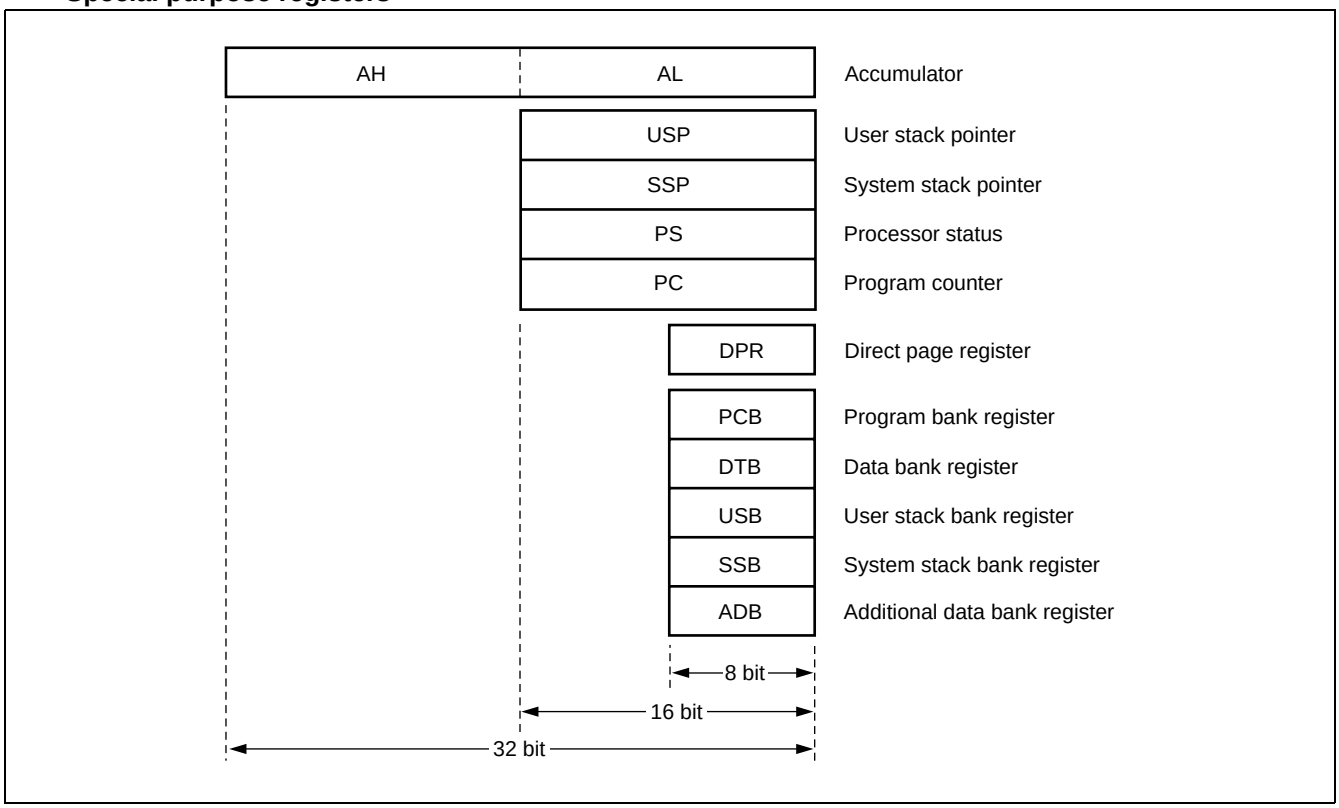
Model	Address 1#	Address 2#
MB90473	FE0000H	002900H
MB90474	FC0000H	004000H
MB90477/478	FC0000H	002100H
MB90F474	FC0000H	004000H
MB90V470	(FC0000H)	004000H

The image of FF bank ROM is reflected in the top of the 00 bank, for greater efficiency in using the C compiler for small models. The lower 16-bit address on the FF bank is the same as the lower 16-bit address on the 00 bank, so that it is possible to reference tables in ROM without using the pointer for a far specification.

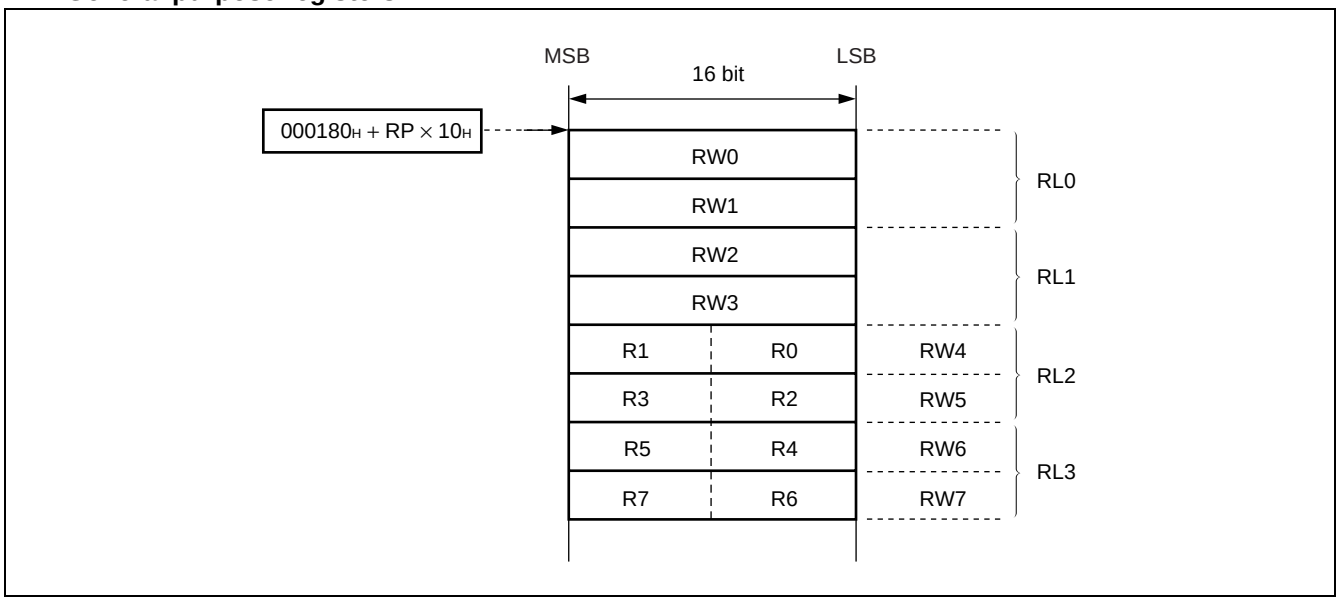
For example, when accessing 00C000H, it is actually the content of ROM at FFC000H that is accessed. Here, because the ROM area on the FF bank exceeds 48 KB, it is not possible to view the entire area in the image on the 00 bank. Therefore, the image from FF4000H to FFFFFFH is visible on the 00 bank, and FF0000H to FF3FFFH is visible only on the FF bank.

■ F²MC-16L CPU PROGRAMMING MODEL

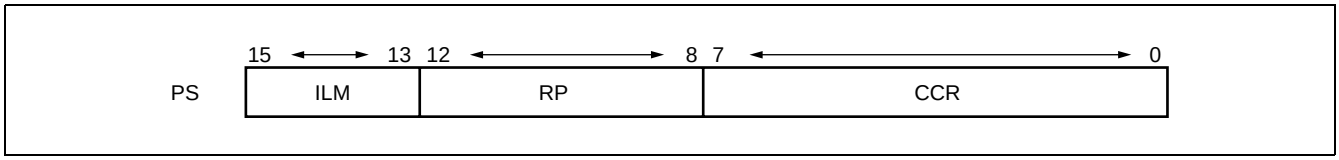
- **Special purpose registers**



- **General purpose registers**



- **Processor status**



■ I/O MAP

Address	Register name	Symbol	Access	Resource name	Default
00H	Port 0 data register	PDR0	R/W	Port 0	XXXXXXXX
01H	Port 1 data register	PDR1	R/W	Port 1	XXXXXXXX
02H	Port 2 data register	PDR2	R/W	Port 2	XXXXXXXX
03H	Port 3 data register	PDR3	R/W	Port 3	XXXXXXXX
04H	Port 4 data register	PDR4	R/W	Port 4	XXXXXXXX
05H	Port 5 data register	PDR5	R/W	Port 5	XXXXXXXX
06H	Port 6 data register	PDR6	R/W	Port 6	XXXXXXXX
07H	Port 7 data register	PDR7	R/W	Port 7	1 1XXXXXX
08H	Port 8 data register	PDR8	R/W	Port 8	XXXXXXXX
09H	Port 9 data register	PDR9	R/W	Port 9	XXXXXXXX
0AH	Port A data register	PDRA	R/W	Port A	- - - - XXXX
0BH	Port 3 timer input enable register	UDRE	R/W	Up/down timer input control	XX 0 0 0 0 0 0
0CH	Interrupt/DTP enable register	ENIR	R/W	DTP/external interrupt	0 0 0 0 0 0 0 0
0DH	Interrupt/DTP enable register	EIRR	R/W		0 0 0 0 0 0 0 0
0EH	Demand level setting register	ELVR	R/W		0 0 0 0 0 0 0 0
0FH	Demand level setting register		R/W		0 0 0 0 0 0 0 0
10H	Port 0 direction register	DDR0	R/W	Port 0	0 0 0 0 0 0 0 0
11H	Port 1 direction register	DDR1	R/W	Port 1	0 0 0 0 0 0 0 0
12H	Port 2 direction register	DDR2	R/W	Port 2	0 0 0 0 0 0 0 0
13H	Port 3 direction register	DDR3	R/W	Port 3	0 0 0 0 0 0 0 0
14H	Port 4 direction register	DDR4	R/W	Port 4	0 0 0 0 0 0 0 0
15H	Port 5 direction register	DDR5	R/W	Port 5	0 0 0 0 0 0 0 0
16H	Port 6 direction register	DDR6	R/W	Port 6	0 0 0 0 0 0 0 0
17H	Port 7 direction register	DDR7	R/W	Port 7	- - 0 0 0 0 0 0
18H	Port 8 direction register	DDR8	R/W	Port 8	0 0 0 0 0 0 0 0
19H	Port 9 direction register	DDR9	R/W	Port 9	0 0 0 0 0 0 0 0
1AH	Port A direction register	DDRA	R/W	Port A	- - - - 0 0 0 0
1BH	Port 4 pin register	ODR4	R/W	Port 4 (OD control)	0 0 0 0 0 0 0 0
1CH	Port 0 resistance register	RDR0	R/W	Port 0 (pull-up)	0 0 0 0 0 0 0 0
1DH	Port 1 resistance register	RDR1	R/W	Port 1 (pull-up)	0 0 0 0 0 0 0 0
1EH	Port 7 pin register	ODR7	R/W	Port 7 (OD control)	- - 0 0 0 0 0 0
1FH	Analog input enable register	ADER	R/W	Port 5, A/D	1 1 1 1 1 1 1 1

(Continued)

Address	Register name	Symbol	Access	Resource name	Default
20H	Serial mode register 0	SMR0	R/W	UART0	0 0 0 0 0 X 0 0
21H	Serial control register 0	SCR0	R/W		0 0 0 0 0 1 0 0
22H	Serial input register/ serial output register	SIDR/ SODR0	R/W		XXXXXXXX
23H	Serial status register	SSR0	R/W		0 0 0 0 1 0 0 0
24H	Reserved				
25H	Clock divider control register	CDCR	R/W	Communication prescaler (UART)	0 0 - - 0 0 0 0
26H	Serial mode control status register 0	SMCS0	R/W	SCI1 (ch0)	- - - - 0 0 0 0
27H	Serial mode control status register 0	SMCS0	R/W		0 0 0 0 0 0 1 0
28H	Serial data register	SDR0	R/W		XXXXXXXX
29H	Clock divider control register	SDCR0	R/W	Communication prescaler (SCI0)	0 - - - 0 0 0 0
2AH	Serial mode control status register 1	SMCS1	R/W	SCI2 (ch1)	- - - - 0 0 0 0
2BH	Serial mode control status register 1	SMCS1	R/W		0 0 0 0 0 0 1 0
2CH	Serial data register	SDR1	R/W		XXXXXXXX
2DH	Clock divider control register	SDCR1	R/W	Communication prescaler (SCI1)	0 - - - 0 0 0 0
2EH	PPG reload register L (ch0)	PRLL0	R/W	8/16-bit PPG (ch0-ch5)	XXXXXXXX
2FH	PPG reload register H (ch0)	PRLH0	R/W		XXXXXXXX
30H	PPG reload register L (ch1)	PRLL1	R/W		XXXXXXXX
31H	PPG reload register H (ch1)	PRLH1	R/W		XXXXXXXX
32H	PPG reload register L (ch2)	PRLL2	R/W		XXXXXXXX
33H	PPG reload register H (ch2)	PRLH2	R/W		XXXXXXXX
34H	PPG reload register L (ch3)	PRLL3	R/W		XXXXXXXX
35H	PPG reload register H (ch3)	PRLH3	R/W		XXXXXXXX
36H	PPG reload register L (ch4)	PRLL4	R/W		XXXXXXXX
37H	PPG reload register H (ch4)	PRLH4	R/W		XXXXXXXX
38H	PPG reload register L (ch5)	PRLL5	R/W		XXXXXXXX
39H	PPG reload register H (ch5)	PRLH5	R/W		XXXXXXXX
3AH	PPG0 operating mode control register	PPGC0	R/W		0 X 0 0 0XX 1
3BH	PPG1 operating mode control register	PPGC1	R/W		0 X 0 0 0 0 0 1
3CH	PPG2 operating mode control register	PPGC2	R/W		0 X 0 0 0XX 1
3DH	PPG3 operating mode control register	PPGC3	R/W		0 X 0 0 0 0 0 1
3EH	PPG4 operating mode control register	PPGC4	R/W		0 X 0 0 0XX 1
3FH	PPG5 operating mode control register	PPGC5	R/W		0 X 0 0 0 0 0 1
40H	PPG0, 1 output control register	PPG01	R/W	8/16-bit PPG	0 0 0 0 0 0 0 0

(Continued)

Address	Register name	Symbol	Access	Resource name	Default
41H	Reserved				
42H	PPG2, 3 output control register	PPG23	R/W	8/16-bit PPG	0 0 0 0 0 0 0 0
43H	Reserved				
44H	PPG4, 5 output control register	PPG45	R/W	8/16-bit PPG	0 0 0 0 0 0 0 0
45H	Reserved				
46H	Control status register	ADCS1	R/W	A/D converter	0 0 0 0 0 0 0 0
47H		ADCS2	R/W		0 0 0 0 0 0 0 0
48H	Data register	ADCR1	R		XXXXXXXX
49H		ADCR2	R		0 0 0 0 0 XXX
4AH	Output compare register (ch0) low	OCCP0	R/W	16-bit output timer output compare (ch0-ch5)	XXXXXXXX
4BH	Output compare register (ch0) high				XXXXXXXX
4CH	Output compare register (ch1) low	OCCP1	R/W		XXXXXXXX
4DH	Output compare register (ch1) high				XXXXXXXX
4EH	Output compare register (ch2) low	OCCP2	R/W		XXXXXXXX
4FH	Output compare register (ch2) high				XXXXXXXX
50H	Output compare register (ch3) low	OCCP3	R/W		XXXXXXXX
51H	Output compare register (ch3) high				XXXXXXXX
52H	Output compare register (ch4) low	OCCP4	R/W		XXXXXXXX
53H	Output compare register (ch4) high				XXXXXXXX
54H	Output compare register (ch5) low	OCCP5	R/W		XXXXXXXX
55H	Output compare register (ch5) high				XXXXXXXX
56H	Output compare control register (ch0)	OCS0	R/W		0 0 0 0 - - 0 0
57H	Output compare control register (ch1)	OCS1	R/W		- - - 0 0 0 0 0
58H	Output compare control register (ch2)	OCS2	R/W		0 0 0 0 - - 0 0
59H	Output compare control register (ch3)	OCS3	R/W	—	- - - 0 0 0 0 0
5AH	Output compare control register (ch4)	OCS4	R/W	16-bit output timer OCU (ch4, 5)	0 0 0 0 - - 0 0
5BH	Output compare control register (ch5)	OCS5	R/W		- - - 0 0 0 0 0
5CH	Input capture register (ch0) low	IPCP0	R	16-bit output timer Input capture (ch0, 1)	XXXXXXXX
5DH	Input capture register (ch0) high		R		XXXXXXXX
5EH	Input capture register (ch1) low	IPCP1	R		XXXXXXXX
5FH	Input capture register (ch1) high		R		XXXXXXXX
60H	Input capture control register	ICS01	R/W		0 0 0 0 0 0 0 0
61H	Reserved				

(Continued)

Address	Register name	Symbol	Access	Resource name	Default
62H	Timer data register low	TCDT	R/W	16-bit output timer Free run timer	0 0 0 0 0 0 0 0
63H	Timer data register high	TCDT	R/W		0 0 0 0 0 0 0 0
64H	Timer control status register	TCCS	R/W		0 0 0 0 0 0 0 0
65H	Timer control status register	TCCS	R/W		0 - - 0 0 0 0 0
66H	Compare clear register low	CPCLR	R/W		XXXXXXXX
67H	Compare clear register high				XXXXXXXX
68H	Up down count register ch0	UDCR0	R	8/16-bit up-down timer-counter	0 0 0 0 0 0 0 0
69H	Up down count register ch1	UDCR1	R		0 0 0 0 0 0 0 0
6AH	Reload compare register ch0	RCR0	W		0 0 0 0 0 0 0 0
6BH	Reload compare register ch1	RCR1	W		0 0 0 0 0 0 0 0
6CH	Counter control register low ch0	CCRL0	R/W		0 X 0 0 X 0 0 0
6DH	Counter control register high ch0	CCRH0	R/W		0 0 0 0 0 0 0 0
6EH	Reserved				
6FH	ROM mirror function select register	ROMM	W	ROM mirror function	- - - - - - - 1
70H	Counter control register low ch1	CCRL1	R/W	8/16-bit up-down timer-counter	0 X 0 0 X 0 0 0
71H	Counter control register high ch1	CCRH1	R/W		- 0 0 0 0 0 0 0
72H	Count status register ch0	CSR0	R/W		0 0 0 0 0 0 0 0
73H	Reserved				
74H	Count status register ch1	CSR1	R/W	8/16-bit UDC	0 0 0 0 0 0 0 0
75H	Reserved				
76H	PWC0 control status register	PWCSR0	R/W	16-bit PWC timer (ch0)	0 0 0 0 0 0 0 0
77H					0 0 0 0 0 0 0 X
78H	PWC0 data buffer register	PWCR0	R/W		0 0 0 0 0 0 0 0
79H					0 0 0 0 0 0 0 0
7AH	PWC1 control status register	PWCSR1	R/W	16-bit PWC timer (ch1)	0 0 0 0 0 0 0 0
7BH					0 0 0 0 0 0 0 X
7CH	PWC1 data buffer register	PWCR1	R/W		0 0 0 0 0 0 0 0
7DH					0 0 0 0 0 0 0 0
7EH	PWC2 control status register	PWCSR2	R/W	16-bit PWC timer (ch2)	0 0 0 0 0 0 0 0
7FH					0 0 0 0 0 0 0 X
80H	PWC2 data buffer register	PWCR2	R/W		0 0 0 0 0 0 0 0
81H					0 0 0 0 0 0 0 0
82H	PWC0 division ratio register	DIVR0	R/W	PWC (ch0)	- - - - - - 0 0
83H	Reserved				
84H	PWC1 division ratio register	DIVR1	R/W	PWC (ch1)	- - - - - - 0 0
85H	Reserved				

(Continued)

Address	Register name	Symbol	Access	Resource name	Default
86H	PWC2 division ratio register	DIVR2	R/W	PWC (ch2)	- - - - - - 0 0
87H	Reserved				
88H	I²C bus status register	IBSR	R	I²C functions	0 0 0 0 0 0 0 0
89H	I²C bus control register	IBCR	R/W		0 0 0 0 0 0 0 0
8AH	I²C bus clock select register	ICCR	R/W		- - 0XXXXX
8BH	I²C bus address register	IADR	R/W		- XXXXXXX
8CH	I²C bus data register	IDAR	R/W		XXXXXXXX
8DH	Reserved				
8EH	µPG control register	PGCSR	R/W	µPG	0 0 0 0 0 - - -
8FH to 9BH	Prohibited				
9CH	µDMA status register	DSRL	R/W	µDMA	0 0 0 0 0 0 0 0
9DH	µDMA status register	DSRH	R/W	µDMA	0 0 0 0 0 0 0 0
9EH	Program address detection control status resister	PACSR	R/W	Address Match Detection Function	0 0 0 0 0 0 0 0
9FH	Delay interrupt source generate/ release register	DIRR	R/W	Delay interrupt generator module	- - - - - - - - 0
A0H	Low power mode register	LPMCR	R/W	Low power modes	0 0 0 1 1 0 0 0
A1H	Clock select register	CKSCR	R/W	Low power modes	1 1 1 1 1 1 0 0
A2H, A3H	Reserved				
A4H	µDMA stop status register	DSSR	R/W	µDMA	0 0 0 0 0 0 0 0
A5H	Auto ready function select register	ARSR	W	External pins	0 0 1 1 - - 0 0
A6H	External address output control register	HACR	W	External pins	0 0 0 0 0 0 0 0
A7H	Bus control signal control register	EPCR	W	External pins	1 0 0 0 * 1 0 -
A8H	Watchdog control register	WDTC	R/W	Watchdog timer	XXXXX 1 1 1
A9H	Time base timer control register	TBTC	R/W	Time base timer	1 X X 0 0 1 0 0
AAH	Watch timer control register	WTC	R/W	Watch timer	1 0 0 0 1 0 0 0
ABH	Reserved				
ACH	µDMA control register	DERL	R/W	µDMA	0 0 0 0 0 0 0 0
ADH	µDMA control register	DERH	R/W	µDMA	0 0 0 0 0 0 0 0
AEH	Flash memory control status register	FMCR	R/W	Flash memory interface	0 0 0 X 0 0 0 0
AFH	Prohibited				
B0H	Interrupt control register 00	ICR00	R/W	—	XXXX 0 1 1 1
B1H	Interrupt control register 01	ICR01	R/W	—	XXXX 0 1 1 1
B2H	Interrupt control register 02	ICR02	R/W	—	XXXX 0 1 1 1
B3H	Interrupt control register 03	ICR03	R/W	—	XXXX 0 1 1 1

(Continued)

Address	Register name	Symbol	Access	Resource name	Default
B4H	Interrupt control register 04	ICR04	R/W	—	XXXX 0 1 1 1
B5H	Interrupt control register 05	ICR05	R/W	—	XXXX 0 1 1 1
B6H	Interrupt control register 06	ICR06	R/W	—	XXXX 0 1 1 1
B7H	Interrupt control register 07	ICR07	R/W	—	XXXX 0 1 1 1
B8H	Interrupt control register 08	ICR08	R/W	—	XXXX 0 1 1 1
B9H	Interrupt control register 09	ICR09	R/W	—	XXXX 0 1 1 1
BAH	Interrupt control register 10	ICR10	R/W	—	XXXX 0 1 1 1
BBH	Interrupt control register 11	ICR11	R/W	—	XXXX 0 1 1 1
BCH	Interrupt control register 12	ICR12	R/W	—	XXXX 0 1 1 1
BDH	Interrupt control register 13	ICR13	R/W	—	XXXX 0 1 1 1
BEH	Interrupt control register 14	ICR14	R/W	—	XXXX 0 1 1 1
BFH	Interrupt control register 15	ICR15	R/W	—	XXXX 0 1 1 1
C0H	Chip select MASK register 0	CMR0	R/W	Chip select functions	0 0 0 0 1 1 1 1
C1H	Chip select area register 0	CAR0	R/W	—	1 1 1 1 1 1 1 1
C2H	Chip select MASK register 1	CMR1	R/W	—	0 0 0 0 1 1 1 1
C3H	Chip select area register 1	CAR1	R/W	—	1 1 1 1 1 1 1 1
C4H	Chip select MASK register 2	CMR2	R/W	—	0 0 0 0 1 1 1 1
C5H	Chip select area register 2	CAR2	R/W	—	1 1 1 1 1 1 1 1
C6H	Chip select MASK register 3	CMR3	R/W	—	0 0 0 0 1 1 1 1
C7H	Chip select area register 3	CAR3	R/W	—	1 1 1 1 1 1 1 1
C8H	Chip select control register	CSCR	R/W	—	- - - - 0 0 0 *
C9H	Chip select control active level register	CALR	R/W	—	- - - - 0 0 0 0
CAH	Timer control status registers	TMCSR	R/W	16-bit reload timer	0 0 0 0 0 0 0 0
CBH					- - - - 0 0 0 0
CCH	16-bit timer register 16-bit reload register	TMR/ TMRLR	R/W		XXXXXXXX
CDH					
CEH, CFH	Reserved				
D0H to FFH	External area				
100H to #H	RAM area				
1FF0	Program address detection resister0 (Low order address)	PADR0	R/W	Address Match Detection Function	XXXXXXXX
1FF1	Program address detection resister0 (Middle order address)				
1FF2	Program address detection resister0 (High order address)				

(Continued)

(Continued)

Address	Register name	Symbol	Access	Resource name	Default
1FF3	Program address detection resister1 (Low order address)	PADR1	R/W	Address Match Detection Function	XXXXXXXX
1FF4	Program address detection resister1 (Middle order address)				
1FF5	Program address detection resister1 (High order address)				

Interrupt symbols :
R/W : Read/write enabled
R : Read only
W : Write only

Default value symbols :
0 : This bit initialized to “0”
1 : This bit initialized to “1”
* : This bit initialized to “0” or “1”
X : Default value undefined
- : This bit is not used.

■ INTERRUPT SOURCES, INTERRUPT VECTORS & INTERRUPT CONTROL REGISTERS

Interrupt source	EI²OS support	µDMA channel no.	Interrupt vector		Interrupt control register	
			No.	Address	No.	Address
Reset	—	—	#08	FFFFDC$_H$	—	—
INT9 instruction	—	—	#09	FFFFD8$_H$	—	—
Exception	—	—	#10	FFFFD4$_H$	—	—
INT0	○	0	#11	FFFFD0$_H$	ICR00	0000B0$_H$
INT1	○	×	#12	FFFFCC$_H$		
INT2	○	×	#13	FFFFC8$_H$	ICR01	0000B1$_H$
INT3	○	×	#14	FFFFC4$_H$		
INT4	○	×	#15	FFFFC0$_H$	ICR02	0000B2$_H$
INT5	○	×	#16	FFFFBC$_H$		
INT6	○	×	#17	FFFFB8$_H$	ICR03	0000B3$_H$
INT7	○	×	#18	FFFFB4$_H$		
PWC1	○	×	#19	FFFFB0$_H$	ICR04	0000B4$_H$
PWC2	○	×	#20	FFFFAC$_H$		
PWC0	○	1	#21	FFFFA8$_H$	ICR05	0000B5$_H$
PPG0/PPG1 counter borrow	○	2	#22	FFFFA4$_H$		
PPG2/PPG3 counter borrow	○	3	#23	FFFFA0$_H$	ICR06	0000B6$_H$
PPG4/PPG5 counter borrow	○	4	#24	FFFF9C$_H$		
8/16-bit up/down counter timer compare/ underflow /overflow/ amp down inversion (ch0, 1)	○	×	#25	FFFF98$_H$	ICR07	0000B7$_H$
Input capture (ch0) load	○	5	#26	FFFF94$_H$		
Input capture (ch1) load	○	6	#27	FFFF90$_H$	ICR08	0000B8$_H$
Output compare (ch0) match	○	8	#28	FFFF8C$_H$		
Output compare (ch1) match	○	9	#29	FFFF88$_H$	ICR09	0000B9$_H$
Output compare (ch2) match	○	10	#30	FFFF84$_H$		
Output compare (ch3) match	○	×	#31	FFFF80$_H$	ICR10	0000BA$_H$
Output compare (ch4) match	○	×	#32	FFFF7C$_H$		
Output compare (ch5) match	○	×	#33	FFFF78$_H$	ICR11	0000BB$_H$
UART send end	○	11	#34	FFFF74$_H$		
16-bit free run timer/ 16-bit reload timer overflow	○	12	#35	FFFF70$_H$	ICR12	0000BC$_H$
UART receive end	◎	7	#36	FFFF6C$_H$		

(Continued)

(Continued)

Interrupt source	EI²OS support	µDMA channel no.	Interrupt vector		Interrupt control register	
			No.	Address	No.	Address
SIO1	○	13	#37	FFFF68H	ICR13	0000BDH
SIO2	○	14	#38	FFFF64H		
I²C interface	×	×	#39	FFFF60H	ICR14	0000BEH
A/D	○	15	#40	FFFF5CH		
Flash write/erase, time base timer, watch timer*	×	×	#41	FFFF58H	ICR15	0000BFH
Delay interrupt generator module	×	×	#42	FFFF54H		

◎ : Interrupt request flag cleared by the interrupt clear signal. The stop request is available.

○ : Interrupt request flag cleared by the interrupt clear signal.

× : Interrupt request flag not cleared by the interrupt clear signal.

* : Note that flash write/erase cannot be used at the same time as the time base timer or watch timer.

Note : • If two or more interrupt sources have the same interrupt number, the resource will clear both interrupt request flags at the EI²OS/DMAC interrupt clear signal. Thus when EI²OS/µDMA function of two sources is used, the other interrupt function cannot be used. The interrupt request enable bit of the corresponding resource should be set to “0” for software polling processing.

• Maximum assured operation frequency of µDMA is 16 MHz.

■ PERIPHERAL RESOURCES

1. I/O Ports

The I/O ports output data from the CPU to the I/O pins, and also load signals input at the I/O pins into the CPU, according to the port register (PDR) . The ports can also control the input/output direction of the I/O pins in bit units according to the port direction register (DDR) .
The MB90470 series has 82 input/output pins and two open drain output pins. Ports 0 through A are input/output ports, and port 76, and 77 are the open drain ports.

(1) Port Registers

	7	6	5	4	3	2	1	0	Default value	Access
PDR0 Address : 000000H	P07	P06	P05	P04	P03	P02	P01	P00	Undefined	R/W*
PDR1 Address : 000001H	P17	P16	P15	P14	P13	P12	P11	P10	Undefined	R/W*
PDR2 Address : 000002H	P27	P26	P25	P24	P23	P22	P21	P20	Undefined	R/W*
PDR3 Address : 000003H	P37	P36	P35	P34	P33	P32	P31	P30	Undefined	R/W*
PDR4 Address : 000004H	P47	P46	P45	P44	P43	P42	P41	P40	Undefined	R/W*
PDR5 Address : 000005H	P57	P56	P55	P54	P53	P52	P51	P50	Undefined	R/W*
PDR6 Address : 000006H	P67	P66	P65	P64	P63	P62	P61	P60	Undefined	R/W*
PDR7 Address : 000007H	P77	P76	P75	P74	P73	P72	P71	P70	11XXXXXX	R/W*
PDR8 Address : 000008H	P87	P86	P85	P84	P83	P82	P81	P80	Undefined	R/W*
PDR9 Address : 000009H	P97	P96	P95	P94	P93	P92	P91	P90	Undefined	R/W*
PDRA Address : 00000AH	—	—	—	—	PA3	PA2	PA1	PA0	Undefined	R/W*

* : Input/output port read/write operations are somewhat different than reading and writing to memory, and operate as follows.
- Input mode
  Read : Reads the signal level of the corresponding pin.
  Write : Writes to the output latch.
- Output mode
  Read : Reads the value of the data register latch.
  Write : Value is output to the corresponding pin.

(2) Port Direction Registers

	7	6	5	4	3	2	1	0	Default value	Access
DDR0 Address : 000010H	D07	D06	D05	D04	D03	D02	D01	D 00	00000000	R/W
DDR1 Address : 000011H	D17	D16	D15	D14	D13	D12	D11	D10	00000000	R/W
DDR2 Address : 000012H	D27	D26	D25	D24	D23	D22	D21	D20	00000000	R/W
DDR3 Address : 000013H	D37	D36	D35	D34	D33	D32	D31	D30	00000000	R/W
DDR4 Address : 000014H	D47	D46	D45	D44	D43	D42	D41	D40	00000000	R/W
DDR5 Address : 000015H	D57	D56	D55	D54	D53	D52	D51	D50	00000000	R/W
DDR6 Address : 000016H	D67	D66	D65	D64	D63	D62	D61	D60	00000000	R/W
DDR7 Address : 000017H	—	—	D75	D74	D73	D72	D71	D70	00000000	R/W
DDR8 Address : 000018H	D87	D86	D85	D84	D83	D82	D81	D80	00000000	R/W
DDR9 Address : 000019H	D97	D96	D95	D94	D93	D92	D91	D90	00000000	R/W
DDRA Address : 00001AH	—	—	—	—	DA3	DA2	DA1	DA0	- - - - 0000	R/W

- When a pin is functioning as a port, the corresponding pin control setting is as follows :
  0 : Input mode
  1 : Output mode The register value is “0” at reset.
- Port 76, 77
  These ports do not have DDR registers. Data at these pins is always valid, so that when P76, P77 are used as I^2C pins the PDR value should be “1”. (The I^2C functions should be stopped, when these pins are used as P76,P77 .)
  These ports have open drain configuration. If they are used as input ports, the output transistor is turned off, so that the output data register must be set to “1” and pull-up resistance applied.

Note : If these registers are accessed using read-modify-write instructions (such as bit set instructions) ,the bit that is the object of the instruction will be set to the specified value but for other bits the value of the corresponding output register will be rewritten to the input value of the pin at that time. For this reason when a pin used for input is switched to output, first write the desired value to the PDR register, then set the DDR register to switch the pin direction.

(3) Input Resistance Registers

RDR0 Address : 00001C$_H$

7	6	5	4	3	2	1	0	Default value	Access
RD07	RD06	RD05	RD04	RD03	RD02	RD01	RD00	00000000	R/W

RDR1 Address : 00001D$_H$

7	6	5	4	3	2	1	0	Default value	Access
RD17	RD16	RD15	RD14	RD13	RD12	RD11	RD10	00000000	R/W

These registers control pull-up resistance in input mode.

0 : No pull-up resistance in input mode.

1 : Pull-up resistance applied in input mode.

In output mode, the setting has no significance (no pull-up resistance) . The direction registers (DDR) control switching between input and output modes.

In stop mode (SPL = 1) pull-up resistance is removed (high impedance) . When an external bus is used, this function is prohibited and no values should be written to this register.

(4) Output Pin Registers

ODR7 Address : 00001E$_H$

7	6	5	4	3	2	1	0	Default value	Access
—	—	OD75	OD74	OD73	OD72	OD71	OD70	00000000	R/W

ODR4 Address : 00001B$_H$

7	6	5	4	3	2	1	0	Default value	Access
OD47	OD46	OD45	OD44	OD43	OD42	OD41	OD40	00000000	R/W

These registers control open drain operation in output mode.

0 : Operates as standard output port in output mode.

1 : Operates as open drain port in output mode.

In input mode, the setting has no significance (High-Z output) . The direction registers (DDR) control switching between input and output modes. When an external bus is used, this function is prohibited and no values should be written to this register.

(5) Analog Input Enable Register

ADER Address : 00001F$_H$

7	6	5	4	3	2	1	0	Default value	Access
ADE7	ADE6	ADE5	ADE4	ADE3	ADE2	ADE1	ADE0	11111111	R/W

This register controls the port 6 pins as follows.

0 : Port input/output mode.

1 : Analog input mode. The register value is “1” at reset.

(6) Up-down Timer Input Enable Mode

UDER Address : 00000B$_H$

7	6	5	4	3	2	1	0	Default value	Access
—	—	UDE5	UDE4	UDE3	UDE2	UDE1	UDE0	XX000000	R/W

This register controls the port 3 pins as follows.

0 : Port input mode

1 : Up-down timer input mode. The register value is “0” at reset.

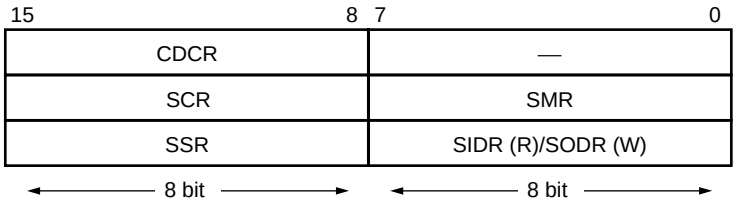
In the MB90470 series, the pin functions are as follows : UDE0 : P30/AIN0, UDE1 : P31/BIN0, UDE2 : P32/ZIN0, UDE3 : P33/AIN1, UDE4 : P34/BIN1, UDE5 : P35/ZIN1

2. UART

The UART is a serial I/O port for asynchronous (start-stop synchronized) communication or CLK synchronized communication.

- Full duplex double buffer
- Asynchronous (start-stop synchronized) and CLK synchronized (no start bit or stop bit) operation
- Supports multi-processor modes
- Built-in dedicated baud rate generator
  Asynchronous operation : 76923/38461/19230/9615/500 K/250 Kbps
  CLK synchronized : 16 M/8 M/4 M/2 M/1 M/500 K
- Baud rate can be set independently from external clock
- Can use internal clock feed from PPG1.
- Data length : 7 bits (asynchronous normal mode only) or 8 bits
- Master-slave communication functions (in multi-processor mode) : allows 1 (master) -to-n (slave) communications
- Error detection functions (parity, framing, overrun)
- NRZ-encoded transfer signal
- DMAC support (receiving/sending)

(1) Register List



Serial mode register (SMR)

Address : 000020H

7	6	5	4	3	2	1	0
MD1	MD0	CS2	CS1	CS0	Reserved	SCKE	SOE
(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
(0)	(0)	(0)	(0)	(0)	(X)	(0)	(0)

Default value

Serial control register (SCR)

Address : 000021H

15	14	13	12	11	10	9	8
PEN	P	SBL	CL	A/D	REC	RXE	TXE
(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(W)	(R/W)	(R/W)
(0)	(0)	(0)	(0)	(0)	(1)	(0)	(0)

Default value

Serial input/output register (SIDR/SODR)

Address : 000022H

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0
(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
(X)	(X)	(X)	(X)	(X)	(X)	(X)	(X)

Default value

Serial data register (SSR)

Address : 000023H

15	14	13	12	11	10	9	8
PE	ORE	FRE	RDRF	TDRE	BDS	RIE	TIE
(R)	(R)	(R)	(R)	(R)	(R/W)	(R/W)	(R/W)
(0)	(0)	(0)	(0)	(1)	(0)	(0)	(0)

Default value

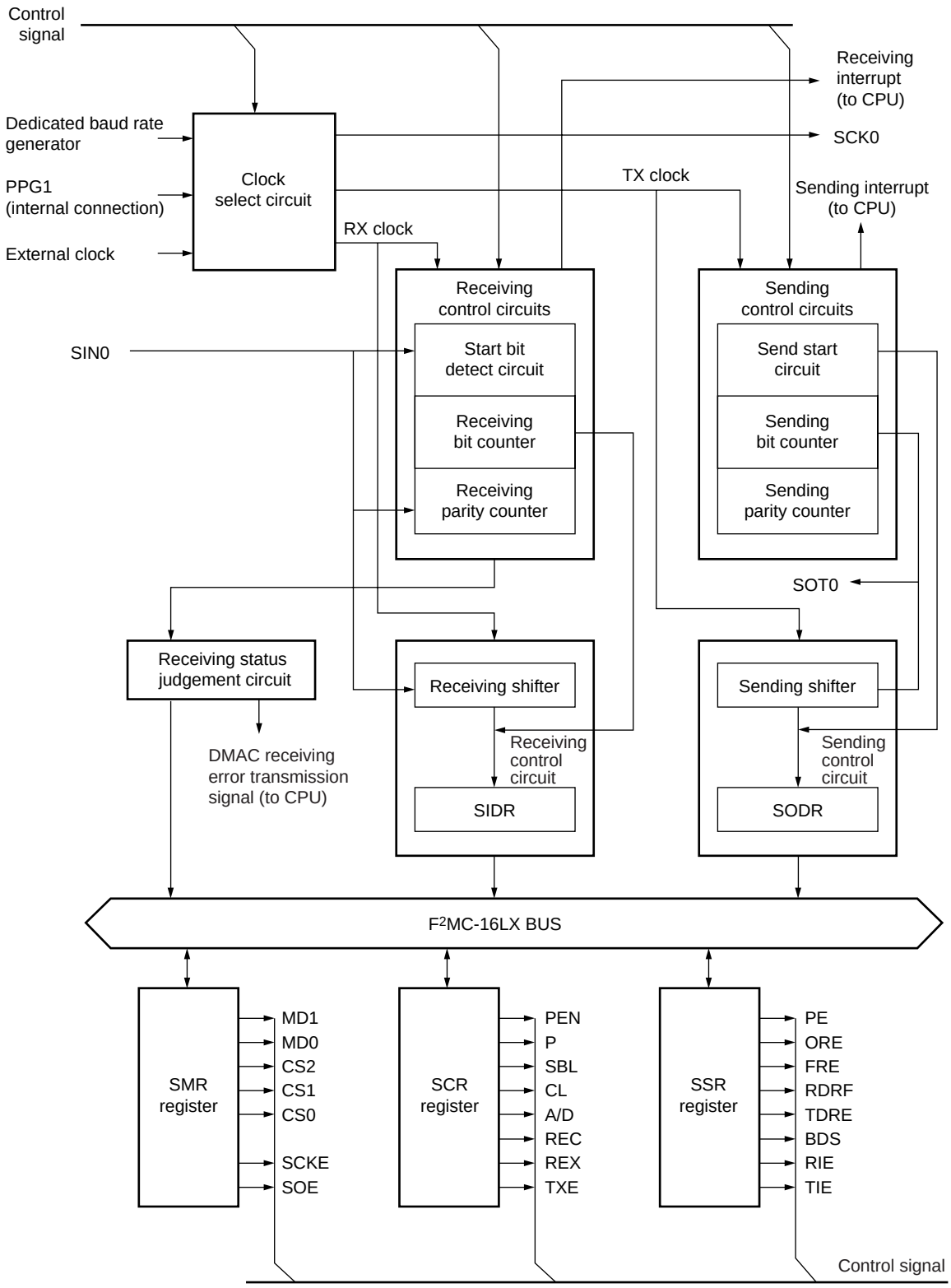
Communication prescaler control register (CDCR)

Address : 000025H

15	14	13	12	11	10	9	8
MD	SRST	—	—	DIV3	DIV2	DIV1	DIV0
(R/W)	(R/W)	(—)	(—)	(R/W)	(R/W)	(R/W)	(R/W)
(0)	(0)	(—)	(—)	(0)	(0)	(0)	(0)

Default value

(2) Block Diagram



3. Expanded I/O Serial Interface

The expended I/O serial interface is a serial I/O interface in 8-bit × 1 channel configuration allowing clock synchronized data transmission.

The interface has two serial I/O operating modes.

- Internal shift clock mode : Data transfer is synchronized with an internal clock.
- External shift clock mode : Data transfer is synchronized with a clock input from an external pin (SCK) . This mode allows the external clock pin (SCK) to be shared with a general purpose port that can transfer data according to CPU instructions.

(1) Register List

Serial mode control status register (SMCS)

Address : 000027_H / $00002B_H$

15	14	13	12	11	10	9	8	Initial value
SMD2	SMD1	SMD0	SIE	SIR	BUSY	STOP	STRT	00000010_B
(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

Address : 000026_H / $00002A_H$

7	6	5	4	3	2	1	0	Initial value
—	—	—	—	MODE	BDS	SOE	SCOE	----0000$_B$
(—)	(—)	(—)	(—)	(R/W)	(R/W)	(R/W)	(R/W)	

Serial data register (SDR)

Address : 000028_H / $00002C_H$

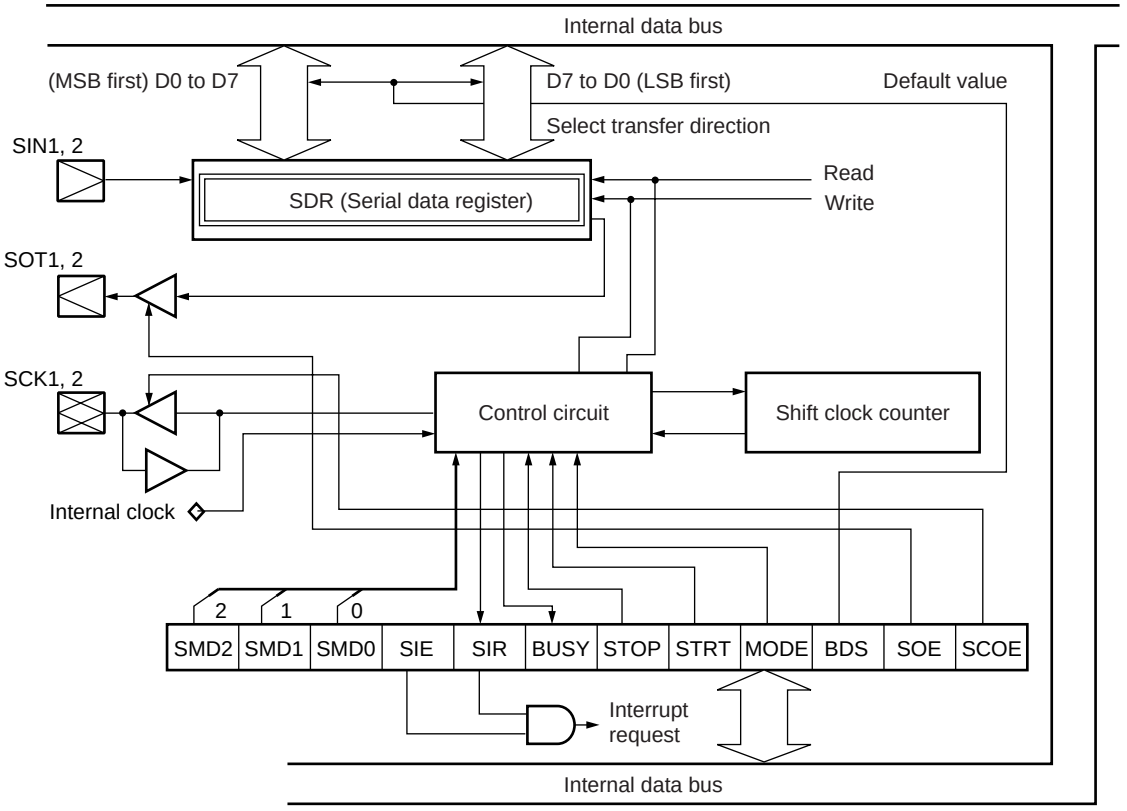
7	6	5	4	3	2	1	0	Initial value
D7	D6	D5	D4	D3	D2	D1	D0	XXXXXXXX$_B$
(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

Communication prescaler control register (SDCR0, SDCR1)

Address : 000029_H / $00002D_H$

15	14	13	12	11	10	9	8	Initial value
MD	—	—	—	DIV3	DIV2	DIV1	DIV0	0---0000$_B$
(R/W)	(—)	(—)	(—)	(R/W)	(R/W)	(R/W)	(R/W)	

(2) Block Diagram



4. 8/10-bit A/D Converter

The A/D converter converts analog input voltages into digital values, and provides the following features :

- Conversion time : minimum 4.9 µs per channel
  (at 98 machine cycles/machine clock 20 MHz, including sampling time)
- Sampling time : minimum 3.0 µs per channel
  (at 60 machine cycles/machine clock 20 MHz)
- Uses RC sequential comparison conversion with sample & hold circuit.
- Selection of 8- or 10-bit resolution
- Analog input from 8 channels, by program selection
  Single conversion mode : Convert 1 selected channel
  Scan conversion mode : Convert multiple consecutive channels. Select up to 8 channels by program selection.
  Continuous conversion mode : Convert specified channel continuously.
  Stop conversion mode : Convert one channel, pause and stand by until the next start. (Simultaneous conversion start available.)
- At the end of A/D conversion, an A/D conversion end interrupt request can be sent to the CPU. This interrupt request can start the µDMA and transfer the conversion data to memory, making it ideal for continuous processing.
- Start sources include selection of software, external trigger (falling edge) , or timer (rising edge) .

(1) Register List

ADCS2, ADCS1 (Control status registers)

ADCS1
Address : 000046H

bit	7	6	5	4	3	2	1	0	
	MD1	MD0	ANS2	ANS1	ANS0	ANE2	ANE1	ANE0	
	0	0	0	0	0	0	0	0	←Default value
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	←Bit attributes

ADCS2
Address : 000047H

bit	15	14	13	12	11	10	9	8	
	BUSY	INT	INTE	PAUS	STS1	STS0	STRT	Reserved	
	0	0	0	0	0	0	0	0	←Default value
	R/W	R/W	R/W	R/W	R/W	R/W	W	R/W	←Bit attributes

ADCR2, ADCR1 (Data registers)

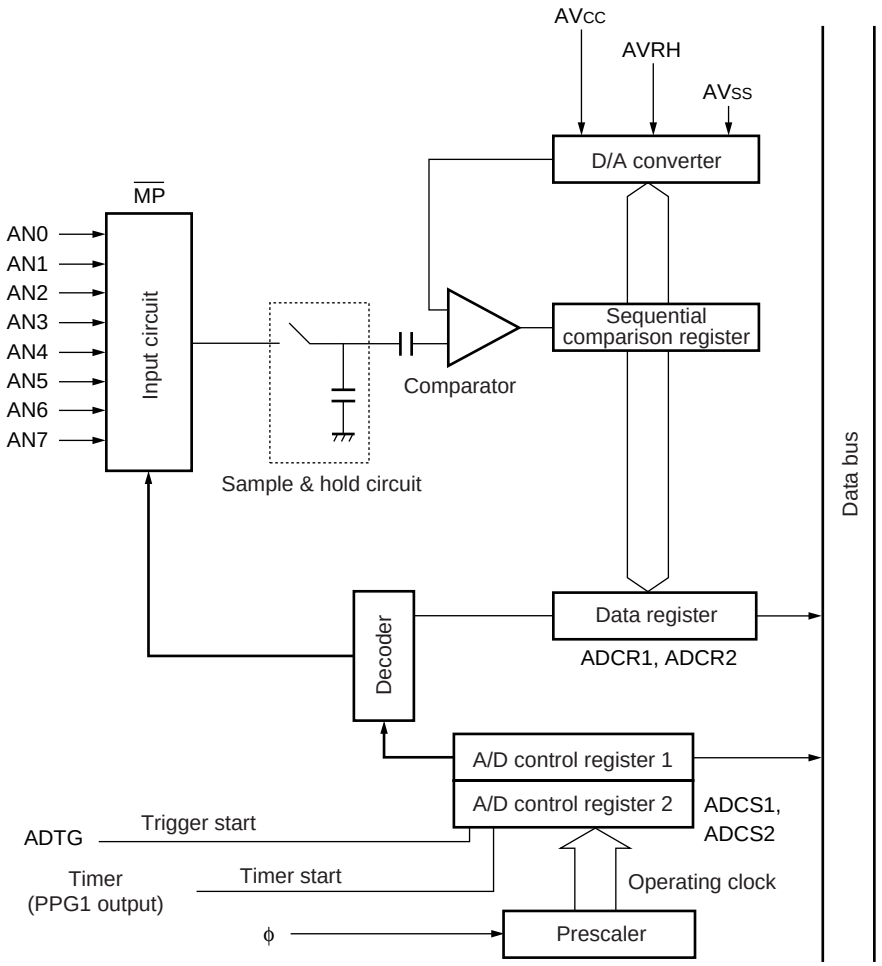
ADCR1
Address : 000048H

bit	7	6	5	4	3	2	1	0	
	D7	D6	D5	D4	D3	D2	D1	D0	
	X	X	X	X	X	X	X	X	←Default value
	R	R	R	R	R	R	R	R	←Bit attributes

ADCR2
Address : 000049H

bit	15	14	13	12	11	10	9	8	
	S10	ST1	ST0	CT1	CT0	—	D9	D8	
	0	0	0	0	0	X	X	X	←Default value
	R/W	W	W	W	W	R	R	R	←Bit attributes

(2) Block Diagram



5. 8/16-bit PPG

The 8/16-bit PPG is an 8-bit reload timer module that produces a PPG output in the form of a pulse for timer operation. The hardware configuration includes six 8-bit down counters, twelve 8-bit reload timers, three 16-bit control registers, six external pulse output pins, and six interrupt outputs. The MB90470 provides six 8-bit PPG channels, which can also operate as three 16-bit PPG channels in the combination PPG0 + PPG1, PPG2 + PPG3, PPG4 + PPG5. The following is an overview of the functions of the PPG.

- Six-channel independent 8-bit PPG output mode : Provides PPG output operation independently on six channels.
- 16-bit PPG output operation mode : Provides 16-bit PPG output operation on three channels, using the combination PPG0 + PPG1, PPG2 + PPG3, PPG4 + PPG5.
- 8 + 8-bit PPG output operation mode :
  Uses the PPG0 (PPG2/PPG4) output as the PPG1 (PPG3/PPG5) clock input, to enable 8-bit PPG output with any desired period.
- PPG output operation :
  Outputs pulse waves at a specified period and duty ratio.
  Can be also used with an external circuit as a D/A converter.

(1) Register List

PPGC0 (PPG0/2/4 operating mode control register)

	7	6	5	4	3	2	1	0	
00003A$_H$ 00003C$_H$ 00003E$_H$	PEN0	—	PE00	PIE0	PUF0	—	—	Reserved	
	(R/W) (0)	(—) (X)	(R/W) (0)	(R/W) (0)	(R/W) (0)	(—) (X)	(—) (X)	(—) (1)	Read/write Default value

PPGC1 (PPG1/3/5 operating mode control register)

	15	14	13	12	11	10	9	8	
00003B$_H$ 00003D$_H$ 00003F$_H$	PEN1	—	PE10	PIE1	PUF1	MD1	MD0	Reserved	
	(R/W) (0)	(—) (X)	(R/W) (0)	(R/W) (0)	(R/W) (0)	(R/W) (0)	(R/W) (0)	(—) (1)	Read/write Default value

PPG01/PPG23/PPG45 (PPG0-PPG5 output control register)

	7	6	5	4	3	2	1	0	
000040$_H$ 000042$_H$ 000044$_H$	PCS2	PCS1	PCS0	PCM2	PCM1	PCM0	Reserved	Reserved	
	(R/W) (0)	(R/W) (0)	(R/W) (0)	(R/W) (0)	(R/W) (0)	(R/W) (0)	(R/W) (0)	(R/W) (0)	Read/write Default value

PPLL0 to PPLL5 (Reload register L)

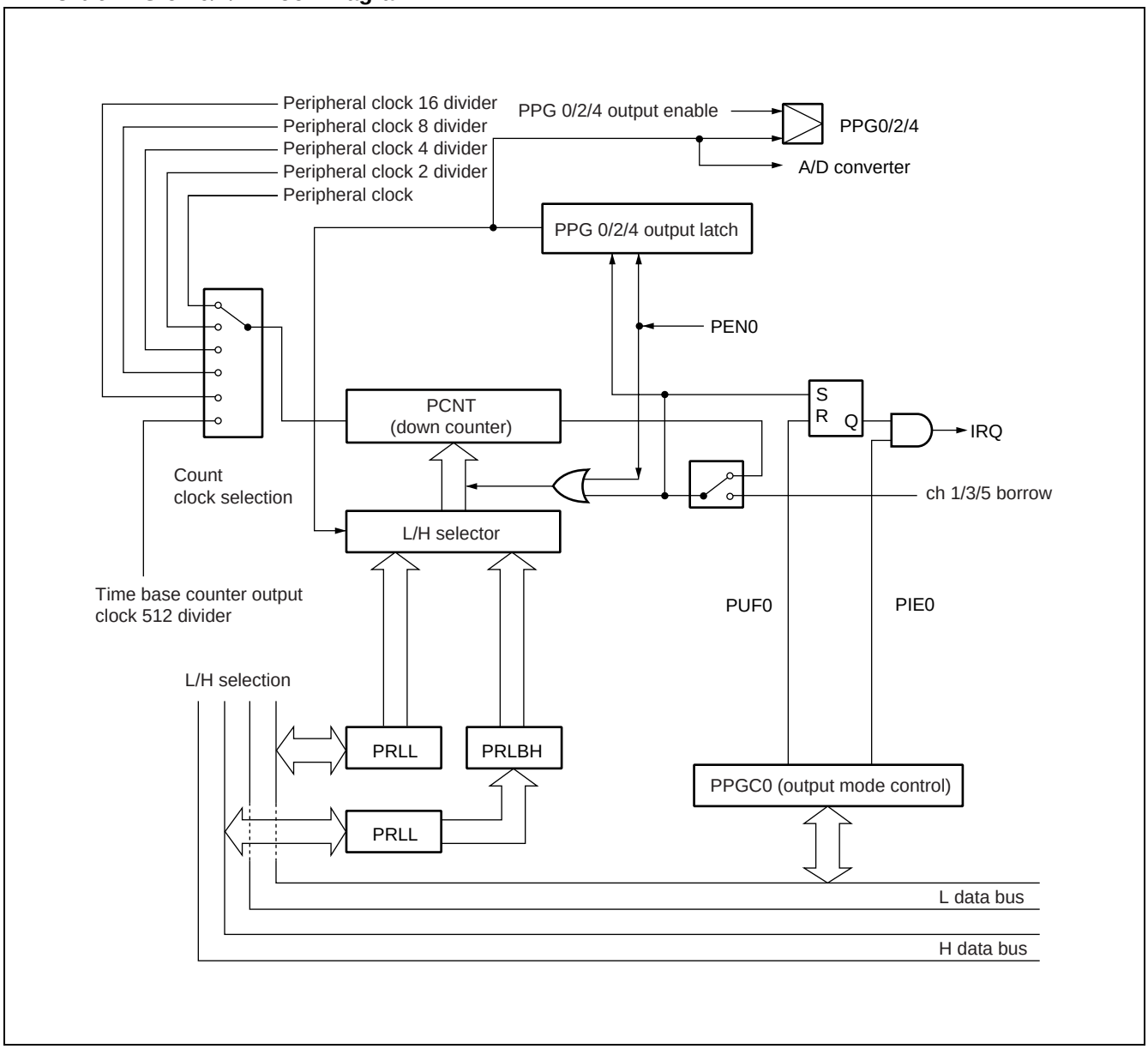
	7	6	5	4	3	2	1	0	
00002E$_H$ 000030$_H$ 000032$_H$ 000034$_H$ 000036$_H$ 000038$_H$	D07	D06	D05	D04	D03	D02	D01	D00	
	(R/W) (X)	(R/W) (X)	(R/W) (X)	(R/W) (X)	(R/W) (X)	(R/W) (X)	(R/W) (X)	(R/W) (X)	Read/write Default value

PPLH0 to PPLH5 (Reload register H)

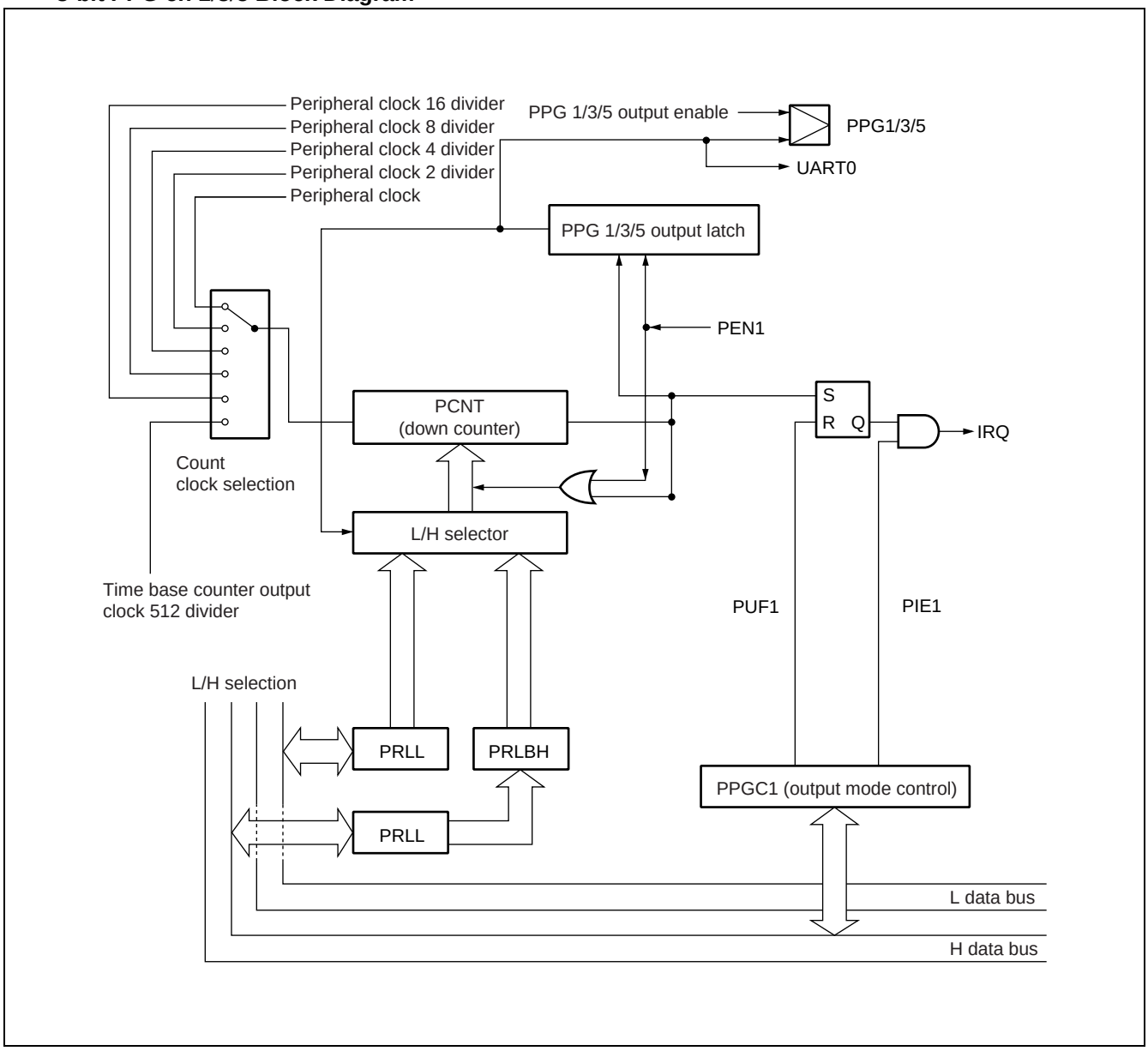
	15	14	13	12	11	10	9	8	
00002F$_H$ 000031$_H$ 000033$_H$ 000035$_H$ 000037$_H$ 000039$_H$	D15	D14	D13	D12	D11	D10	D09	D08	
	(R/W) (X)	(R/W) (X)	(R/W) (X)	(R/W) (X)	(R/W) (X)	(R/W) (X)	(R/W) (X)	(R/W) (X)	Read/write Default value

(2) Block Diagram

- **8-bit PPG ch 0/2/4 Block Diagram**



- **8-bit PPG ch 1/3/5 Block Diagram**



6. 8/16-bit Up-down Counter/Timer

This block is an up-down counter/timer configured with six event input pins, two 8-bit up/down counters, two 8-bit reload/compare registers, and related control circuits.

(1) Principal functions

- 8-bit count registers for counting in the range 0 to 256.
  (Also operates in 16-bit × 1 mode for counting in the range 0 to 65535.)
- Count clock selection provides four count modes.
  - Count mode
    - Time mode
    - Up/down count mode
    - Phase differential count mode (2 ×)
    - Phase differential count mode (8 ×)
- In timer mode, there is a choice of two internal count clocks.
  - Count clock (16 MHz operation)
    - 125 ns (8 MHz : divided by 2)
    - 0.5 µs (2 MHz : divided by 8)
- In up/down count mode, there is a choice of external pin input signal detection edge.
  - Detection edge
    - Falling edge detection
    - Rising edge detection
    - Falling/rising edge, both edges' detection
    - Edge detection disabled
- In phase differential count mode, to provide counts for encoders for motors, etc., the A phase, B phase, and Z phase of the encoder can be input separately for highly precise counts of rotation angle, rotary speed, etc.
- The ZIN pin provides a choice of two functions.
  - ZIN pin
    - Counter clear function
    - Gate function
- Compare and reload functions are provided, each available independently or in combination. Both can be started together to provide any desired type of up/down count.
  - Compare/reload function
    - Compare function (outputs interrupt at compare events)
    - Compare function (outputs interrupt and clears count at compare events)
    - Reload function (outputs interrupt and reloads at underflow events)
    - Compare/reload function (outputs interrupt and clears count at compare events, outputs interrupt and reloads at underflow events)
    - Compare/reload disabled
- Individually controllable interrupts at compare, reload (underflow) and overflow events.
- Count direction flag enables detection of immediately preceding count direction.
- Interrupt generation at change of count direction.

(2) Register List

15	8	7	0
UDCR1		UDCR0	
RCR1		RCR0	
Reserved		CSR0	
CCRH0		CCRL0	
Reserved		CSR1	
CCRH1		CCRL1	
8 bit		8 bit	

CCRH0 (Counter control register high ch.0)

Address : 00006D$_H$

15	14	13	12	11	10	9	8
M16E	CDCF	CFIE	CLKS	CMS1	CMS0	CES1	CES0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Default value 00000000$_B$

CCRH1 (Counter control register high ch.1)

Address : 000071$_H$

15	14	13	12	11	10	9	8
—	CDCF	CFIE	CLKS	CMS1	CMS0	CES1	CES0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Default value -0000000$_B$

CCRL0/1 (Counter control register low ch.0/1)

Address : 00006C$_H$
Address : 000070$_H$

7	6	5	4	3	2	1	0
UDMS	CTUT	UCRE	RLDE	UDCC	CGSC	CGE1	CGE0
R/W	W	R/W	R/W	W	R/W	R/W	R/W

Default value 0X00X000$_B$

CSR0/1 (Counter status register ch. 0/1)

Address : 000072$_H$
Address : 000074$_H$

7	6	5	4	3	2	1	0
CSTR	CITE	UDIE	CMPF	OVFF	UDFF	UDF1	UDF0
R/W	R/W	R/W	R/W	R/W	R/W	R	R

Default value 00000000$_B$

UDCR0/1 (Up down count register ch. 0/1)

Address : 000069$_H$

15	14	13	12	11	10	9	8
D17	D16	D15	D14	D13	D12	D11	D10
R	R	R	R	R	R	R	R

Default value 00000000$_B$

Address : 000068$_H$

7	6	5	4	3	2	1	0
D07	D06	D05	D04	D03	D02	D01	D00
R	R	R	R	R	R	R	R

Default value 00000000$_B$

RCR0/1 (Reload/compare register ch. 0/1)

Address : 00006B$_H$

15	14	13	12	11	10	9	8
D17	D16	D15	D14	D13	D12	D11	D10
W	W	W	W	W	W	W	W

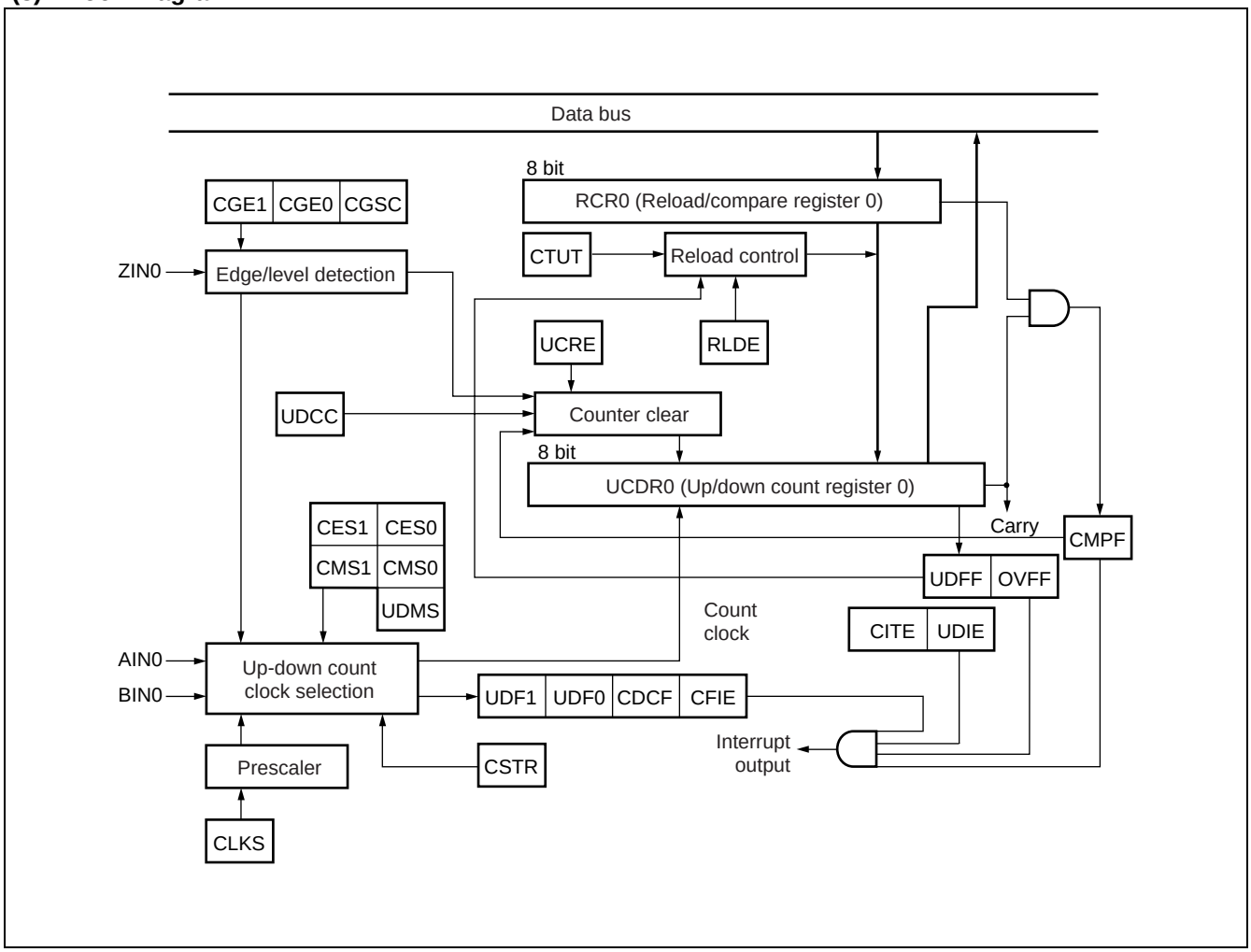
Default value 00000000$_B$

Address : 00006A$_H$

7	6	5	4	3	2	1	0
D07	D06	D05	D04	D03	D02	D01	D00
W	W	W	W	W	W	W	W

Default value 00000000$_B$

(3) Block Diagram



7. DTP/External Interrupts

The DTP (Data Transfer Peripheral) is a peripheral block that interfaces external peripherals to the F²MC-16L CPU. The DTP receives DMA request from external peripherals and passes the requests to the F²MC-16L CPU to activate the extended µDMA or interrupt processing.

(1) Register Descriptions

Interrupt/DTP enable register (ENIR : Enable Interrupt Request Register)

ENIR
Address : 00000C$_H$

7	6	5	4	3	2	1	0
EN7	EN6	EN5	EN4	EN3	EN2	EN1	EN0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Default value
00000000$_B$

Interrupt/DTP source register (EIRR : External Interrupt Request Register)

EIRR
Address : 00000D$_H$

15	14	13	12	11	10	9	8
ER7	ER6	ER5	ER4	ER3	ER2	ER1	ER0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Default value
00000000$_B$
(note that both registers relate to different interrupts)

Request level setting register (ELVR : External Level Register)

Address : 00000E$_H$

7	6	5	4	3	2	1	0
LB3	LA3	LB2	LA2	LB1	LA1	LB0	LA0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

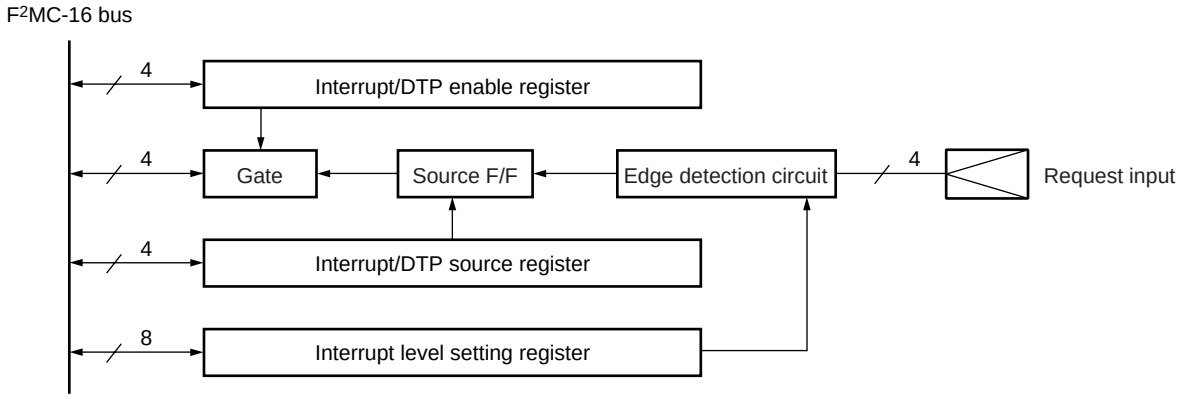
Default value
00000000$_B$

Address : 00000F$_H$

15	14	13	12	11	10	9	8
LB7	LA7	LB6	LA6	LB5	LA5	LB4	LA4
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Default value
00000000$_B$

(2) Block Diagram



8. 16-bit Input Output Timer

The 16-bit input/output timer is composed of one 16-bit free-run timer module, 6 output compare modules, and 2 input capture modules. These functions can be used to produce output of six independent wave forms based on the 16-bit free-run timer, with input pulse width measurement and external clock period measurement.

- **List of Registers for All Modules**

- 16-bit free-run timer

	15		0	
000066/67H	CPCLR			Compare clear register
000062/63H	TCDT			Timer data register
000064/65H	TCCS			Control status register

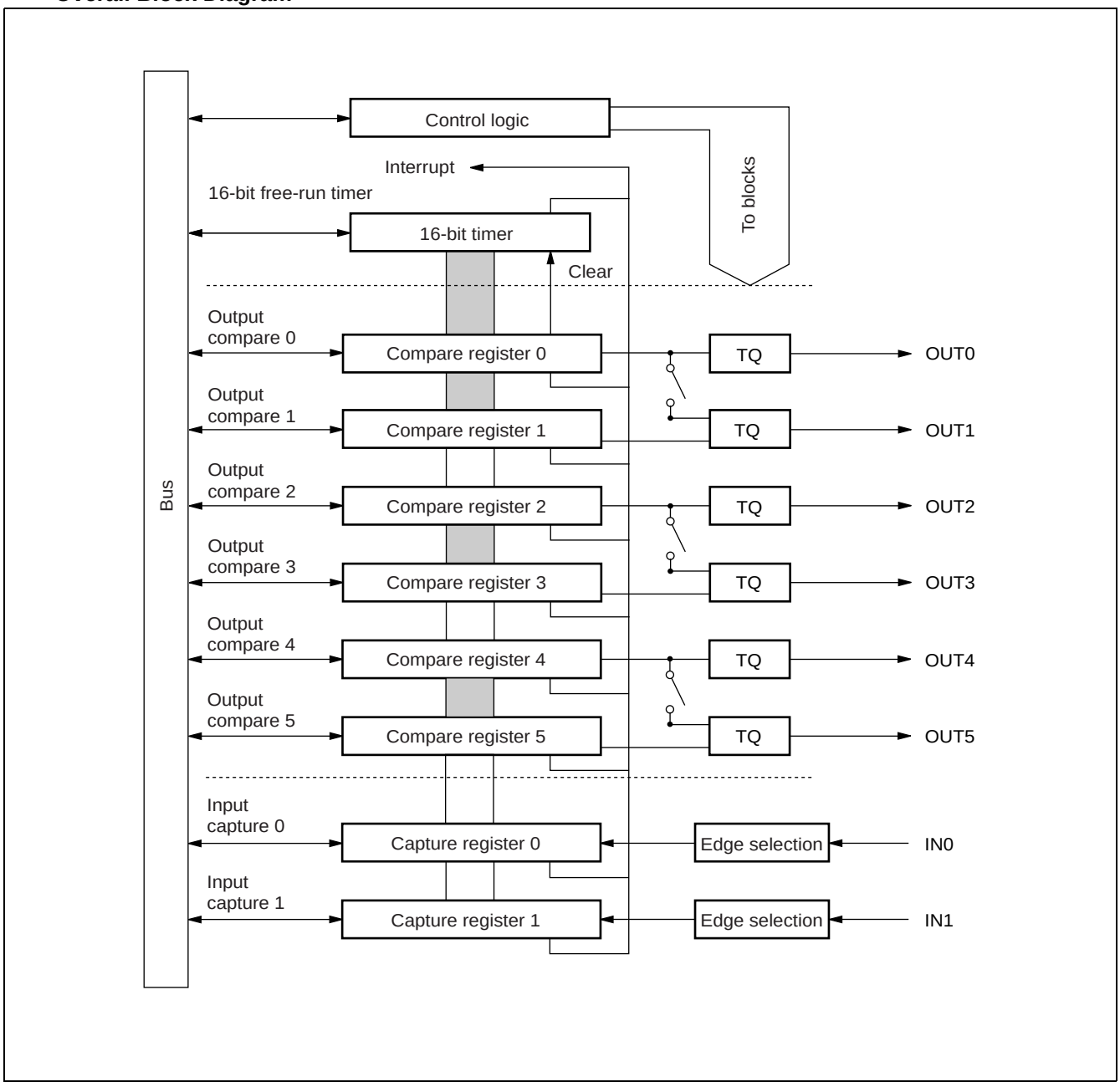
- 16-bit output compare

	15		0	
00004A, 4C, 4E, 50, 52, 54H 00004B, 4D, 4F, 51, 53, 55H	OCCP0 to OCCP5			Compare register
000056, 58, 5AH 000057, 59, 5BH	OCS1/3/5	OCS0/2/4		Control status register

- 16-bit input capture

	15		0	
00005C, 5EH 00005D, 5FH	IPCP0, ICCP1			Compare register
000060H		ICS		Control status register

- **Overall Block Diagram**



(1) 16-bit Free-run Timer

The 16-bit free-run timer is composed of a 16-bit up-down counter and control register.

The count value from this timer is used as the base timer for the input capture and output compare modules.

- A selection of 8 clock types for counter operation is available.
- Counter overflow interrupts can be generated.
- By a mode setting, the counter can be initialized when the timer value matches the compare register value for the output compare module.

- **Register list**

Compare clear register (CPCLR)

	15	14	13	12	11	10	9	8	Default value
000067H	CL15	CL14	CL13	CL12	CL11	CL10	CL09	CL08	XXXXXXXXB
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

	7	6	5	4	3	2	1	0	Default value
000066H	CL07	CL06	CL05	CL04	CL03	CL02	CL01	CL00	XXXXXXXXB
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

Timer counter data register (TCDT)

	15	14	13	12	11	10	9	8	Default value
000063H	T15	T14	T13	T12	T11	T10	T09	T08	00000000B
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

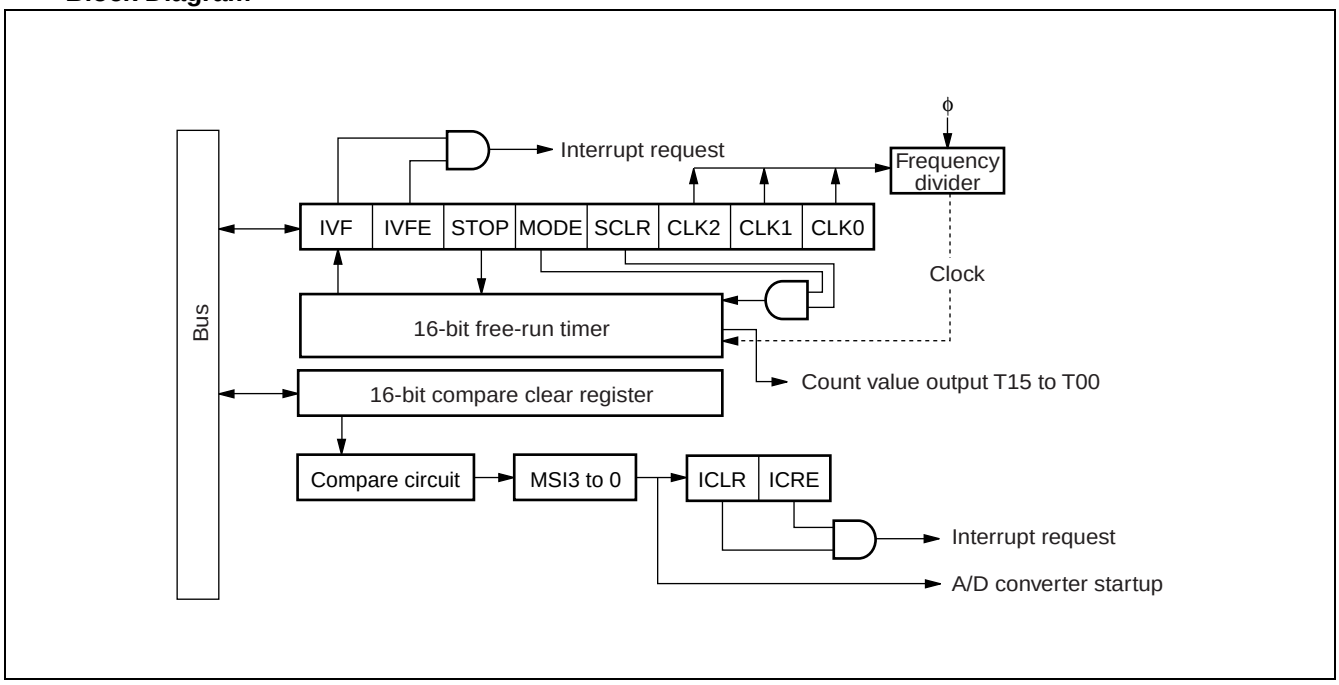
	7	6	5	4	3	2	1	0	Default value
000062H	T07	T06	T05	T04	T03	T02	T01	T00	00000000B
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

Timer counter control/status register (TCCS)

	15	14	13	12	11	10	9	8	Default value
000065H	ECKE	—	—	MSI2	MSI1	MSI0	ICLR	ICRE	0--00000B
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

	7	6	5	4	3	2	1	0	Default value
000064H	IVF	IVFE	STOP	MODE	SCLR	CLK2	CLK1	CLK0	00000000B
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

- **Block Diagram**



(2) Output Compare

The output compare module consists of a 16-bit compare register, compare output pin unit, and control register. When the value in the compare register in this module matches the value of the 16-bit free-run timer, the pin output level can be inverted and an interrupt generated.

- There are six compare registers that can operate independently. Module settings can be used to use the two compare registers to control the output.
- The interrupt can be set by a compare match.

- **Register List**

Compare register (OCCP0 to OCCP5)

	15	14	13	12	11	10	9	8	Default value
00004BH 00004DH 00004FH 000051H 000053H 000055H	C15	C14	C13	C12	C11	C10	C09	C08	XXXXXXXXB
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

	6	5	4	3	2	1	0		Default value
00004AH 00004CH 00004EH 000050H 000052H 000054H	C07	C06	C05	C04	C03	C02	C01	C00	XXXXXXXXB
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

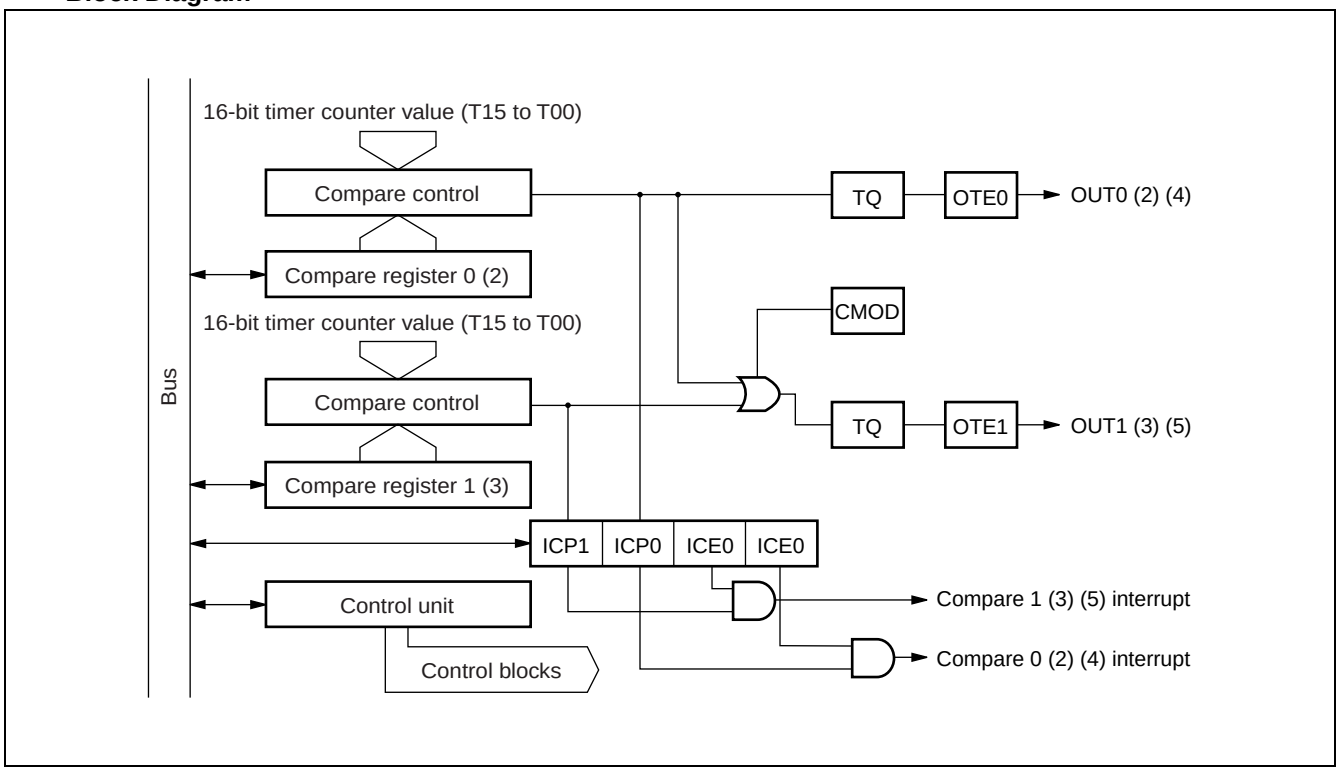
Control register (OCS1/3/5)

	15	14	13	12	11	10	9	8	Default value
000057H 000059H 00005BH	—	—	—	CMOD	OTE1	OTE0	OTD1	OTD0	---00000B
	(—)	(—)	(—)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

Control register (OCS0/2/4)

	7	6	5	4	3	2	1	0	Default value
000056H 000058H 00005AH	ICP1	ICP0	ICE1	ICE0	—	—	CST1	CST0	0000--00B
	(R/W)	(R/W)	(R/W)	(R/W)	(—)	(—)	(R/W)	(R/W)	

- **Block Diagram**



(3) Input Capture

The input capture module detects the rising edge, falling edge, or both edges of an input signal and saves the value of the 1-bit free-run timer at that moment in a register. This module can also generate an interrupt when an edge is detected.

The input capture module is composed of input capture registers and a control register. Each of the input captures has a corresponding external input pin.

- Selection of three valid edges for external input :
  Rising edge/falling edge/both edges
- An interrupt can be generated when the valid edge is detected.

- **Register List**

Input capture data registers (IPCP0, IPCP1)

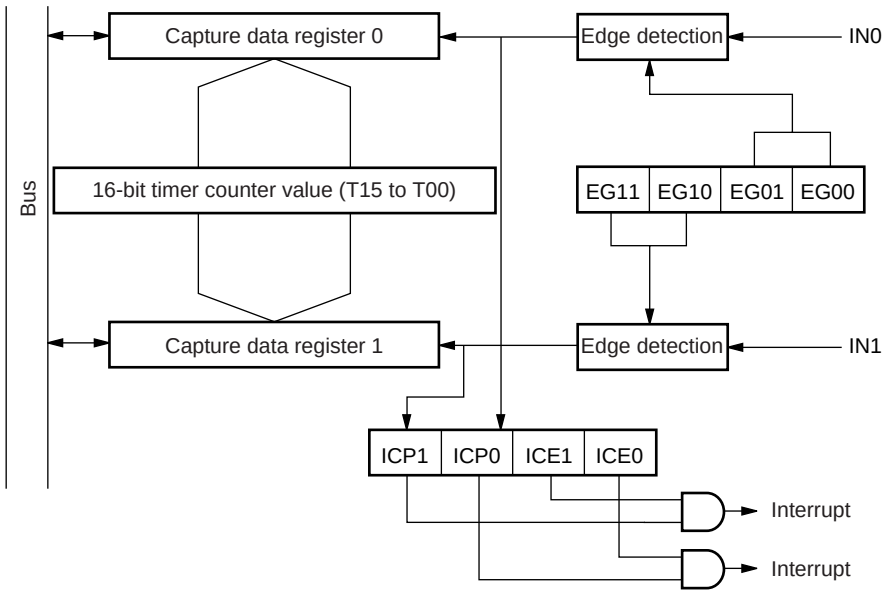
	15	14	13	12	11	10	9	8	Default value
00005D$_H$	CP15	CP14	CP13	CP12	CP11	CP10	CP09	CP08	XXXXXXXX$_B$
00005F$_H$	(R)	(R)	(R)	(R)	(R)	(R)	(R)	(R)	

	7	6	5	4	3	2	1	0	Default value
00005C$_H$	CP07	CP06	CP05	CP04	CP03	CP02	CP01	CP00	XXXXXXXX$_B$
00005E$_H$	(R)	(R)	(R)	(R)	(R)	(R)	(R)	(R)	

Control status register (ICS0, ICS1)

	7	6	5	4	3	2	1	0	Default value
000060$_H$	ICP1	ICP0	ICE1	ICE0	EG11	EG10	EG01	EG00	00000000$_B$
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

- **Block Diagram**



9. I²C Interface

The I²C interface is a serial I/O port supporting Inter IC bus operation, and operates as a master/slave device on the I²C bus. The following features are provided.

- Master/slave sending and receiving
- Arbitration functions
- Clock synchronization functions
- Slave address/general call address detection functions
- Transfer direction detection function
- Start condition repeat generator and detection function
- Bus error detection function

(1) Register List

IBSR (bus status register)

	7	6	5	4	3	2	1	0	⇦ Bit no.
Address : 000088H	BB	RSC	AL	LRB	TRX	AAS	GCA	FBT	
Read/write ⇨	(R)	(R)	(R)	(R)	(R)	(R)	(R)	(R)	
Default value ⇨	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	

IBCR (bus control register)

	15	14	13	12	11	10	9	8	⇦ Bit no.
Address : 000089H	BER	BEIE	SCC	MSS	ACK	GCAA	INTE	INT	
Read/write ⇨	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
Default value ⇨	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	

ICCR (clock control register)

	7	6	5	4	3	2	1	0	⇦ Bit no.
Address : 00008AH	—	—	EN	CS4	CS3	CS2	CS1	CS0	
Read/write ⇨	(—)	(—)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
Default value ⇨	(—)	(—)	(0)	(X)	(X)	(X)	(X)	(X)	

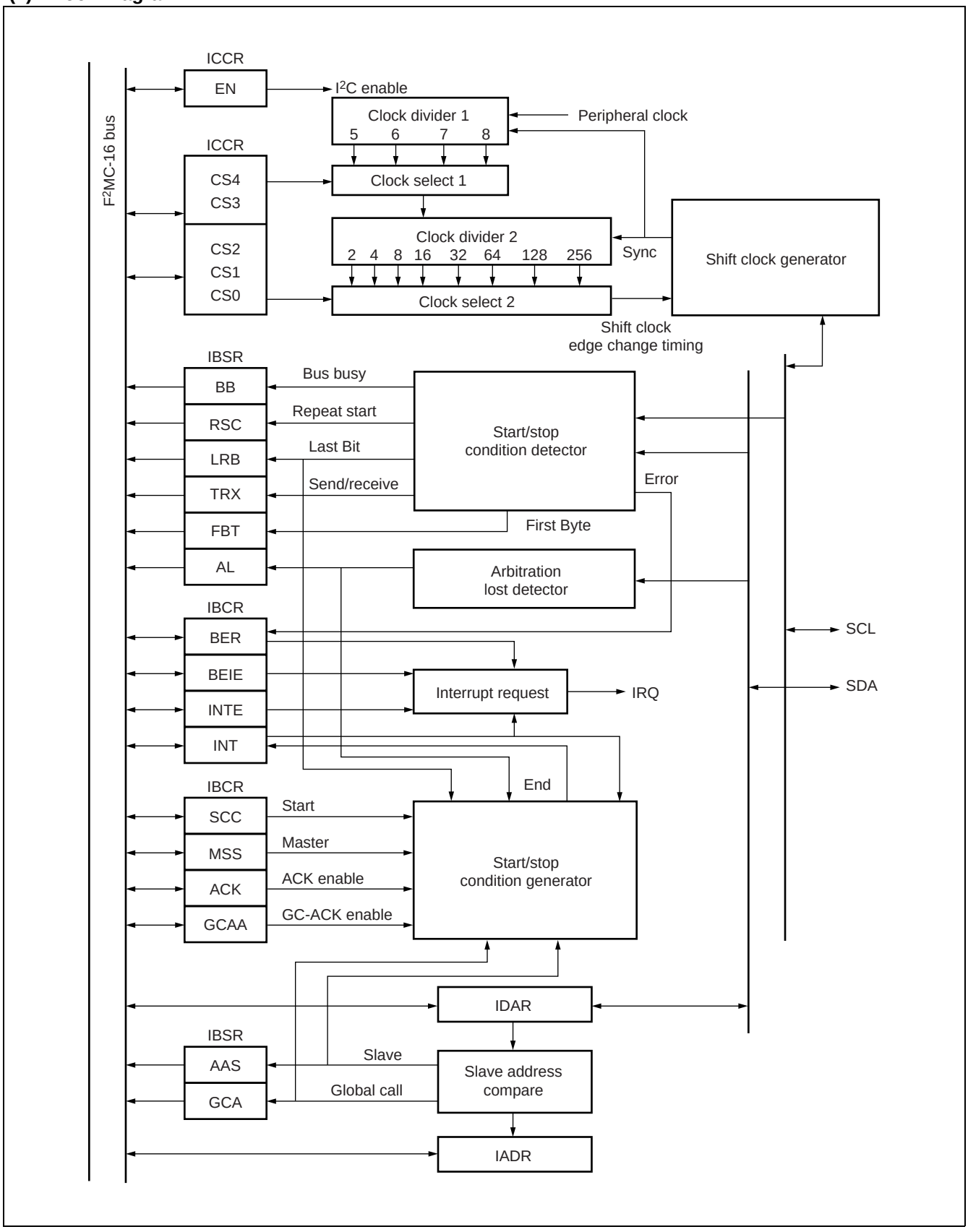
IADR (address register)

	15	14	13	12	11	10	9	8	⇦ Bit no.
Address : 00008BH	—	A6	A5	A4	A3	A2	A1	A0	
Read/write ⇨	(—)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
Default value ⇨	(—)	(X)	(X)	(X)	(X)	(X)	(X)	(X)	

IDAR (data register)

	7	6	5	4	3	2	1	0	⇦ Bit no.
Address : 00008CH	D7	D6	D5	D4	D3	D2	D1	D0	
Read/write ⇨	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
Default value ⇨	(X)	(X)	(X)	(X)	(X)	(X)	(X)	(X)	

(2) Block Diagram



10. 16-bit reload timer

The 16-bit reload timer provides a choice of two functions, one is an internal clock countdown synchronized with any of 3 types of internal clock, and the other is an event count mode that counts down at detection of a given edge of a pulse input externally. This timer defines an underflow as a transition of the count value from 0000_H to $FFFF_H$. Therefore, an underflow will occur at the count value “reload register setting count + 1”. The count operation includes a choice of reload mode in which the count set value is reloaded at each underflow event, and one-shot mode in which the count stops at an underflow event. An interrupt can be generated when the counter reaches an underflow, and the timer is DTC compatible.

(1) Register List

• TMCSR (Timer control status registers)

Timer control status register (high)

	15	14	13	12	11	10	9	8	
$0000CB_H$	—	—	—	—	CSL1	CSL0	MOD2	MOD1	
	(—)	(—)	(—)	(—)	(R/W)	(R/W)	(R/W)	(R/W)	Read/write
	(—)	(—)	(—)	(—)	(0)	(0)	(0)	(0)	Default value

Timer control status register (low)

	7	6	5	4	3	2	1	0	
$0000CA_H$	MOD0	OUTE	OUTL	RELD	INTE	UF	CNTE	TRG	
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	Read/write
	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	Default value

• 16-bit timer register/16-bit reload register

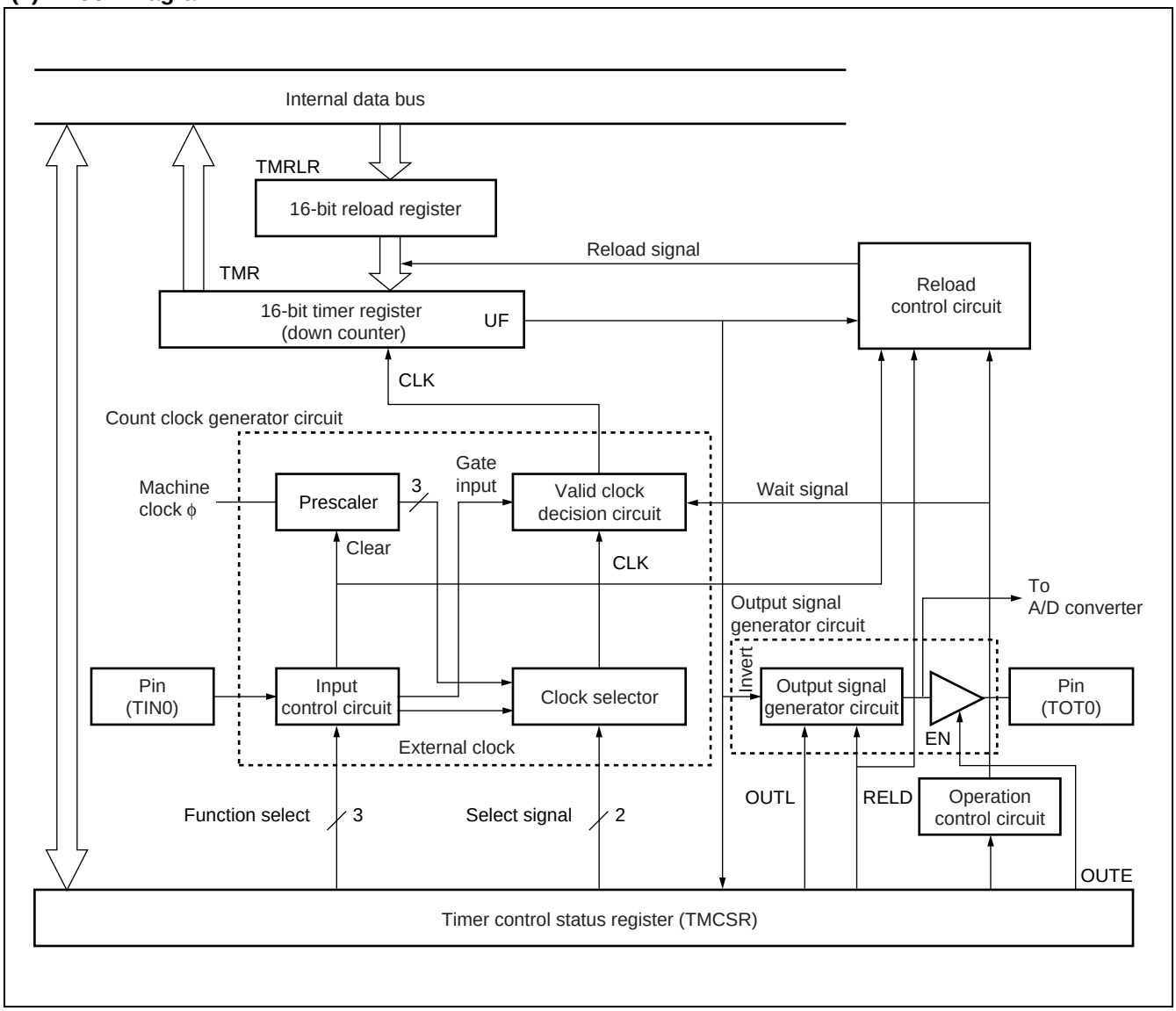
TMR/TMRLR (high)

	15	14	13	12	11	10	9	8	
$0000CD_H$	D15	D14	D13	D12	D11	D10	D09	D08	
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	Read/write
	(X)	(X)	(X)	(X)	(X)	(X)	(X)	(X)	Default value

TMR/TMRLR (low)

	7	6	5	4	3	2	1	0	
$0000CC_H$	D07	D06	D05	D04	D03	D02	D01	D00	
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	Read/write
	(X)	(X)	(X)	(X)	(X)	(X)	(X)	(X)	Default value

(2) Block Diagram



11. µPG Timer

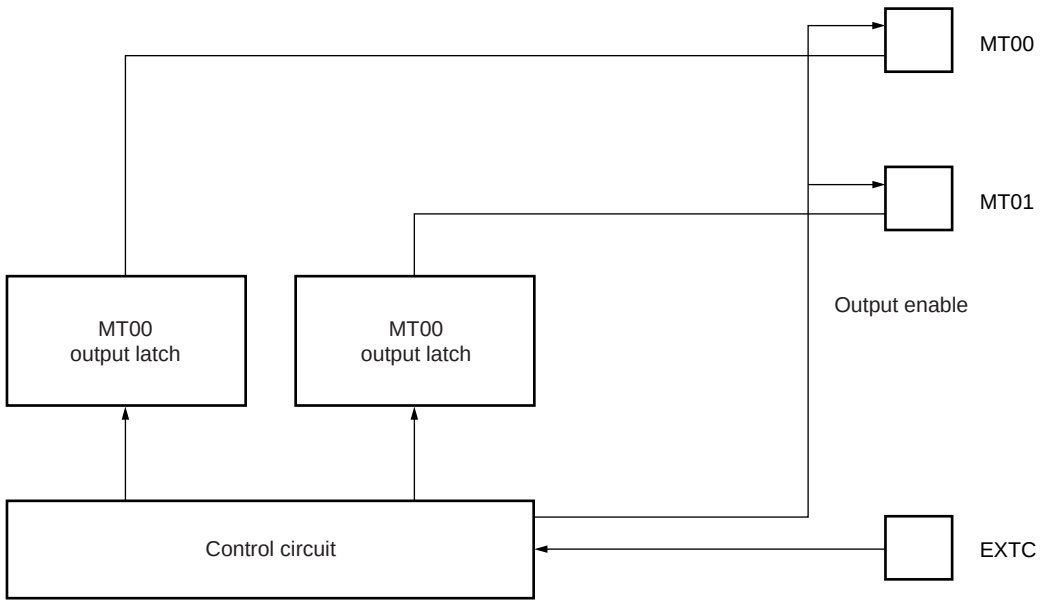
The µPG timer produces a pulse output according to an external input signal.

(1) Register List

PGCSR (PG control/status register)
Operating mode control register

	7	6	5	4	3	2	1	0	
00008E$_H$	PEN0	PE1	PE0	PMT1	PMT0	—	—	—	
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(—)	(—)	(—)	Read/write
	(0)	(0)	(0)	(0)	(0)	(—)	(—)	(—)	Default value

(2) Block Diagram



12. PWC (Pulse Width Count) Timer

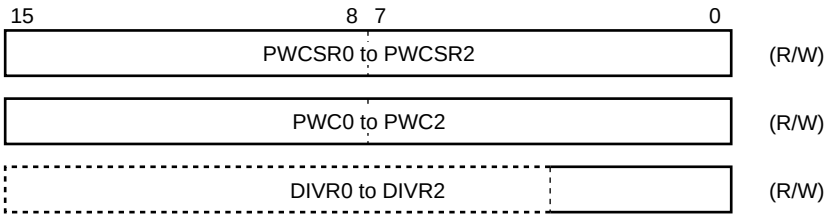
The PWC timer is a 16-bit multi-function up-count timer with an input signal pulse width measurement function.

The hardware includes a total of three channels, each with one 16-bit up-count timer, one input pulse divider and divider ration control register, one measurement input pin, and one 16-bit control register. The following functions are provided :

Timer functions :
An interrupt can be generated each time a set time interval elapses. A choice of three internal reference clocks is available.

Pulse width measurement functions :
Measures the time between designated events on an externally input pulse signal. The reference clock is selected from three internal clock signals.
Measurement modes : 1) H pulse width (↑ to ↓) /L pulse width (↑ to ↓)
2) Rise period (↑ to ↑) /fall period (↓ to ↓)
3) Measurement between edges (high or low to low or high)
An 8-bit input divider can divide the input pulse into 2^{2n} divisions (n = 1, 2, 3, 4) and measure the divisions.
An interrupt can be generated when measurement is ended. Both one-time and continuous measurement are enabled.

(1) Register List



PWCSR0 to PWCSR2 (PWC control/status registers)

	15	14	13	12	11	10	9	8	
000077H 00007BH 00007FH	STRT	STOP	EDIR	EDIE	OVIR	OVIE	ERR	Reserved	
	(R/W)	(R/W)	(R)	(R/W)	(R/W)	(R/W)	(R)	(—)	Read/write
	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(X)	Default value

	7	6	5	4	3	2	1	0	
000076H 00007AH 00007EH	CKS1	CKS0	PIS1	PIS0	S/C	MOD2	MOD1	MOD0	
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	Read/write
	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	Default value

PWCR0 to PWCR2 (PWC data buffer registers)

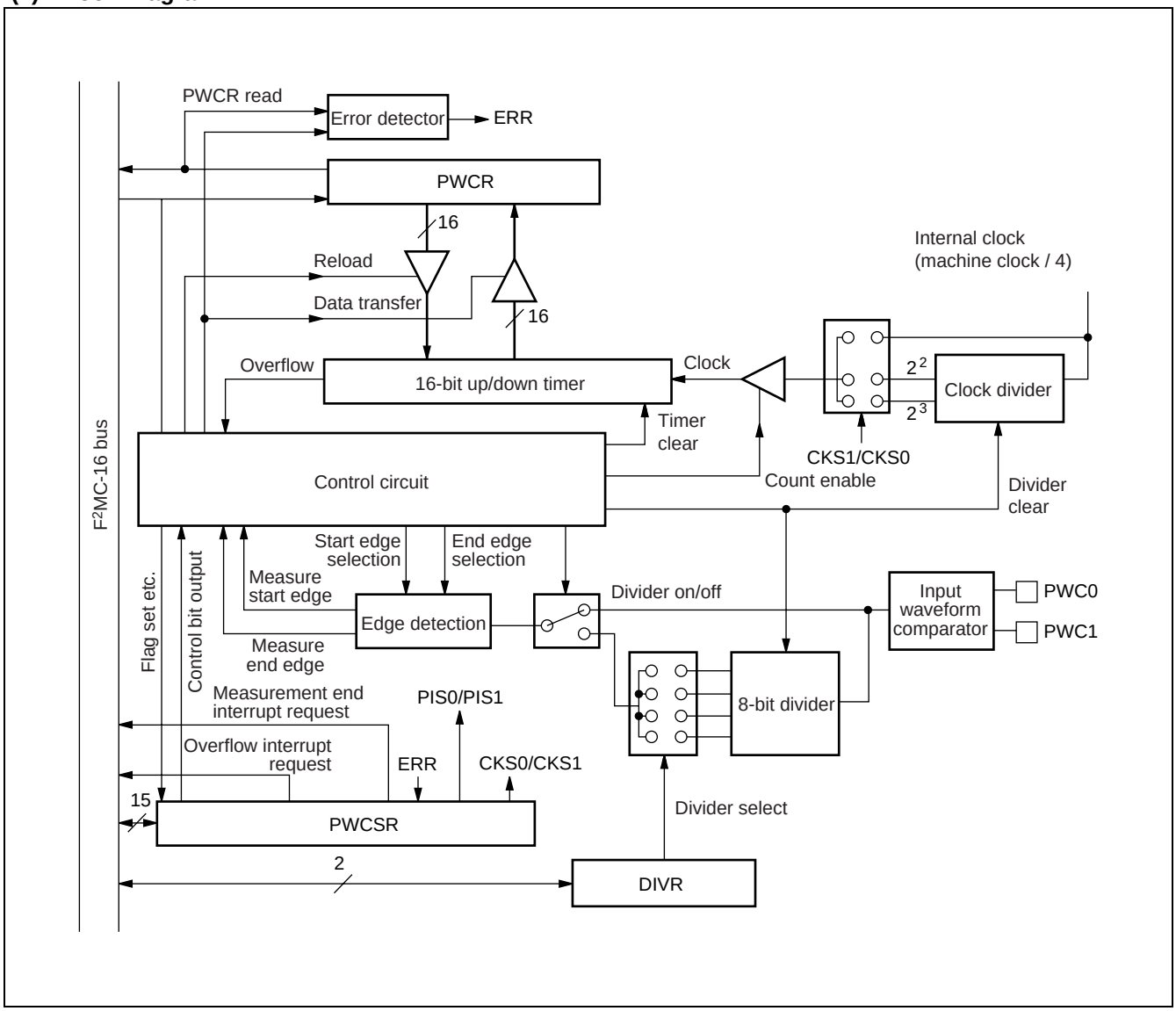
	15	14	13	12	11	10	9	8	
000079H 00007DH 000081H	D15	D14	D13	D12	D11	D10	D9	D8	
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	Read/write
	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	Default value

	7	6	5	4	3	2	1	0	
000078H 00007CH 000080H	D7	D6	D5	D4	D3	D2	D1	D0	
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	Read/write
	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	Default value

DIVR0 to DIVR2 (Divider control register)

	7	6	5	4	3	2	1	0	
000082H 000084H 000086H	—	—	—	—	—	—	DIV1	DIV0	
	(—)	(—)	(—)	(—)	(—)	(—)	(R/W)	(R/W)	Read/write
	(X)	(X)	(X)	(X)	(X)	(X)	(0)	(0)	Default value

(2) Block Diagram



13. Watch Timer

The watch timer is a 15-bit timer using a sub-clock signal. This timer can generate interval interrupts. Also, by a register setting, it can be used as a clock source for the watchdog timer.

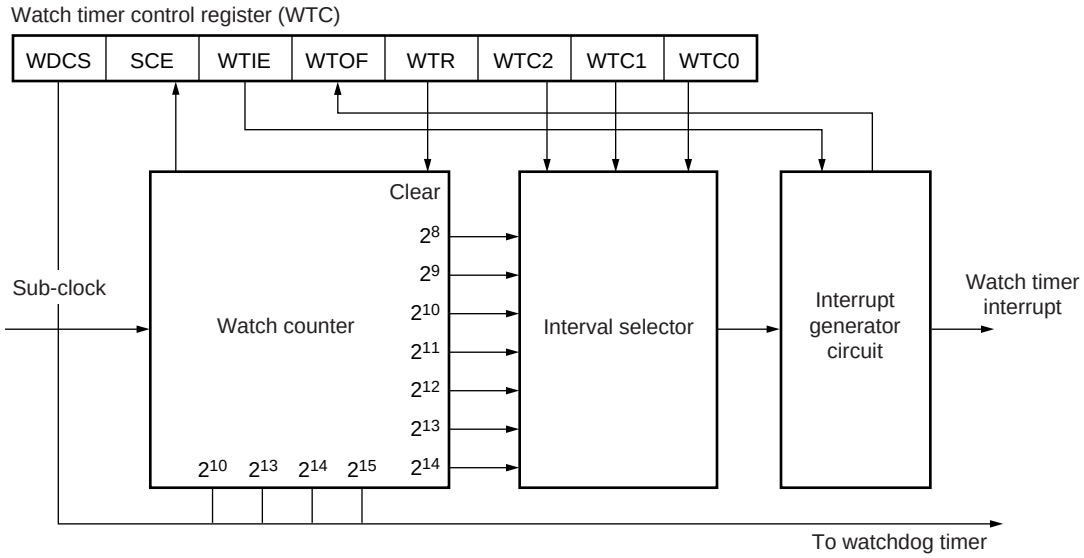
(1) Register List

Watch timer control register (WTC)

	7	6	5	4	3	2	1	0
0000AA$_H$	WDCS	SCE	WTIE	WTOF	WTR	WTC2	WTC1	WTC0
	(R/W)	(R)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
	(1)	(0)	(0)	(0)	(1)	(0)	(0)	(0)

Default value

(2) Block Diagram



14. Watchdog Timer

The watchdog timer is a 2-bit counter that uses a count clock signal output by the timer base timer or watch timer and will reset the CPU unless cleared within a specified period of time.

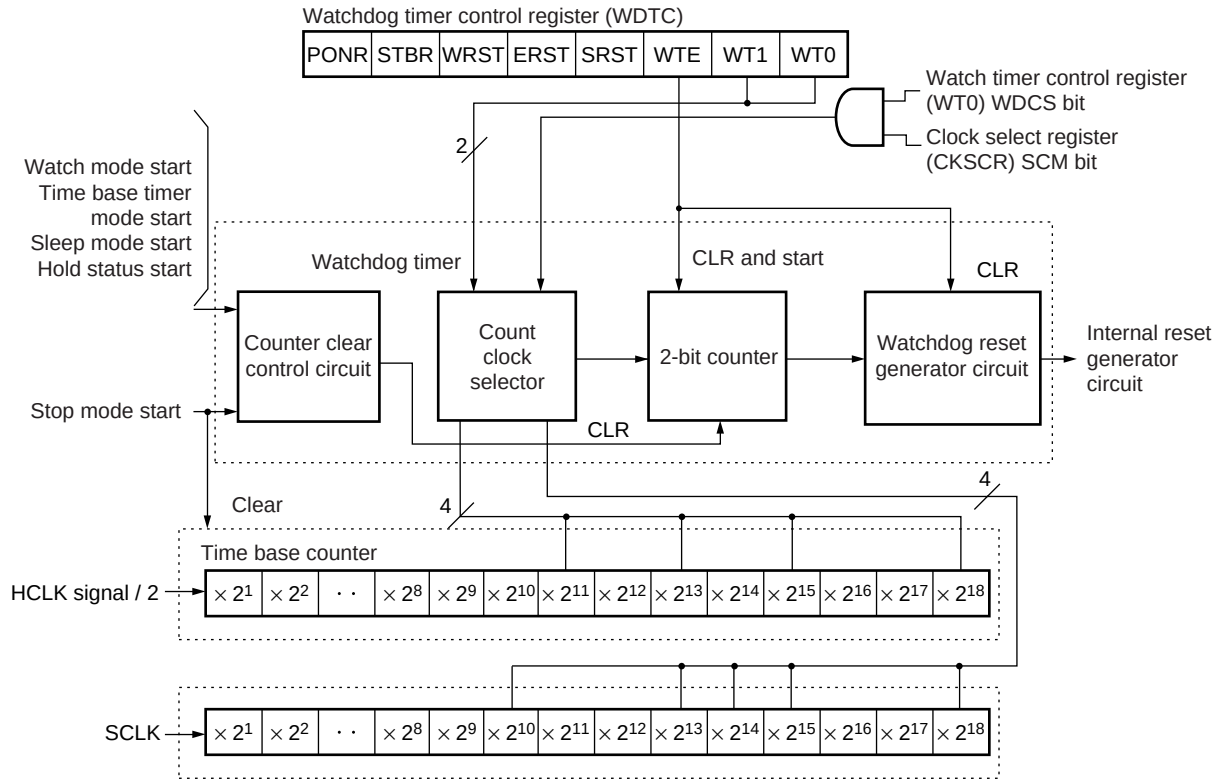
(1) Register List

Watchdog timer control register (WDTC)

	7	6	5	4	3	2	1	0
0000A8H	PONR	Reserved	WRST	ERST	SRST	WTE	WT1	WT0
	(R) (X)	(—) (X)	(R) (X)	(R) (X)	(R) (X)	(W) (1)	(W) (1)	(W) (1)

Default value

(2) Block Diagram



HCLK : Oscillator clock
SCLK : Sub-clock

15. Time Base Timer

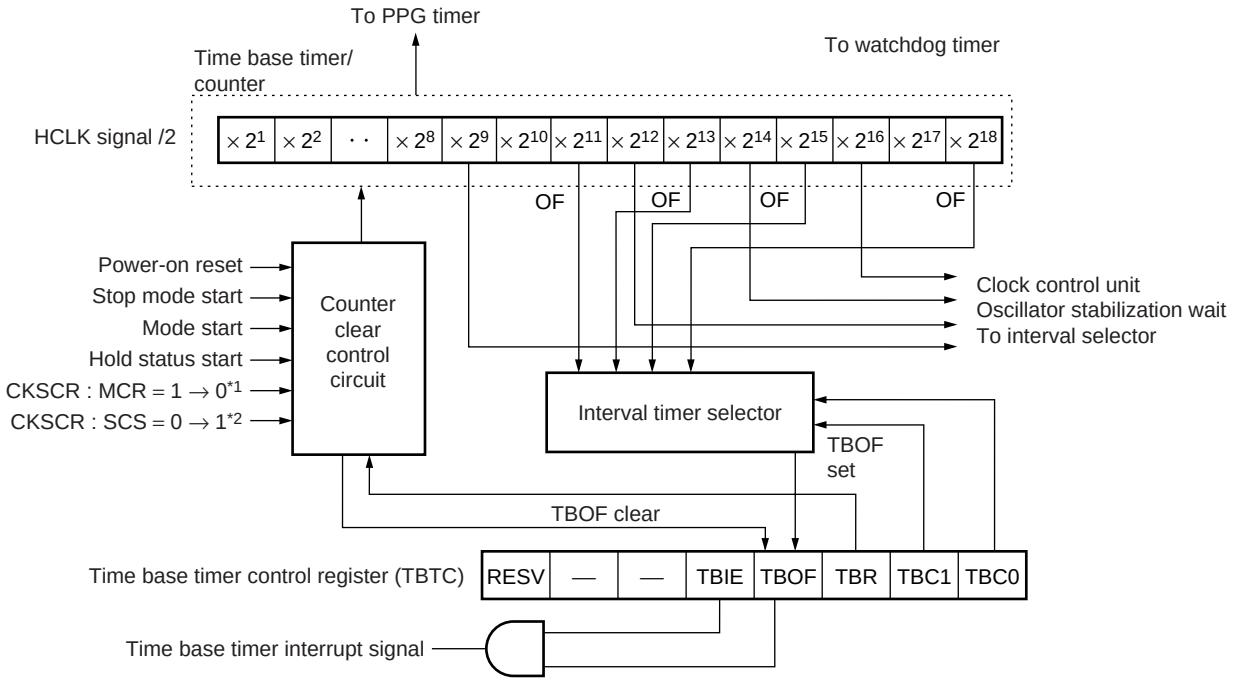
The time base timer is an 18-bit free-run timer that counts up in synchronization with the internal count clock (base oscillator divided by 2) . It functions as an interval timer with a selection of four types of time intervals. Other functions of this timer also include output of a timer signal for the oscillator stabilization wait time and an operating clock signal for the watchdog timer.

(1) Register List

Time base timer control register (TBTC)

	15	14	13	12	11	10	9	8
0000A9H	RESV	—	—	TBIE	TBOF	TBR	TBC1	TBC0
	(R/W) (1)	(—) (X)	(—) (X)	(R/W) (0)	(R/W) (0)	(W) (1)	(R/W) (0)	(R/W) (0)

(2) Block Diagram



— : Not used
OF : Overflow
HCLK : Oscillator clock
*1 : Switches machine clock from main clock or sub-clock to PLL clock.
*2 : Switches machine clock from sub-clock to main clock.

16. Clock

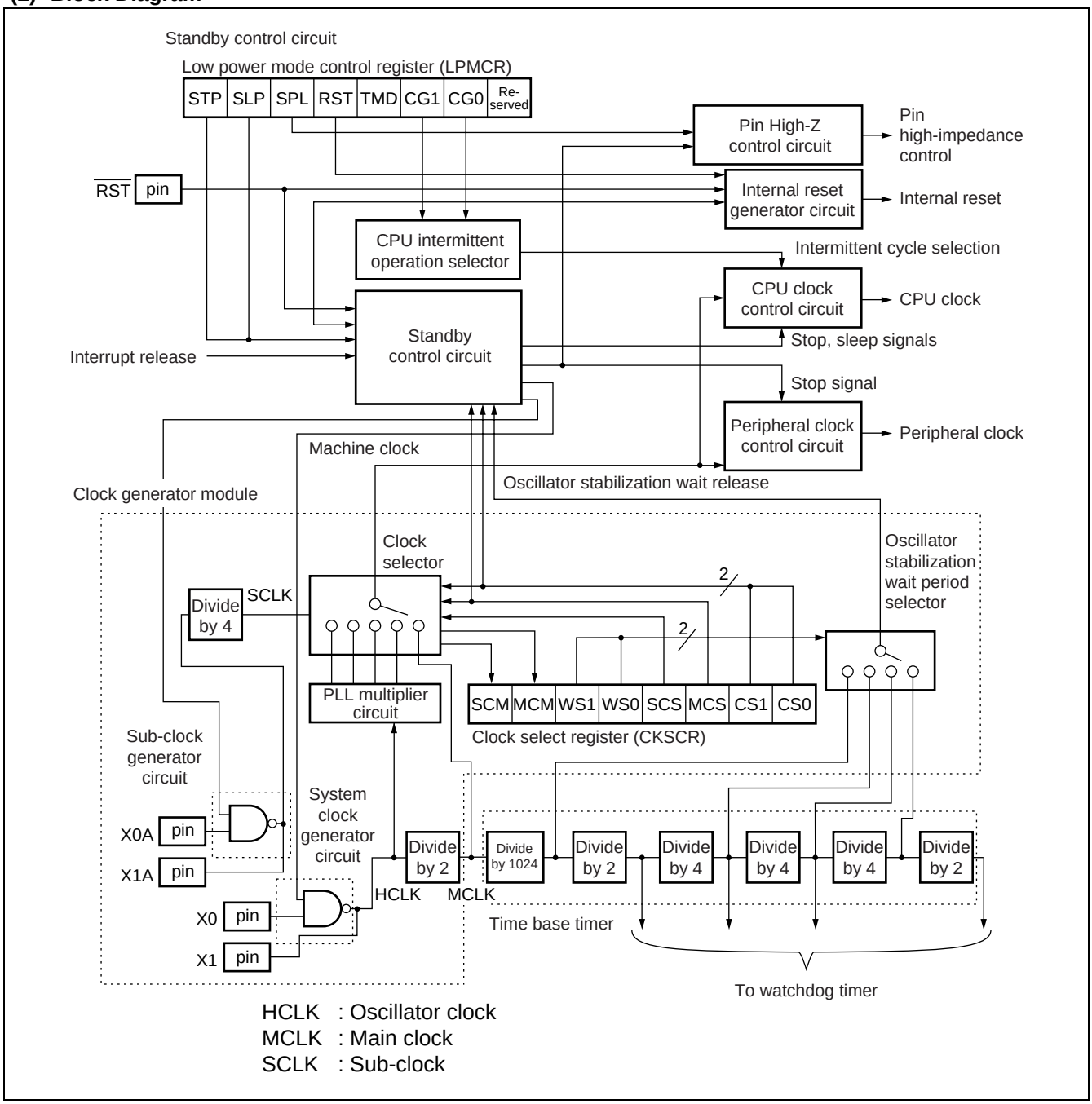
The clock generator module controls the operation of the internal clocks that produce the operating clock signals for the CPU and peripheral devices. This internal clock signal is called the machine clock, and one period is called a machine cycle. The clock signal from the base oscillator is called the oscillator clock, and the clock signal generated by the internal PLL module is called the PLL clock.

(1) Register List

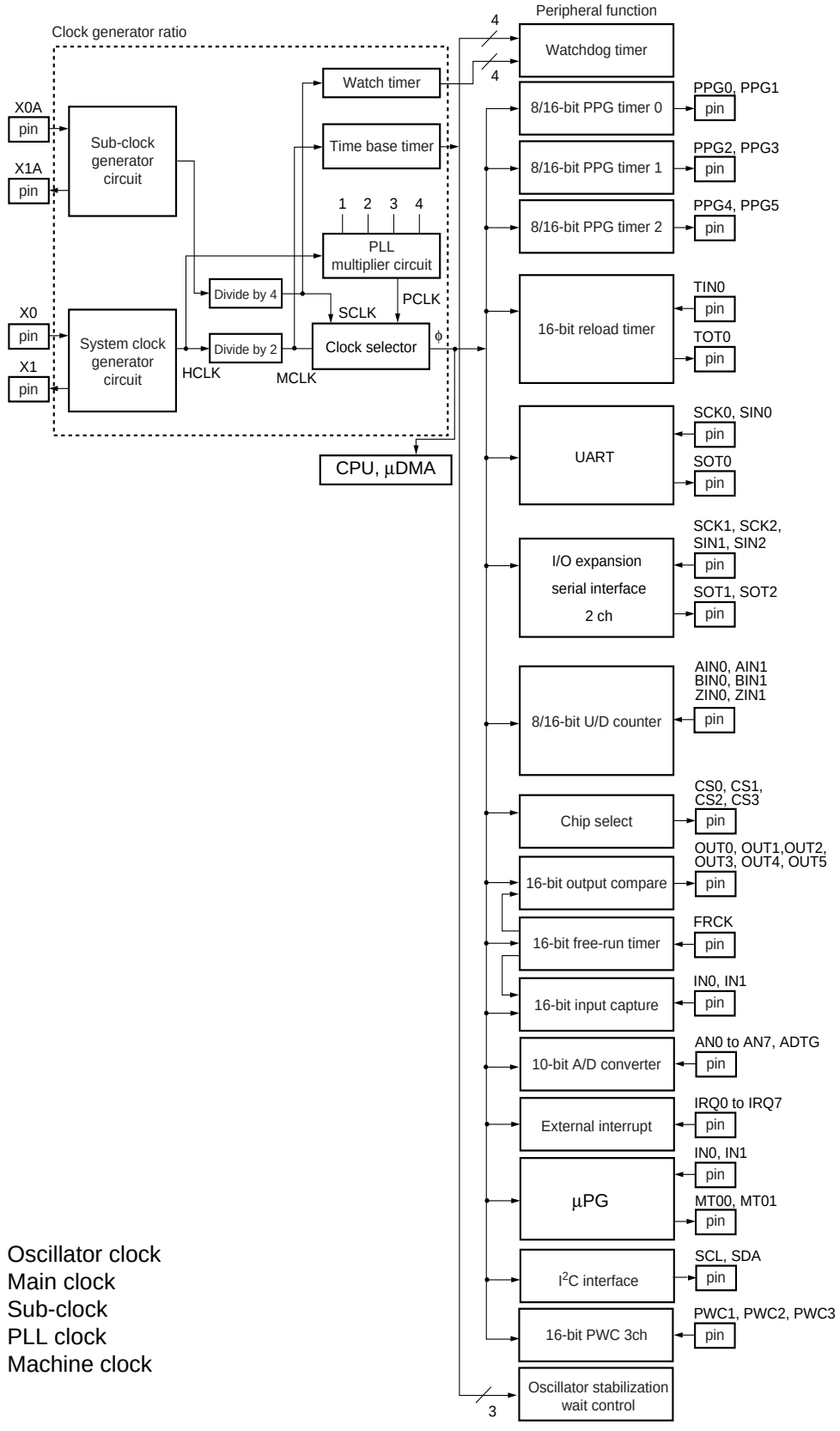
Clock select register (CKSCR)

	15	14	13	12	11	10	9	8	
0000A1H	SCM	MCM	WS1	WS0	SCS	MCS	CS1	CS0	
	(R) (1)	(R) (1)	(R/W) (1)	(R/W) (1)	(R/W) (1)	(R/W) (1)	(R/W) (0)	(R/W) (0)	Default value

(2) Block Diagram



(3) Clock Signal Supply Map



HCLK : Oscillator clock
MCLK : Main clock
SCLK : Sub-clock
PCLK : PLL clock
ϕ : Machine clock

17. Low Power Modes

The MB90470 series uses a selection of operating clock signals and clock operation controls to provide the following CPU operating modes.

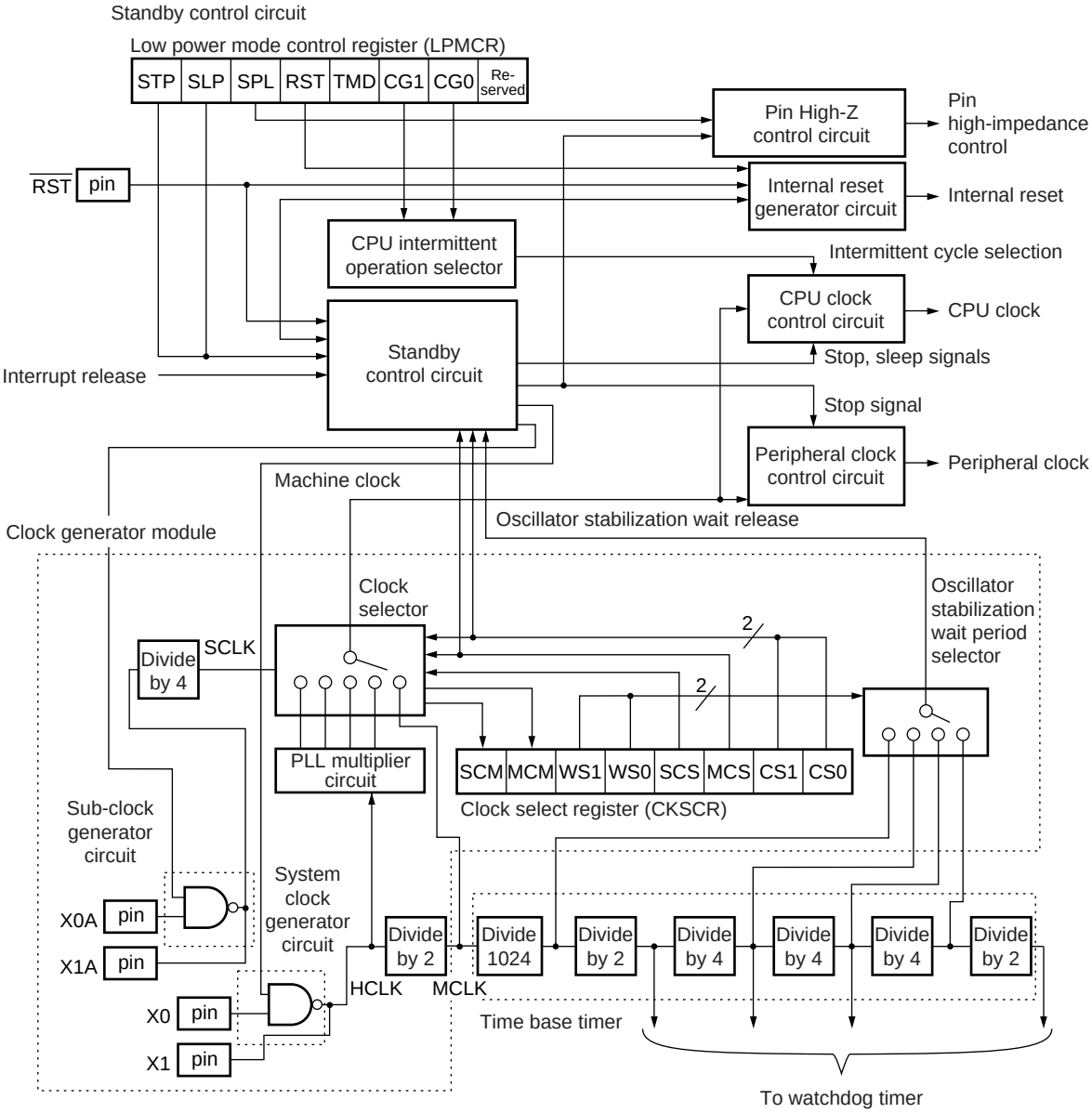
- Clock modes
  (PLL clock mode, main clock mode, sub-clock mode)
- CPU intermittent operation modes
  (PLL clock intermittent operation mode, main clock intermittent operation mode, sub-clock intermittent operation mode)
- Standby mode
  (Sleep mode, time base timer mode, stop mode, watch mode)

(1) Register List

Low power mode control register (LPMCR)

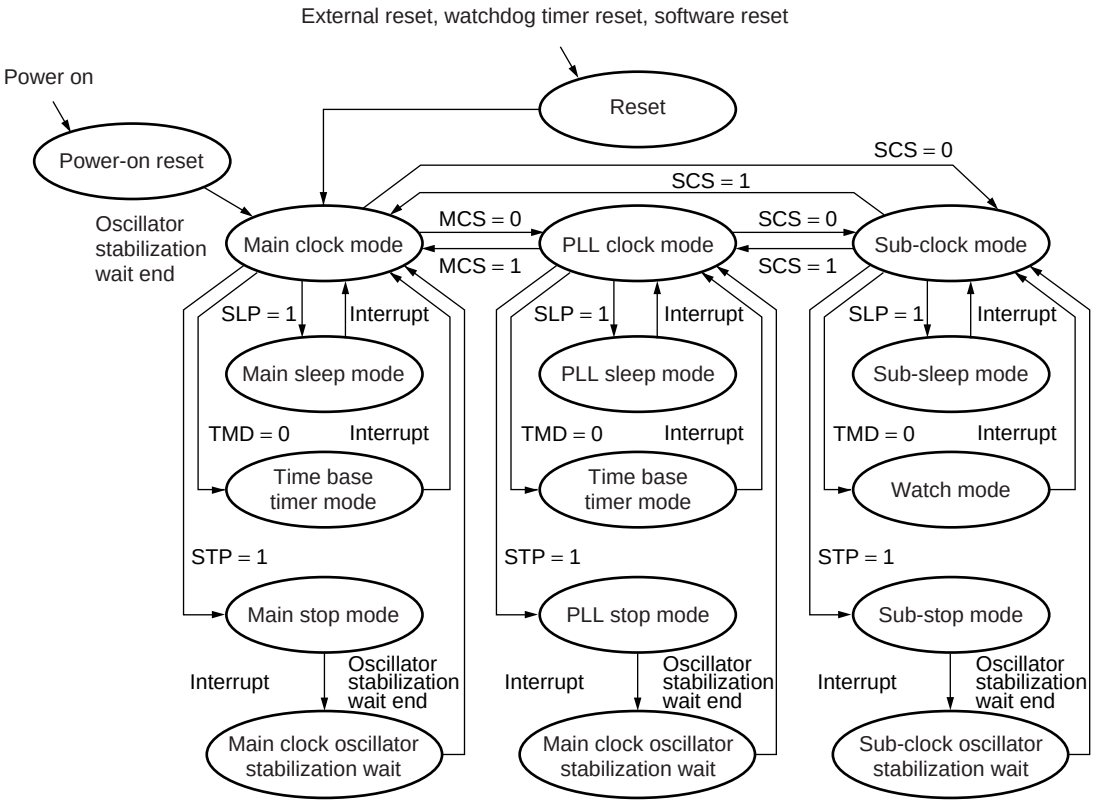
	7	6	5	4	3	2	1	0	
0000A0$_H$	STP	SLP	SPL	RST	TMD	CG1	CG0	Reserved	
	(W)	(W)	(R/W)	(W)	(R/W)	(R/W)	(R/W)	(R/W)	
	(0)	(0)	(0)	(1)	(1)	(0)	(0)	(0)	Default value

(2) Block Diagram



HCLK : Oscillator clock
MCLK : Main clock
SCLK : Sub-clock

(3) Status Transition Chart



18. Overview of the Chip Select Function

This module issues chip select signals in order to facilitate connection to external memory. There are four chip select output pins, with hardware areas set using a register for each output, so that the select signal is output from the related pin whenever access to an external address is detected.

- **Features of the chip select function**

The chip select function has two 8-bit registers for settings for each of the four output pins. One register (CARx) is used to specify the upper 8 bits of the address for match detection, thereby providing memory area detection in 64 KB units. The other register (CMRx) can be set to detect areas larger than 64 KB by masking bits in the match detection value.

Note that the CS output is set to high impedance during a bus hold condition.

(1) Register List

15 8	7 0	
CAR0	CMR0	(R/W)
CAR1	CMR1	(R/W)
CAR2	CMR2	(R/W)
CAR3	CMR3	(R/W)
CALR	CSCR	(R/W)

Chip select area MASK register (CMRx)

	7	6	5	4	3	2	1	0	
0000C0H 0000C2H 0000C4H 0000C6H	M7	M6	M5	M4	M3	M2	M1	M0	
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	Read/write
	(0)	(0)	(0)	(0)	(1)	(1)	(1)	(1)	Default value

Chip select area register (CARx)

	15	14	13	12	11	10	9	8	
0000C1H 0000C3H 0000C5H 0000C7H	A7	A6	A5	A4	A3	A2	A1	A0	
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	Read/write
	(1)	(1)	(1)	(1)	(1)	(1)	(1)	(1)	Default value

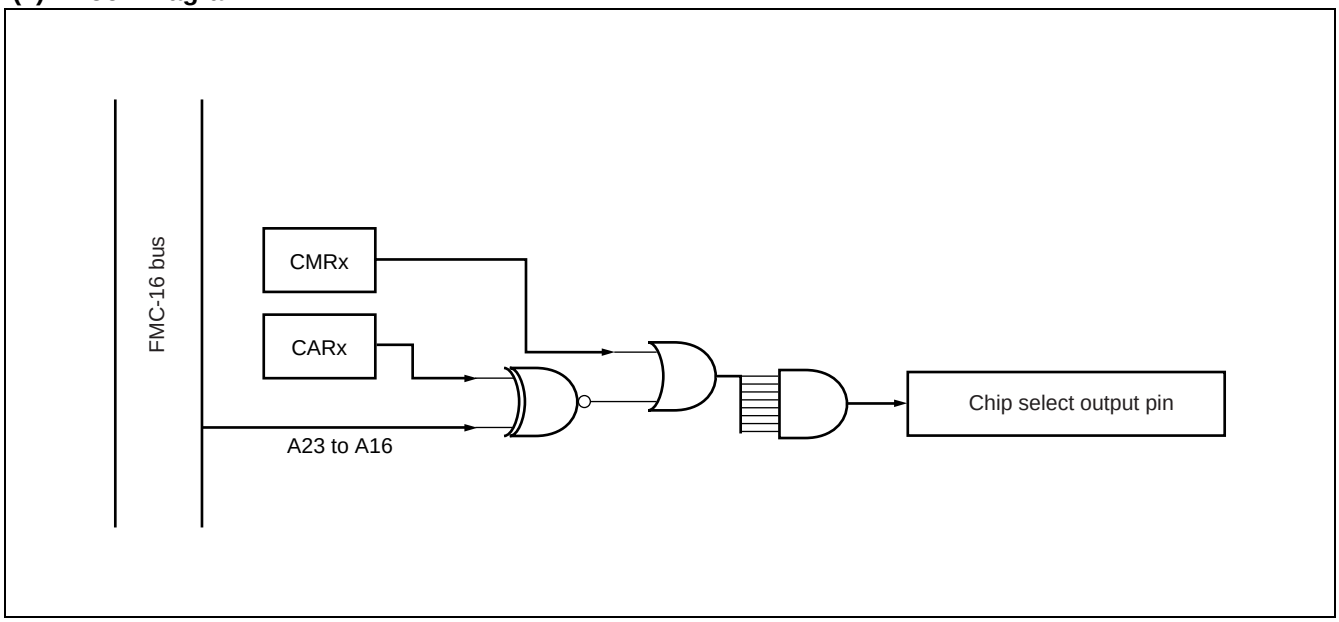
Chip select control register (CSCR)

	7	6	5	4	3	2	1	0	
0000C8H	—	—	—	—	OPL3	OPL2	OPL1	OPL0	
	(—)	(—)	(—)	(—)	(R/W)	(R/W)	(R/W)	(R/W)	Read/write
	(—)	(—)	(—)	(—)	(0)	(0)	(0)	(*)	Default value

Chip selector active level register (CALR)

	15	14	13	12	11	10	9	8	
0000C9H	—	—	—	—	ACTL3	ACTL2	ACTL1	ACTL0	
	(—)	(—)	(—)	(—)	(R/W)	(R/W)	(R/W)	(R/W)	
	(—)	(—)	(—)	(—)	(0)	(0)	(0)	(0)	Default value

(2) Block Diagram



19. ROM Mirror Function Select Module

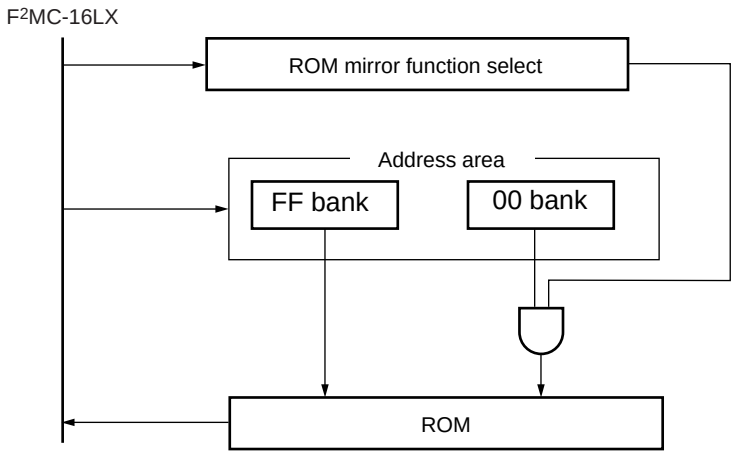
The ROM mirror function select module provides a register selection that allows the FF bank in ROM to be viewed in the 00 bank.

(1) Register List

	bit	15	14	13	12	11	10	9	8	Default value
ROMM Address : 00006F$_H$		—	—	—	—	—	—	—	MI	-------1$_B$
									W	

W : Write only
- : Not used

(2) Block Diagram



Note : Do not access this register during operations to address 004000$_H$ to 00FFFF$_H$.

20. Interrupt Controller

The interrupt control registers are located in the interrupt controller. An interrupt control register is provided for each I/O with an interrupt function. The registers have the following functions.

- Set the interrupt level of the corresponding peripheral.

(1) Register List

Interrupt control register

Address: ICR01: 0000B1H, ICR03: 0000B3H, ICR05: 0000B5H, ICR07: 0000B7H, ICR09: 0000B9H, ICR11: 0000BBH, ICR13: 0000BDH, ICR15: 0000BFH

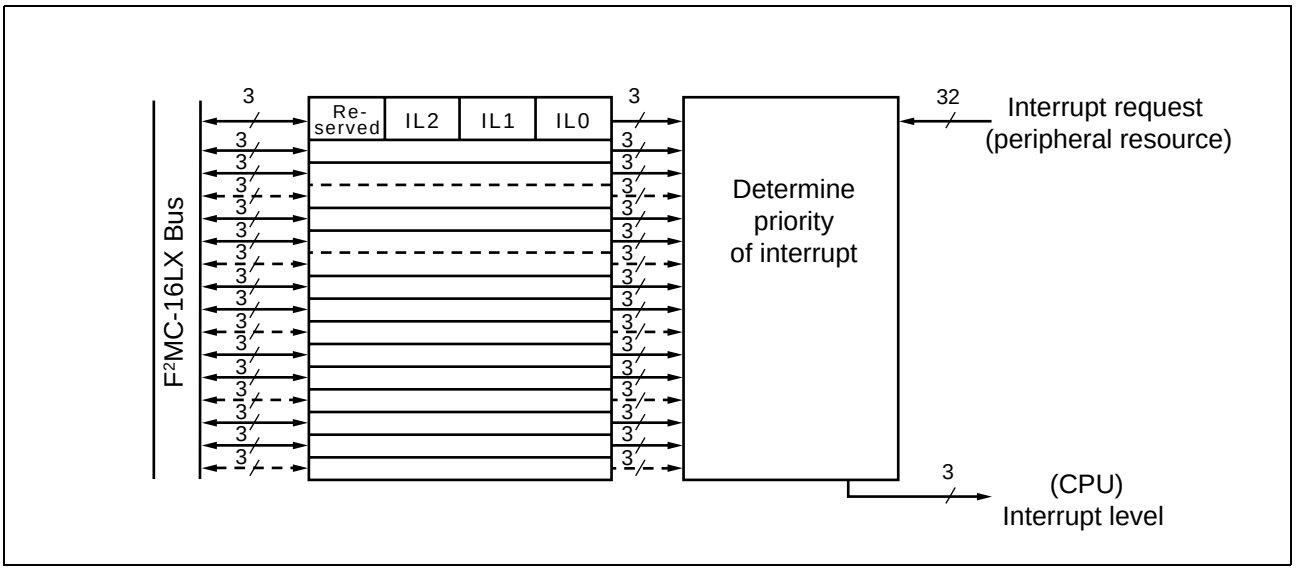
bit	15	14	13	12	11	10	9	8	
	-	-	-	-	Reserved	IL2	IL1	IL0	ICR01, 03, 05, 07, 09, 11, 13, 15
Read/Write→	(W)	(W)	(W)	(W)	(R/W)	(R/W)	(R/W)	(R/W)	
Initial value→	(0)	(0)	(0)	(0)	(0)	(1)	(1)	(1)	

Address: ICR00: 0000B0H, ICR02: 0000B2H, ICR04: 0000B4H, ICR06: 0000B6H, ICR08: 0000B8H, ICR14: 0000BEH

bit	15	14	13	12	11	10	9	8	
	-	-	-	-	Reserved	IL2	IL1	IL0	ICR00, 02, 04, 26, 08, 10, 12, 14
Read/Write→	(W)	(W)	(W)	(W)	(R/W)	(R/W)	(R/W)	(R/W)	
Initial value→	(0)	(0)	(0)	(0)	(0)	(1)	(1)	(1)	

Note : Do not access these registers using read-modify-write instructions as this can cause misoperation.

(2) Block Diagram



21. μDMA

μDMA is the simplified DMA which has the equivalent function to EI^{2}OS function μDMA has DMA transfer channel which consists of 16 channels and has the following functions.

- Automatic data transfer between peripheral resources (I/O) and memory.
- CPU program executing stops dring DMA operation.
- Selectable for address transfer increase/decrease .
- DMA transfer control is done at DMA enable register, DMA stop status register, DMA status register and descriptor.
- Stop request stops DMA transfer from resources.
- After DMA transfer, flag is set to bit corresponding to DMA status register transfer stop channel and stop interrupt is output to interrupt controller.

(1) Register List

DMA enable register

bit	15	14	13	12	11	10	9	8	Initial value
DERH : 0000AD$_H$	EN15	EN14	EN13	EN12	EN11	EN10	EN9	EN8	0 0 0 0 0 0 0 0$_B$
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

DMA enable register

bit	7	6	5	4	3	2	1	0	Initial value
DERL : 0000AC$_H$	EN7	EN6	EN5	EN4	EN3	EN2	EN1	EN0	0 0 0 0 0 0 0 0$_B$
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

DMA stop status register

bit	7	6	5	4	3	2	1	0	Initial value
DSSR : 0000A4$_H$	STP7	STP6	STP5	STP4	STP3	STP2	STP1	STP0	0 0 0 0 0 0 0 0$_B$
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

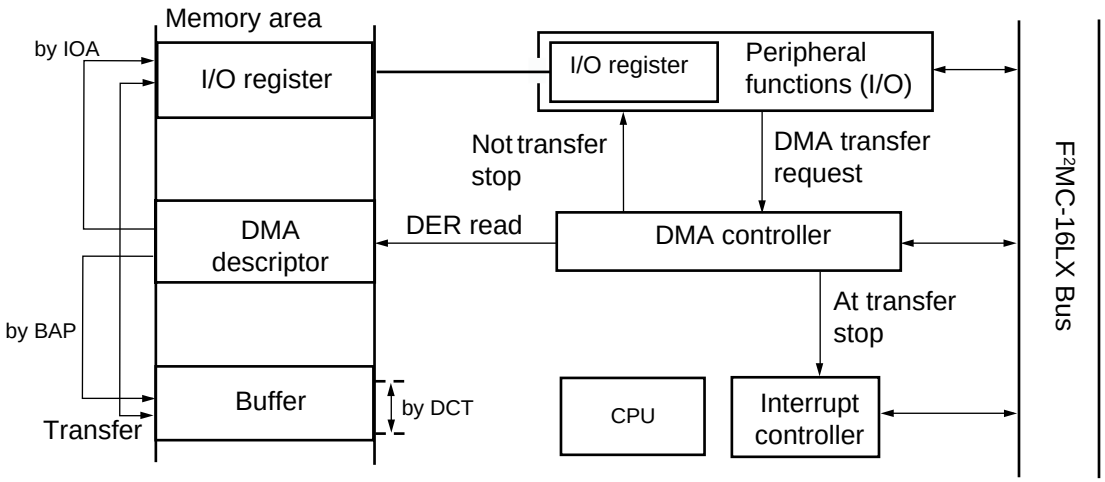
DMA status register

bit	15	14	13	12	11	10	9	8	Initial value
DSRH : 00009D$_H$	DE15	DE14	DE13	DE12	DE11	DE10	DE9	DE8	0 0 0 0 0 0 0 0$_B$
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

DMA status register

bit	7	6	5	4	3	2	1	0	Initial value
DSRL : 00009C$_H$	DE7	DE6	DE5	DE4	DE3	DE2	DE1	DE0	0 0 0 0 0 0 0 0$_B$
	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	

(2) Block Diagram



IOA : Address pointer
BAP : Buffer address pointer
DER : DMA enable register (ENx selection is done.)
DTC : Data counter

22. External Bus Pin Control Circuit

The external bus pin control circuit controls the external bus pins used to expand the CPU address/data bus connections to external circuits.

(1) Register List

- Auto ready function select register (ARSR)

Address : 0000A5H

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
ICR1	ICR0	HMR1	HMR0	—	—	LMR1	LMR0
W	W	W	W	—	—	W	W

Initial value 0011- - 00B

- External address output control register (HACR)

Address : 0000A6H

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
E23	E22	E21	E20	E19	E18	E17	E16
W	W	W	W	W	W	W	W

Initial value 00000000B

- Bus control signal select register (EPCR)

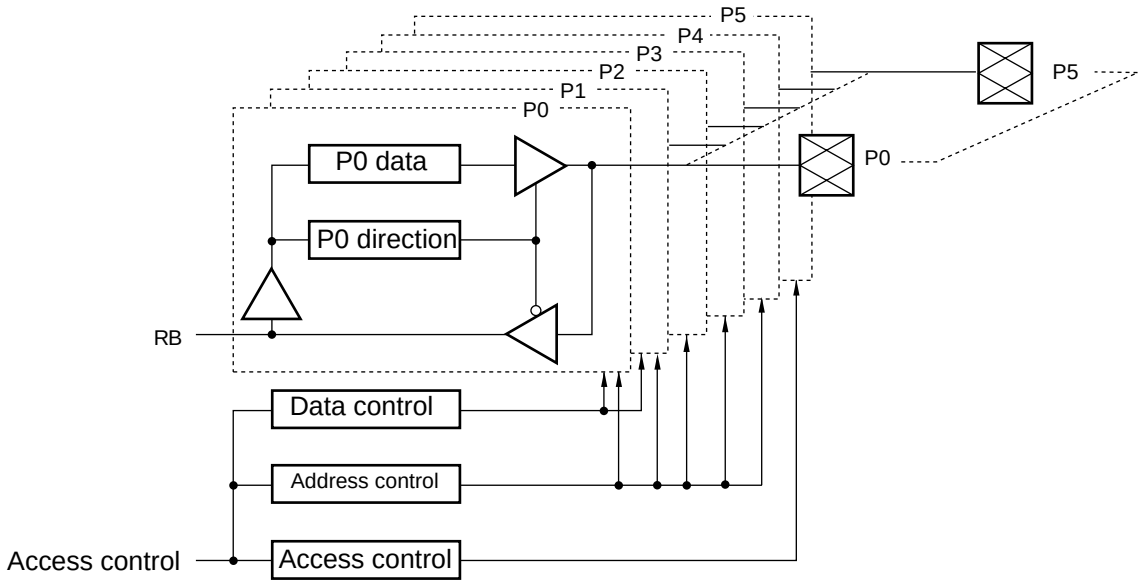
Address : 0000A7H

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
CKE	RYE	HDE	ICBS	HMBS	WRE	LMBS	—
W	W	W	W	W	W	W	—

Initial value 1000∗10 -B

W : Write only
– : Not used
* : May be either “1” or “0”

(2) Block Diagram



23. Address Match Detection Function

When the address is equal to a value set in the address detection register, the instruction code loaded into the CPU is replaced forcibly with the INT9 instruction code (01H). As a result, when the CPU executes a set instruction, the INT9 instruction is executed. Processing by the INT#9 interrupt routine allows the program patching function to be implemented.

Two address detection registers are supported. An interrupt enable bit is prepared for each register. If the value set in the address detection register matches an address and if the interrupt enable bit is set at “1”, the instruction code loaded into the CPU is replaced forcibly with the INT9 instruction code.

(1) Register Configuration

- Program address detection register 0 to 2 (PADR0)

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
PADR0 (Low order address): 001FF0H									XXXXXXXXB
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
PADR0 (Middle order address): 001FF1H									XXXXXXXXB
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
PADR0 (High order address): 001FF2H									XXXXXXXXB
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- Program address detection register 3 to 5 (PADR1)

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
PADR1 (Low order address): 001FF3H									XXXXXXXXB
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
PADR1 (Middle order address): 001FF4H									XXXXXXXXB
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

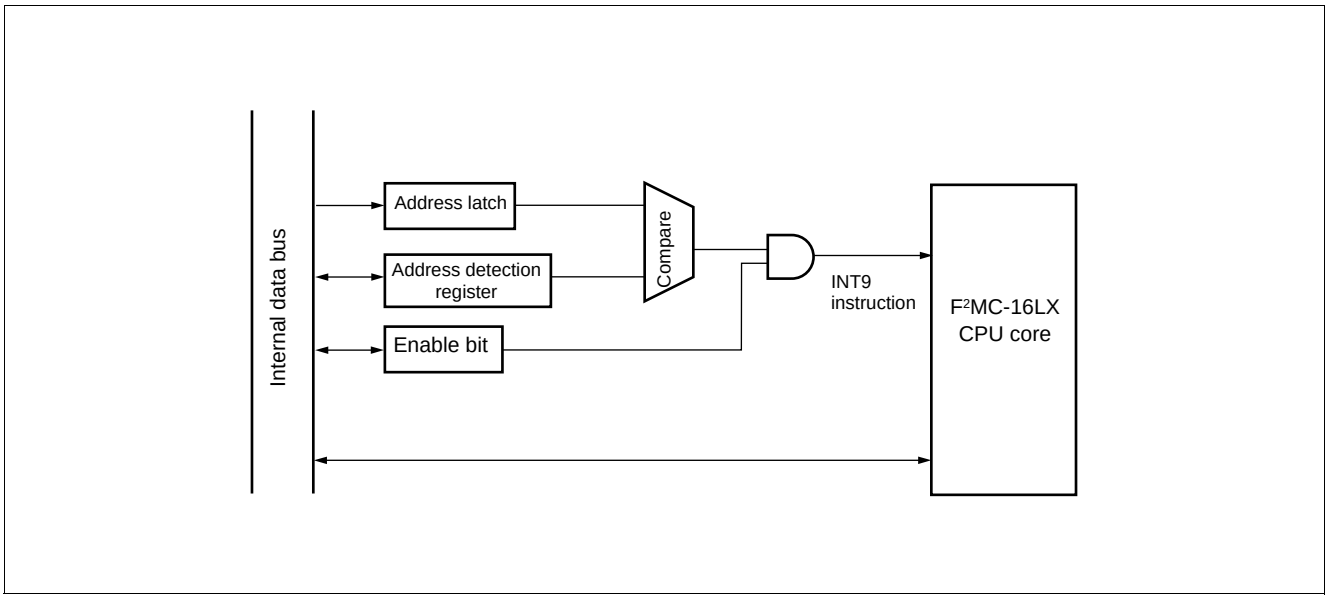
Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
PADR1 (High order address): 001FF5H									XXXXXXXXB
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- Program address detection control status register (PACSR)

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
00009EH	RESV	RESV	RESV	RESV	AD1E	RESV	AD0E	RESV	00000000B
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

R/W :Readable and writable
X :Undefined
RESV:Reserved bit

(2) Block Diagram



■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

(V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Supply voltage	$V_{CC}3$	V_{SS} – 0.3	V_{SS} + 4.0	V	
	$V_{CC}5$	V_{SS} – 0.3	V_{SS} + 7.0	V	
	AV_{CC}	V_{SS} – 0.3	V_{SS} + 4.0	V	*1
	AVRH	V_{SS} – 0.3	V_{SS} + 4.0	V	
Input voltage	V_I	V_{SS} – 0.3	V_{SS} + 4.0	V	*2
		V_{SS} – 0.3	V_{SS} + 7.0	V	*2
Output voltage	V_O	V_{SS} – 0.3	V_{SS} + 4.0	V	*2
		V_{SS} – 0.3	V_{SS} + 7.0	V	*2
Maximum clamp current	I_{CLAMP}	– 2.0	+ 2.0	mA	*6
Total maximum clump current	$\Sigma\lvert I_{CLAMP} \rvert$	—	20	mA	*6
“L” level maximum output current	I_{OL}	—	10	mA	*3
“L” level average output current	I_{OLAV}	—	3	mA	*4
“L” level maximum total output current	ΣI_{OL}	—	60	mA	
“L” level average total output current	ΣI_{OLAV}	—	30	mA	*5
“H” level maximum output current	I_{OH}	—	– 10	mA	*3
“H” level average output current	I_{OHAV}	—	– 3	mA	*4
“H” level maximum total output current	ΣI_{OH}	—	– 60	mA	
“H” level average total output current	ΣI_{OHAV}	—	–30	mA	*5
Power consumption	P_D	—	410	mW	
Operating temperature	T_A	– 40	+ 85	°C	
Storage temperature	Tstg	– 55	+ 150	°C	

*1: AV_{CC} and AVRH must not exceed $V_{CC}3$. Also, AVRH must not exceed AV_{CC} ,too.

*2: V_I, and V_O must not exceed V_{CC} (including $V_{CC}3$, $V_{CC}5$) plus 0.3 V.

*3: Maximum output current is defined as the peak value at one corresponding pin.

*4: Average output current is defined as the average current flowing through one corresponding pin in an interval of 100 ms.

*5: Average total output current is defined as the total average current flowing through all corresponding pins in an interval of 100 ms.

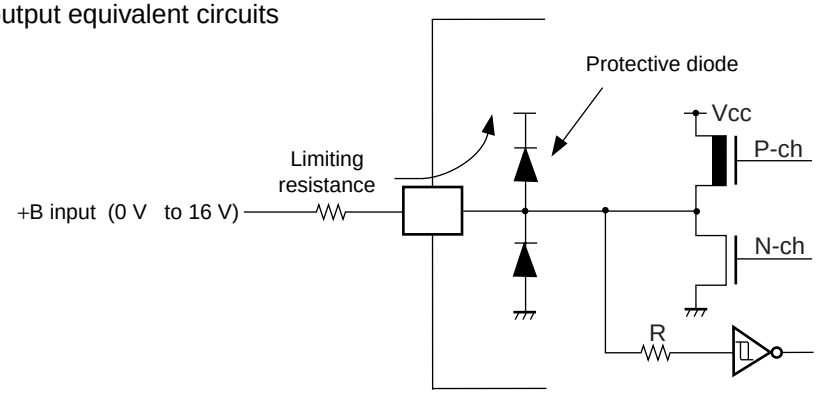
*6:
- Applicable to pins: General purpose CMOS input port (P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, PA0 to PA3)
- Use within recommended operating conditions.
- Use at DC voltage (current)
- The +B signal should always be applied a limiting resistance placed between the +B signal and the microcontroller.

(Continued)

(Continued)

- The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the V_{CC} pin, and this may affect other devices.
- Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V) , the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the power-on reset.
- Care must be taken not to leave the +B input pin open.
- Sample recommended circuits:

- Input/output equivalent circuits



WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Operating Conditions

(V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Supply voltage	$V_{CC}3$*	1.8	3.6	V	MASK version
		2.4	3.6	V	Low voltage FLASH version
		3.0	3.6	V	High speed FLASH version
	$V_{CC}5$*	1.8	5.5	V	MASK version
		2.4	5.5	V	Low voltage FLASH version
		3.0	5.5	V	High speed FLASH version
	$V_{CC}3$	1.8	3.6	V	Hold stop status
	$V_{CC}5$	1.8	5.5	V	Hold stop status (MASK version)
		1.8	5.5	V	Hold stop status (FLASH version)
"H" level input voltage	V_{IH}	0.7 V_{CC}	V_{CC} + 0.3	V	All pins other than V_{HIS}, V_{IHM} pins
	V_{IHS}	0.8 V_{CC}	V_{CC} + 0.3	V	Hysteresis input pins
	V_{IHM}	V_{CC} – 0.3	V_{CC} + 0.3	V	MD pin input
"L" level input voltage	V_{IL}	V_{SS} – 0.3	0.3 V_{CC}	V	All pins other than V_{ILS}, V_{ILM} pins
	V_{ILS}	V_{SS} – 0.3	0.2 V_{CC}	V	Hysteresis input pins
	V_{ILM}	V_{SS} – 0.3	V_{SS} + 0.3	V	MD pin input
Operating temperature	T_A	– 40	+ 85	°C	

* : Pay attention to operating frequency.

Note : When using I^2C functions, the voltage should be at least 2.4 V.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

3. DC Characteristics

(MASK version : V_{CC} = 1.8 V to 3.6 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C) *
(Low voltage FLASH version : V_{CC} = 2.4 V to 3.6 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C) *
(High speed FLASH version : V_{CC} = 3.0 V to 3.6 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C) *

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level output voltage	V_{OH}	All pins except P76-P77	V_{CC} = 2.7 V I_{OH} = – 1.6 mA	V_{CC}3 – 0.3	—	—	V	
			V_{CC} = 4.5 V I_{OH} = – 4.0 mA	V_{CC}5 – 0.5	—	—	V	Using 5 V system power supply
"L" level output voltage	V_{OL}	All output pins	V_{CC} = 2.7 V I_{OL} = 2.0 mA	—	—	0.4	V	
			V_{CC} = 4.5 V I_{OL} = 4.0 mA	—	—	0.4	V	Using 5 V system power supply
Input leak current	I_{IL}	All pins except P76, P77	V_{CC} = 3.3 V $V_{SS} < V_I < V_{CC}$	– 10	—	+ 10	µA	
Pull-up resistance	R_{PULL}	—	V_{CC} = 3.0 V, at T_A = + 25 °C	20	65	200	kΩ	
Open drain output current	I_{leak}	P40 to P47, P70 to P77	—	—	0.1	10	µA	
Supply current	I_{CC}	—	at V_{CC} = 3.3 V, at normal internal 20 MHz operation	—	60	80	mA	MASK version
				—	65	85	mA	MASK version (A/D operation)
				—	51	66	mA	FLASH version
				—	56	71.5	mA	FLASH version (A/D operation)
			at V_{CC} = 3.3 V, flash write/erase at internal 20 MHz	—	57	71.5	mA	FLASH version
	I_{CCS}	—	V_{CC} = 3.3 V, sleep mode at 20 MHz	—	18	33	mA	
	I_{CCL}	—	at V_{CC} = 3.3 V, sub operation, external 32 kHz, internal 8 kHz operation (T_A = + 25 °C)	—	16	140	µA	

* : Pay attention to operating frequency.

(Continued)

(Continued)

(MASK version : V_{CC} = 1.8 V to 3.6 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C) *
(Low voltage FLASH version : V_{CC} = 2.4 V to 3.6 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C) *
(High speed FLASH version : V_{CC} = 3.0 V to 3.6 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C) *

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Supply current	I_{CCT}	—	at V_{CC} = 3.3 V, watch operation, external 32 kHz, internal 8 kHz operation (T_A = + 25 °C)	—	10	40	µA	MASK version
				—	15	40	µA	FLASH version
	I_{CCH}	—	T_A = + 25 °C, stop mode, at V_{CC} = 3.3 V	—	0.1	20	µA	MASK version
				—	0.2	40	µA	FLASH version
Input capacitance	C_{IN}	All pins except AV_{CC}, AV_{SS}, V_{CC}, V_{SS}	—	—	5	15	pF	

* : Pay attention to operating frequency.

Notes :
- Pins P40-P47 and P70-P75 are N-ch open drain pins with controls, and normally used at CMOS level.
- P76 and P77 are N-ch open drain pins.
- $V_{CC} = V_{CC}3 = V_{CC}5$.
- When using two power supplies, the 5 V system pins are P20 to P27, P30 to P37, P40 to P47 and P70 to P77. All other pins are 3 V input/output pins.

4. AC Characteristics

(1) Clock Timing Ratings

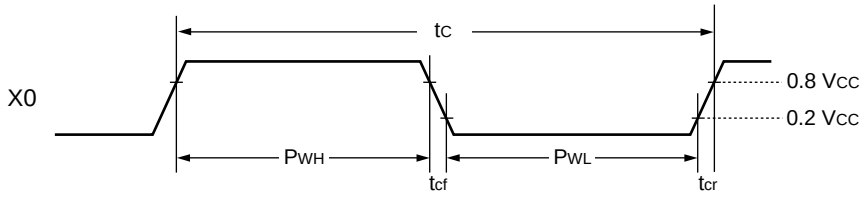
(V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Clock frequency	F_{CH}	X0, X1	—	3	—	20	MHz	for crystal oscillation*2
				3	—	40		for external clock
	F_{CL}	X0A, X1A	—	—	32.768	—	kHz	
Clock cycle time	t_C	X0, X1	—	25	—	333	ns	*2
	t_{CL}	X0A, X1A	—	—	30.5	—	µs	
Input clock pulse width	P_{WH} P_{WL}	X0	—	5	—	—	ns	*1
	P_{WLH} P_{WLL}	X0A	—	—	15.2	—	µs	*1
Input clock rise, fall time	t_{cr} t_{cf}	X0	—	—	—	5	ns	Using external clock
Internal operating clock frequency	f_{CP}	—	—	1.5	—	20	MHz	*2
		—	—	1.5	—	16	MHz	MB90474 only
	f_{CPL}	—	—	—	8.192	—	kHz	
				3	—	20	MHz	MB90F474H
				3	—	12	MHz	MB90F474L
Internal operating clock cycle time	t_{CP}	—	—	50.0	—	666	ns	*2
		—	—	62.5	—	666	ns	MB90474 only
	t_{CPL}	—	—	—	122.1	—	µs	

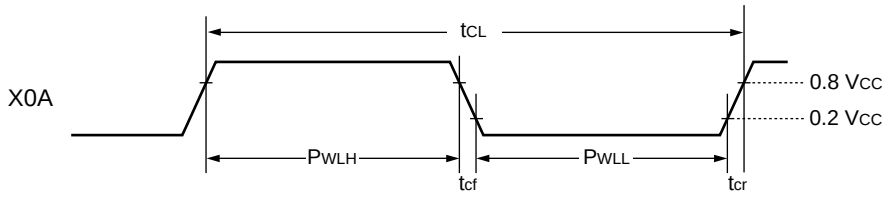
*1 : $V_{CC} = V_{CC}3 = V_{CC}5$

*2 : Observe the operating voltage with care.

- **X0**, **X1 clock timing**

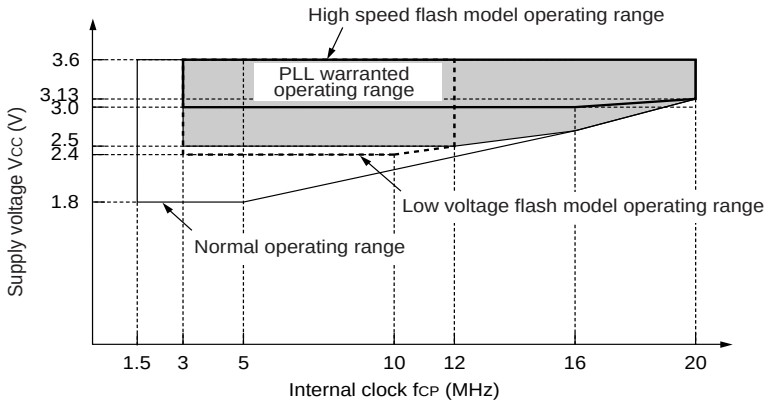


- **X0A**, **X1A clock timing**



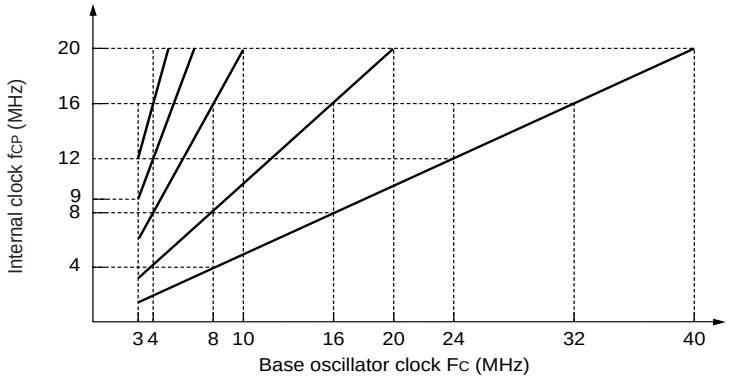
- **PLL warranted operating range**

Internal operating clock frequency vs. Supply voltage



Note : Use it at f = 16 MHz for MB90474.
When using the high speed flash model at f = 20 MHz, use supply voltages of 3.13 V to 3.6 V.
For A/D operating frequencies, see the electrical characteristics of the A/D converter module.
Maximum assured operation frequency (f_{cp}) of µDMA is 16 MHz.

Base oscillator frequency vs. Internal operating clock frequency

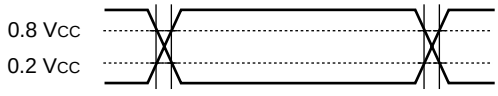


Note : Use PLL circuit when using internal clock at 16 MHz or more. It is recommended to use base oscillator clock of up to 20 MHz.

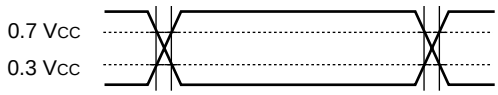
AC characteristics are determined using the following measurement reference voltage values.

- **Input signal waveform**

Hysteresis input pins

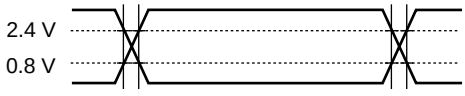


Pins other than hysteresis input/MD input pins



- **Output signal waveform**

Output pins

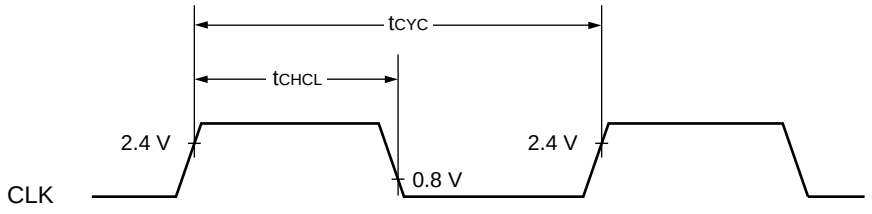


(2) Clock Output Timing

(V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Cycle time	t_{CYC}	CLK	—	t_{CP}	—	ns	
CLK ↑→ to CLK ↓	t_{CHCL}	CLK	V_{CC} = 3.0 V to 3.6 V	t_{CP} / 2 – 15	t_{CP} / 2 + 15	ns	at f_{cp} = 20 MHz
			V_{CC} = 2.7 V to 3.3 V	t_{CP} / 2 – 20	t_{CP} / 2 + 20	ns	at f_{cp} = 16 MHz
			V_{CC} = 2.7 V to 3.3 V	t_{CP} / 2 – 64	t_{CP} / 2 + 64	ns	at f_{cp} = 5 MHz

Notes : • t_{CP} : See (1) Clock Timing Ratings.
• $V_{CC} = V_{CC}3 = V_{CC}5$



(3) Reset Input Ratings

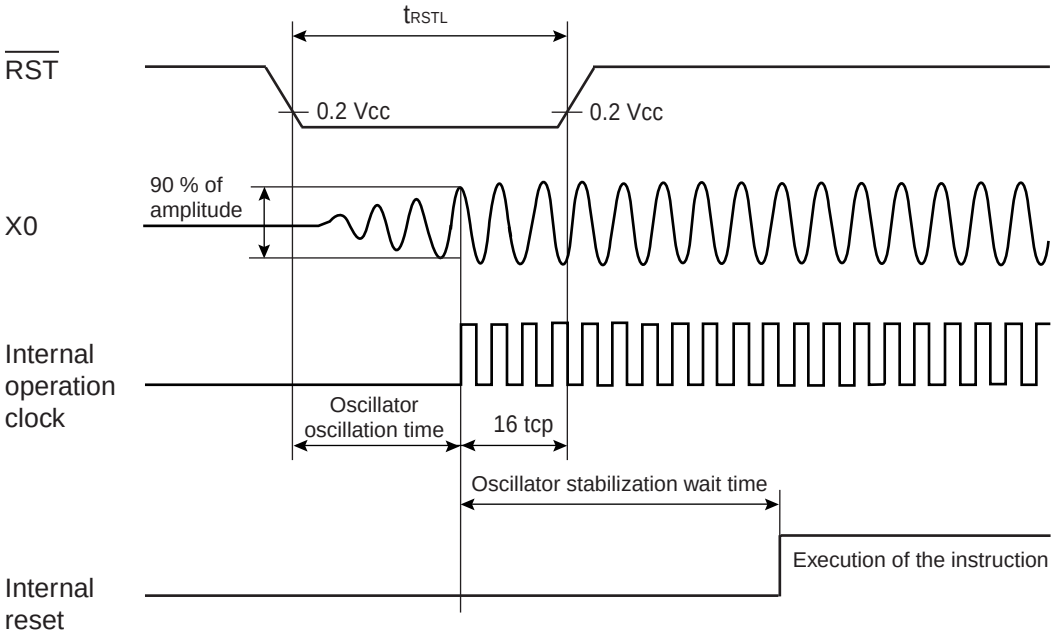
(V_{CC} = 2.7 V to 3.6 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Reset input time	t_{RSTL}	$\overline{RST}$	—	16 t_{CP}	—	ns	In normal operation
				Oscillator oscillation time* + 16 t_{CP}	—	ms	In stop mode

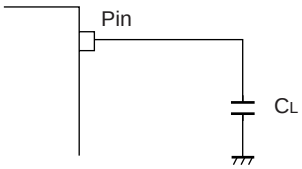
* : Oscillator oscillation time is the time to reach 90% amplitude. For a crystal oscillator, this is a few to several dozen ms; for a FAR/ceramic oscillator, this is several hundred µs to a few ms, and for an external clock this is 0 ms.

Note: t_{CP} : See (1) Clock Timing Ratings.

• In stop mode



• **Measurement conditions for AC ratings**



C_L : Load capacitance applied to pin during testing

CLK, ALE, C_L = 30 pF
AD15 to AD00 (Address, data bus) , $\overline{RD}$, $\overline{WR}$,
A23 to A00/D15 to D00 : C_L = 80 pF

(4) Power On Ratings (Power-on reset)

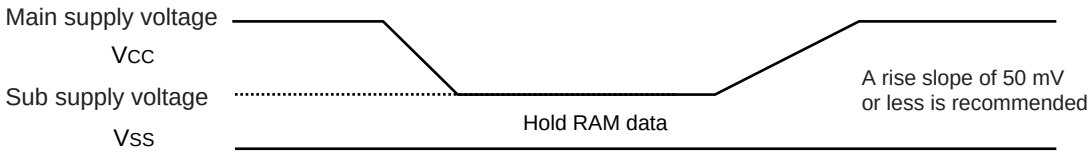
(V_{CC} = 2.7 V to 3.6 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Power rise time	t_R	V_{CC}	—	—	30	ms	*
Power cutoff time	t_{OFF}	V_{CC}		1	—	ms	For continuous operation

* : Power supply rise time requires V_{CC} < 0.2 V.

Notes : • $V_{CC} = V_{CC}3 = V_{CC}5$
- The above ratings are values for power-on reset.
- A power-on reset should be applied by restarting the power supply inside the device.

Extreme variations in supply voltage may activate a power-on reset. As the illustration shows below , when varying supply voltage during operation the use of a smooth voltage rise with suppressed fluctuation is recommended.

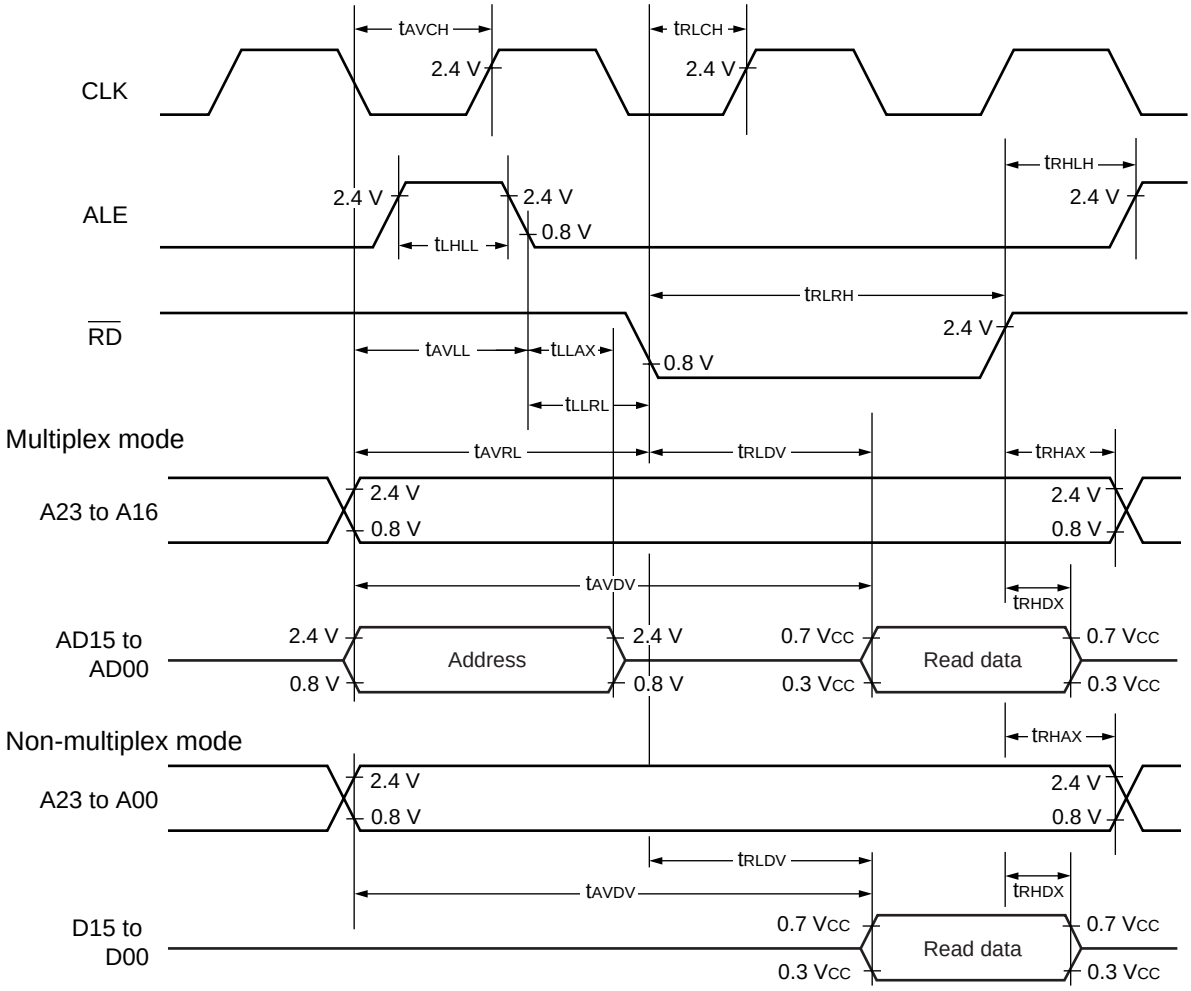


(5) Bus read timing

(V_{CC} = 2.7 V to 3.6 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
ALE pulse width	t_{LHLL}	ALE	—	t_{CP} / 2 – 15	—	ns	at f_{cp} = 20 MHz
				t_{CP} / 2 – 20	—	ns	at f_{cp} = 16 MHz
				t_{CP} / 2 – 35	—	ns	at f_{cp} = 8 MHz
Valid address → ALE ↓ time	t_{AVLL}	Address pins, ALE	—	t_{CP} / 2 – 20	—	ns	
				t_{CP} / 2 – 40	—	ns	at f_{cp} = 8 MHz
ALE ↓ → address valid time	t_{LLAX}	ALE, Address pins	—	t_{CP} / 2 – 15	—	ns	
Valid address → $\overline{RD}$ ↓ time	t_{AVRL}	$\overline{RD}$, address	—	t_{CP} – 20	—	ns	
Valid address → valid data input	t_{AVDV}	Address/data	—	—	5 t_{CP} / 2 – 60	ns	
				—	5 t_{CP} / 2 – 80	ns	at f_{cp} = 8 MHz
$\overline{RD}$ pulse width	t_{RLRH}	$\overline{RD}$	—	3 t_{CP} / 2 – 25	—	ns	at f_{cp} = 20 MHz
				3 t_{CP} / 2 – 20	—	ns	at f_{cp} = 16 MHz
$\overline{RD}$ ↓ → valid data input	t_{RLDV}	$\overline{RD}$, Data	—	—	3 t_{CP} / 2 – 60	ns	
				—	3 t_{CP} / 2 – 80	ns	at f_{cp} = 8 MHz
$\overline{RD}$ ↑ → data hold time	t_{RHDX}	$\overline{RD}$, Data	—	0	—	ns	
$\overline{RD}$ ↑ → ALE ↑ time	t_{RHLH}	$\overline{RD}$, ALE	—	t_{CP} / 2 – 15	—	ns	
$\overline{RD}$ ↑ → address valid time	t_{RHAX}	Address, $\overline{RD}$	—	t_{CP} / 2 – 10	—	ns	
Valid address → CLK ↑ time	t_{AVCH}	Address, CLK	—	t_{CP} / 2 – 20	—	ns	
$\overline{RD}$ ↓ → CLK ↑ time	t_{RLCH}	$\overline{RD}$, CLK	—	t_{CP} / 2 – 20	—	ns	
ALE ↓ → $\overline{RD}$ ↓ time	t_{LLRL}	$\overline{RD}$, ALE	—	t_{CP} / 2 – 15	—	ns	

Notes : • t_{CP} : See (1) Clock Timing Ratings.
• $V_{CC} = V_{CC}3 = V_{CC}5$

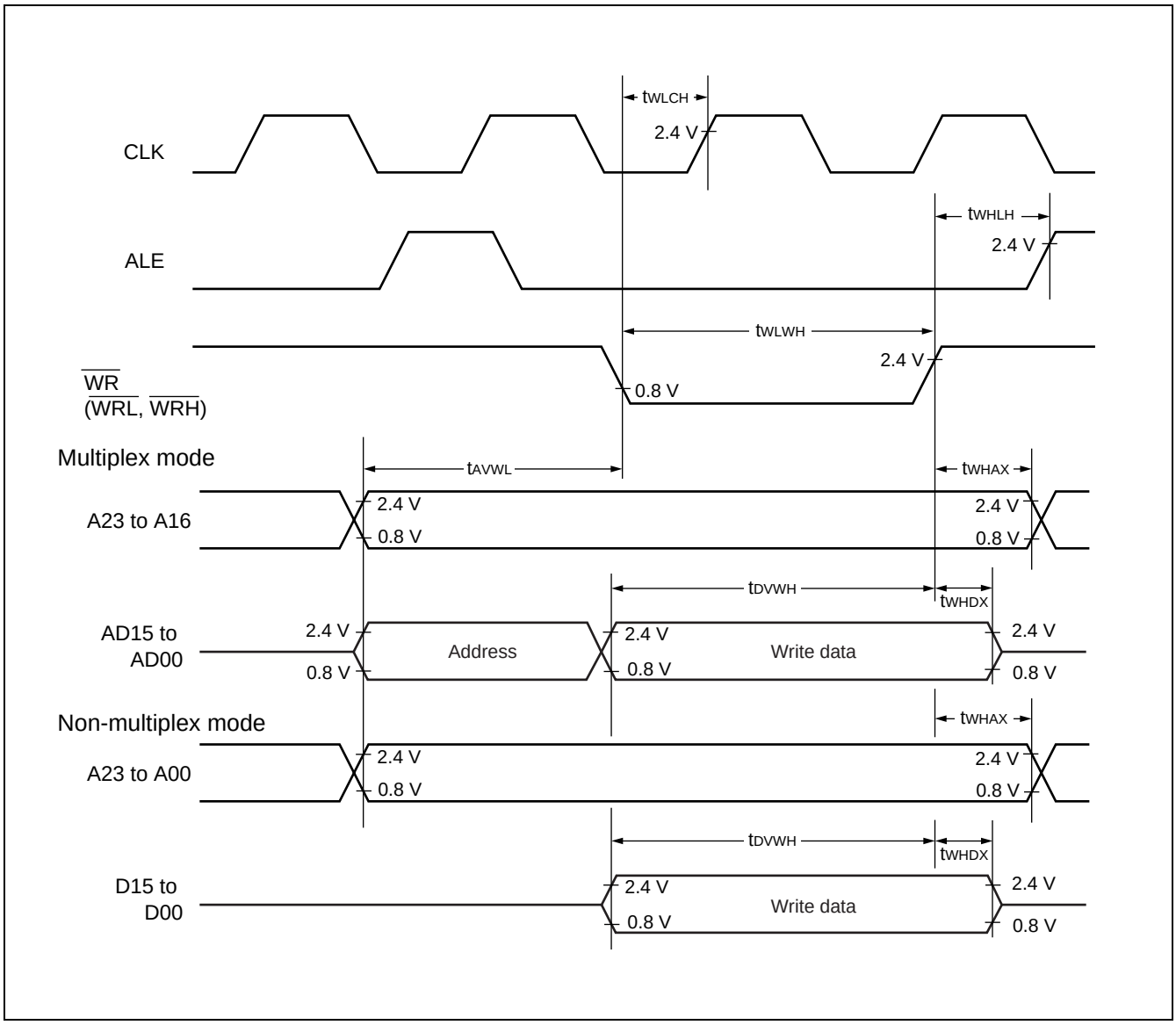

CLK
ALE
RD
Multiplex mode
A23 to A16
AD15 to AD00
Non-multiplex mode
A23 to A00
D15 to D00
tAVCH
tRLCH
tRHLH
tLHLL
tRLRH
tAVLL
tLLAX
tLLRL
tAVRL
tRLDV
tRHAX
tAVDV
tRHDX
2.4 V
0.8 V
0.7 VCC
0.3 VCC
Address
Read data

(6) Bus Write Timing

(V_{CC} = 2.7 V to 3.6 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Valid address → $\overline{WR}$ ↓ time	t_{AVWL}	Address pins, $\overline{WR}$	—	t_{CP} – 20	—	ns	
$\overline{WR}$ pulse width	t_{WLWH}	$\overline{WRL}$, $\overline{WRH}$	—	3 t_{CP} / 2 – 25	—	ns	at f_{cp} = 20 MHz
			—	3 t_{CP} / 2 – 20	—	ns	at f_{cp} = 16 MHz
Valid data output → $\overline{WR}$ ↑ time	t_{DVWH}	Data pins, $\overline{WR}$	—	3 t_{CP} / 2 – 20	—	ns	
$\overline{WR}$ ↑ → data hold time	t_{WHDX}	$\overline{WR}$, Data pins	—	15	—	ns	at f_{cp} = 20 MHz
			—	20	—	ns	at f_{cp} = 16 MHz
			—	30	—	ns	at f_{cp} = 8 MHz
$\overline{WR}$ ↑ → address valid time	t_{WHAX}	$\overline{WR}$, Address pins	—	t_{CP} / 2 – 10	—	ns	
$\overline{WR}$ ↑ → ALE ↑ time	t_{WHLH}	$\overline{WR}$, ALE	—	t_{CP} / 2 – 15	—	ns	
$\overline{WR}$ ↓ → CLK ↑ time	t_{WLCH}	$\overline{WR}$, CLK	—	t_{CP} / 2 – 20	—	ns	

Notes : • t_{CP} : See (1) Clock Timing Ratings.
• V_{CC} = $V_{CC}3$ = $V_{CC}5$

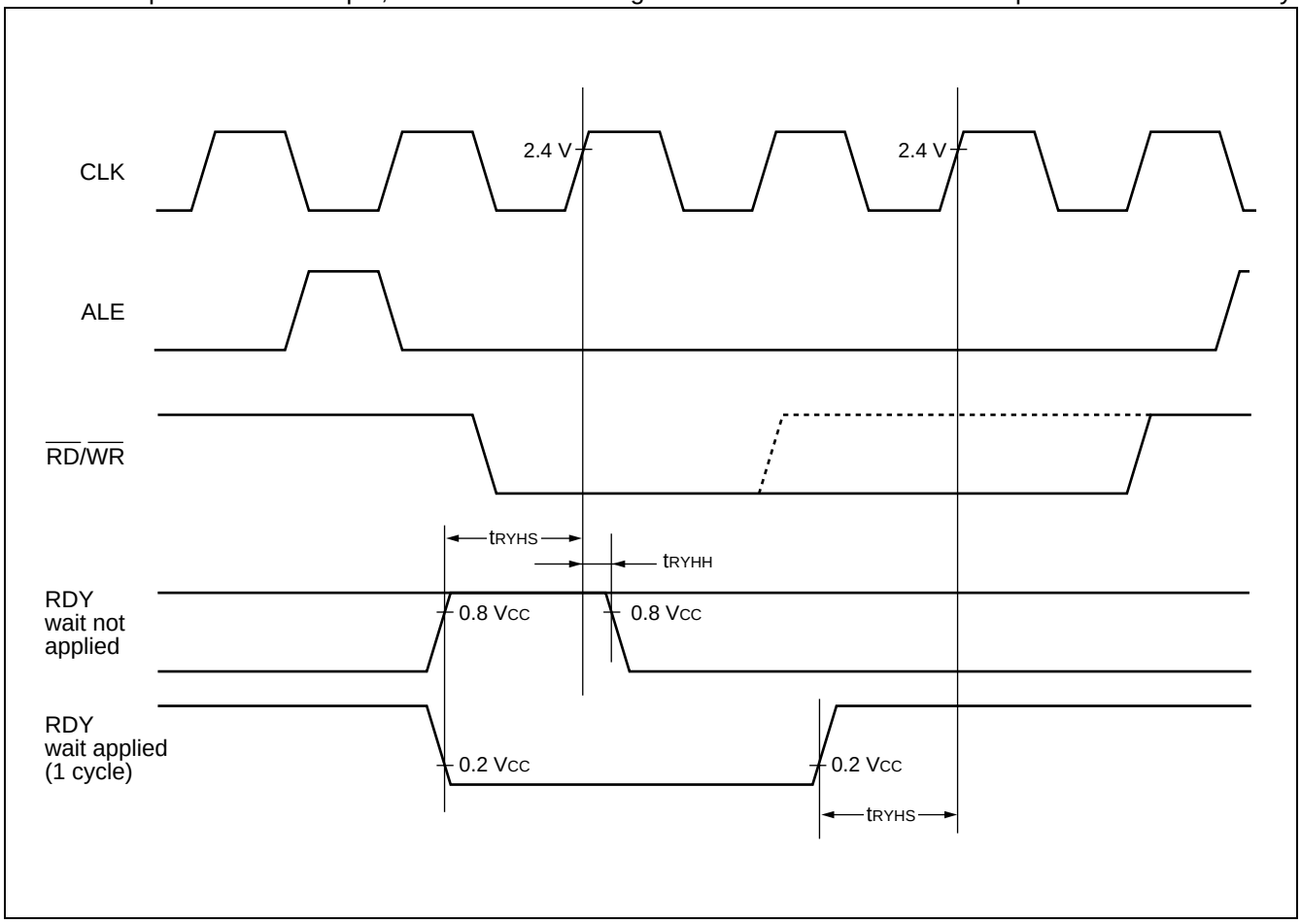

tWLCH
2.4 V
CLK
tWHLH
2.4 V
ALE
tWLWH
2.4 V
0.8 V
WR
(WRL, WRH)
Multiplex mode
tAVWL
tWHAX
A23 to A16
2.4 V
0.8 V
2.4 V
0.8 V
tDVWH
tWHDX
AD15 to AD00
2.4 V
0.8 V
Address
2.4 V
0.8 V
Write data
2.4 V
0.8 V
Non-multiplex mode
tWHAX
A23 to A00
2.4 V
0.8 V
2.4 V
0.8 V
tDVWH
tWHDX
D15 to D00
2.4 V
0.8 V
Write data
2.4 V
0.8 V

(7) Ready Input Timing

(V_{CC} = 2.7 V to 3.6 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condi-tions	Value		Unit	Remarks
				Min	Max		
RDY setup time	t_{RYHS}	RDY	—	45	—	ns	
			—	70	—	ns	f_{cp} = 8 MHz
RDY hold time	t_{RYHH}		—	0	—	ns	

Notes : • If the RDY setup time is not sufficient, use the auto ready function.
• $V_{CC} = V_{CC}3 = V_{CC}5$
• If input from the RDY pin, note that the AC ratings must be satisfied so that the chip will not drive recklessly.

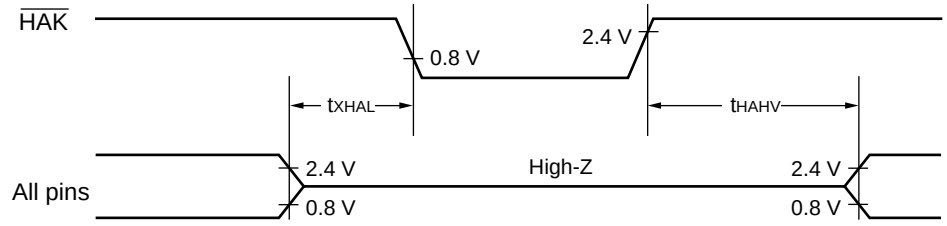


(8) Hold Timing

(V_{CC} = 2.7 V to 3.6 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condi-tions	Value		Unit	Remarks
				Min	Max		
Pin floating → $\overline{HAK}$ ↓ time	t_{XHAL}	$\overline{HAK}$	—	30	t_{CP}	ns	
$\overline{HAK}$ ↓ → valid data time	t_{HAHV}	$\overline{HAK}$		t_{CP}	2 t_{CP}	ns	

Notes : • t_{CP} : See (1) Clock Timing Ratings.
• V_{CC} = $V_{CC}3$ = $V_{CC}5$
• If the HRQ pin is read, at least one cycle is required before the $\overline{HAK}$ pin changes.



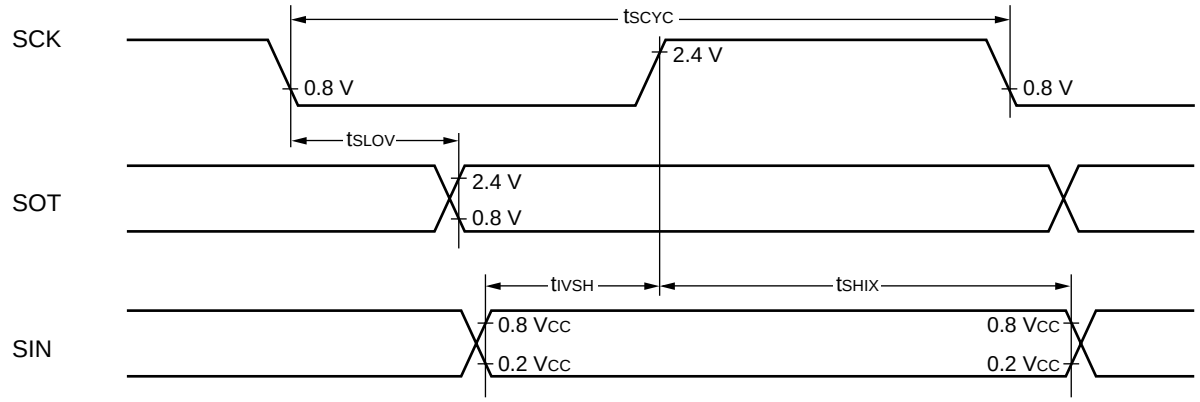
(9) UART Timing

(V_{CC} = 2.7 V to 3.6 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

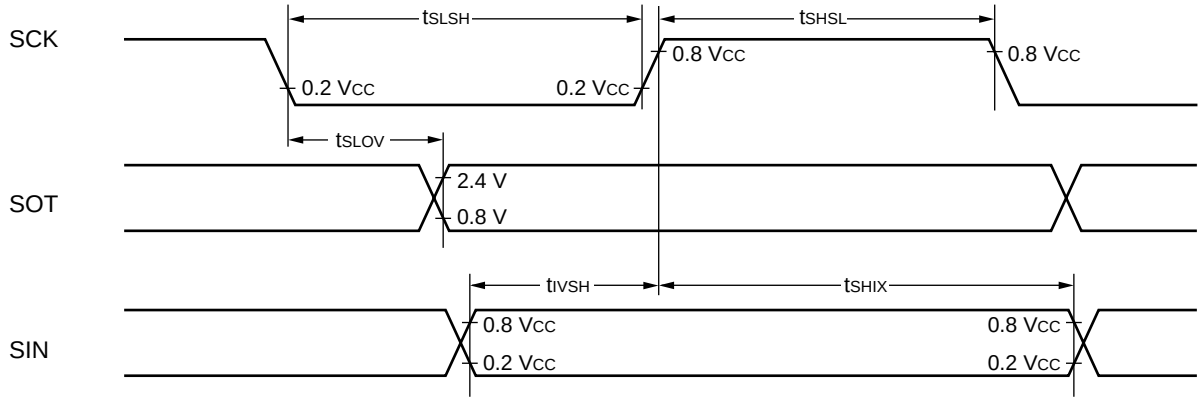
Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	—	Internal shift clock mode output pin C_L = 80 pF + 1 TTL	8 t_{CP}	—	ns	
SCK ↓ → SOT delay time	t_{SLOV}	—		– 80	+ 80	ns	
				– 120	+ 120	ns	f_{cp} = 8 MHz
Valid SIN → SCK ↑	t_{IVSH}	—		100	—	ns	
				200	—	ns	f_{cp} = 8 MHz
SCK ↑ → valid SIN hold time	t_{SHIX}	—		t_{CP}	—	ns	
Serial clock “H” pulse width	t_{SHSL}	—	External shift clock mode output pin C_L = 80 pF + 1 TTL	4 t_{CP}	—	ns	
Serial clock “L” pulse width	t_{SLSH}	—		4 t_{CP}	—	ns	
SCK ↓ → SOT delay time	t_{SLOV}	—		—	150	ns	
				—	200	ns	f_{cp} = 8 MHz
Valid SIN → SCK ↑	t_{IVSH}	—		60	—	ns	
				120	—	ns	f_{cp} = 8 MHz
SCK ↑ → valid SIN hold time	t_{SHIX}	—		60	—	ns	
				120	—	ns	f_{cp} = 8 MHz

Notes : • These AC characteristics are for operation in CLK synchronous mode.
• C_L is the load capacitance applied to pins during testing.
• t_{CP} : See (1) Clock Timing Ratings.
• $V_{CC} = V_{CC}3 = V_{CC}5$

- **Internal Shift Clock Mode**



- **External Shift Clock Mode**



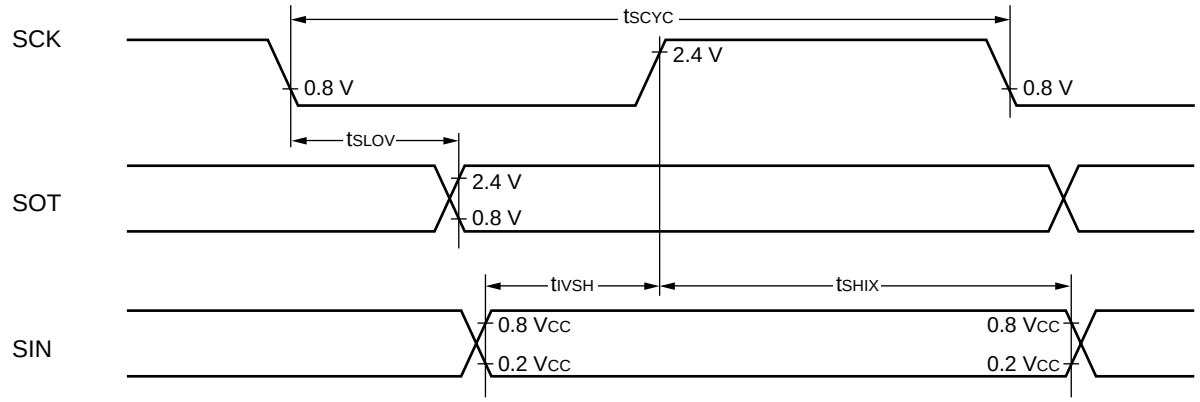
(10) I/O Expanded Serial Interface Timing

(V_{CC} = 2.7 V to 3.6 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

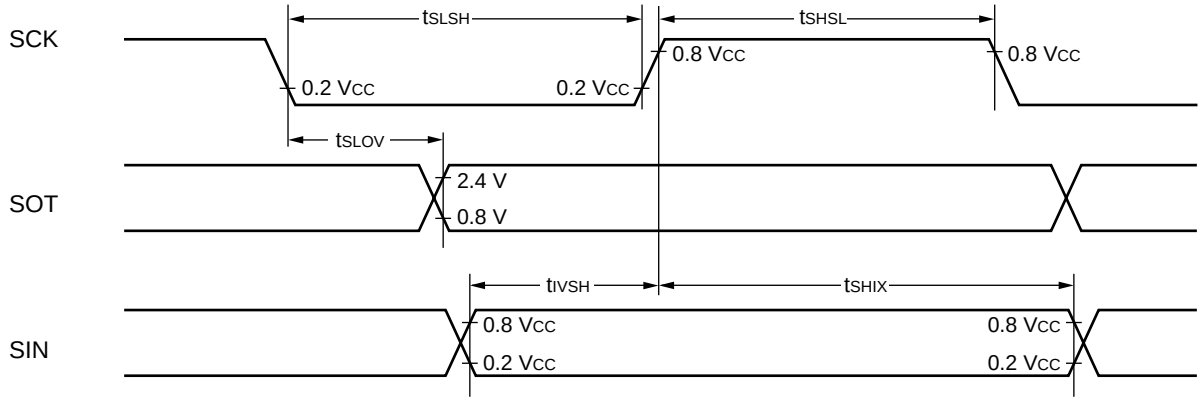
Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	—	Internal shift clock mode output pin C_L = 80 pF + 1 TTL	8 t_{CP}	—	ns	
SCK ↓ → SOT delay time	t_{SLOV}	—		– 80	+ 80	ns	
				– 120	+ 160	ns	f_{cp} = 8 MHz
Valid SIN → SCK ↑	t_{IVSH}	—		100	—	ns	
				200	—	ns	f_{cp} = 8 MHz
SCK ↑ → valid SIN hold time	t_{SHIX}	—		t_{CP}	—	ns	
Serial clock “H” pulse width	t_{SHSL}	—	External shift clock mode output pin C_L = 80 pF + 1 TTL	4 t_{CP}	—	ns	
Serial clock “L” pulse width	t_{SLSH}	—		4 t_{CP}	—	ns	
SCK ↓ → SOT delay time	t_{SLOV}	—		—	150	ns	
				—	200	ns	f_{cp} = 8 MHz
Valid SIN → SCK ↑	t_{IVSH}	—		60	—	ns	
				120	—	ns	f_{cp} = 8 MHz
SCK ↑ → valid SIN hold time	t_{SHIX}	—		60	—	ns	
				120	—	ns	f_{cp} = 8 MHz

Notes : • These AC ratings are for operation in CLK synchronous mode.
- C_L is the load capacitance applied to pins during testing.
- t_{CP} : See (1) Clock Timing Ratings.
- Values shown are target values.
- $V_{CC} = V_{CC}3 = V_{CC}5$

- **Internal shift clock mode**



- **External shift clock mode**

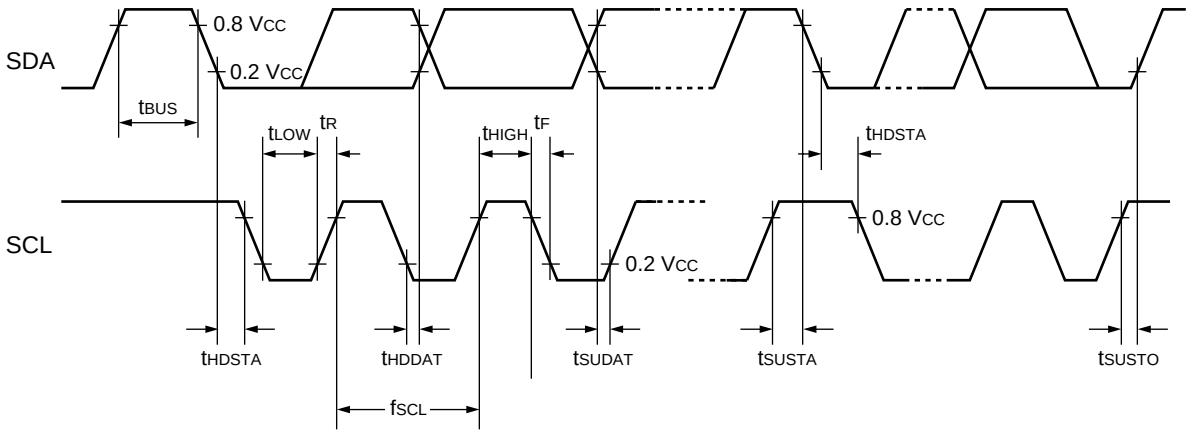


(11) I²C Timing

(V_{CC} = 2.7 V to 3.6 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Sym-bol	Pin name	Condi-tions	Value		Unit	Remarks
				Min	Max		
SCL clock frequency	f_{SCL}	—	—	0	100	kHz	
Bus free time between stop and start	t_{BUS}	—		4.7	—	µs	
Hold time (resend) start	t_{HDSTA}	—		4.0	—	µs	First clock pulse is generated after this interval.
SCL clock “L” status hold time	t_{LOW}	—		4.7	—	µs	
SCL clock “H” status hold time	t_{HIGH}	—		4.0	—	µs	
Resend start condition setup time	t_{SUSTA}	—		4.7	—	µs	
Data hold time	t_{HDDAT}	—		0	—	µs	
Data setup time	t_{SUDAT}	—		40	—	ns	
SDA and SCL signal rise time	t_R	—		—	1000	ns	
SDA and SCL signal fall time	t_F	—		—	300	ns	
Stop condition setup time	t_{SUSTO}	—		4.0	—	µs	

Note : $V_{CC} = V_{CC}3 = V_{CC}5$

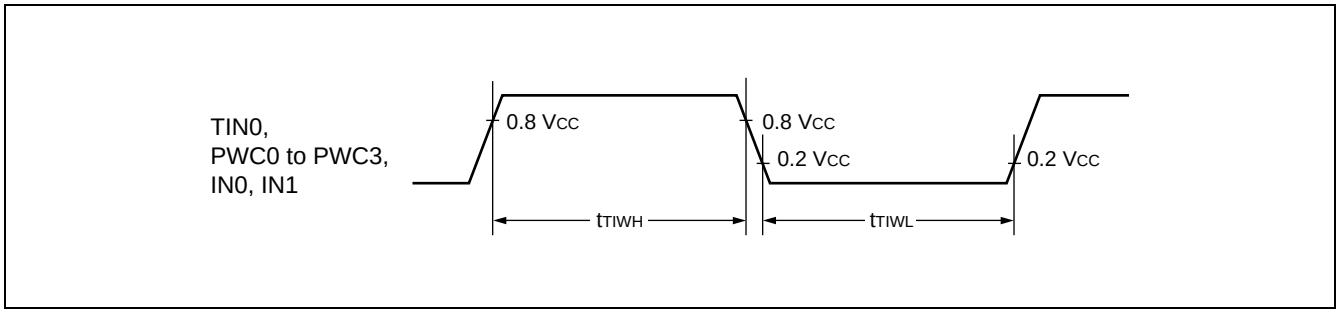


(12) Timer Input Timing

(V_{CC} = 2.7 V to 3.6 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condi-tions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TIWH} t_{TIWL}	TIN0, IN0, IN1, PWC0 to PWC3	—	4 t_{CP}	—	ns	

Notes : • t_{CP} : See (1) Clock Timing Ratings.
• $V_{CC} = V_{CC}3 = V_{CC}5$

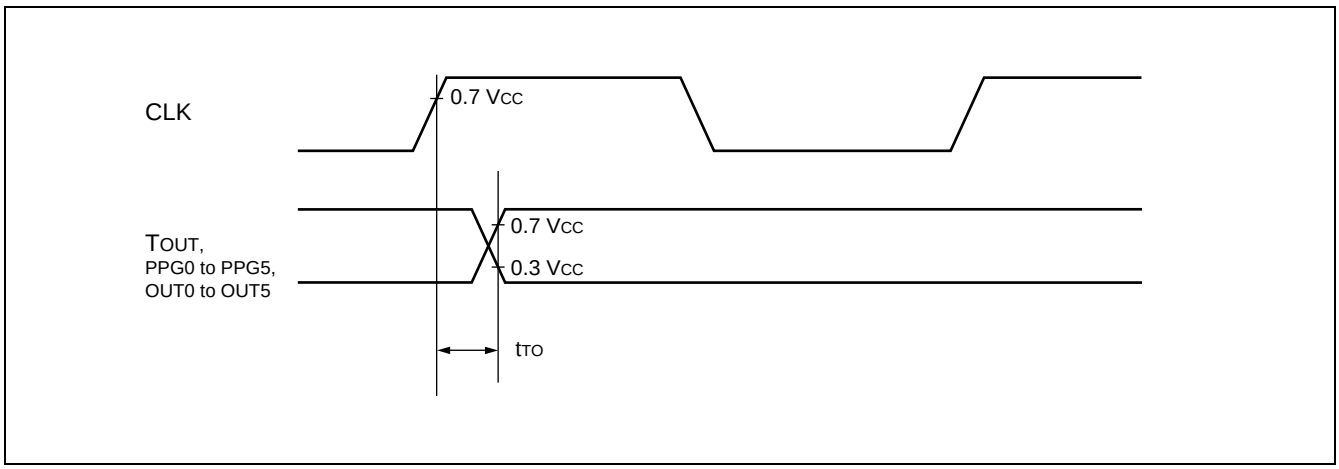


(13) Timer Output Timing

(V_{CC} = 2.7 V to 3.6 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Sym-bol	Pin name	Condi-tions	Value		Unit	Remarks
				Min	Max		
CLK ↑ → Tout change time PPG0 to PPG5 change time OUT0 to OUT5 change time	t_{TO}	TOT0, PPG0 to PPG5, OUT0 to OUT5	80 pF load	30	—	ns	

Note : $V_{CC} = Vcc3 = V_{CC}5$

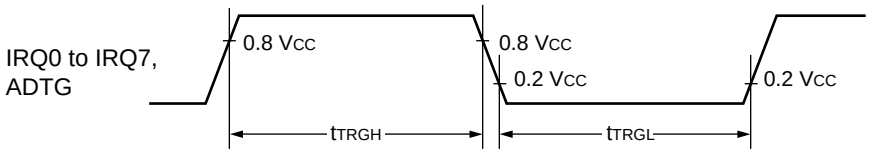


(14) Trigger Input Timing

(V_{CC} = 2.7 V to 3.6 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TRGH} t_{TRGL}	ADTG, IRQ0 to IRQ7	—	5 t_{CP}	—	ns	In normal operation
				1	—	µs	Stop mode

Notes : • t_{CP} : See (1) Clock Timing Ratings.
• $V_{CC} = V_{CC}3 = V_{CC}5$

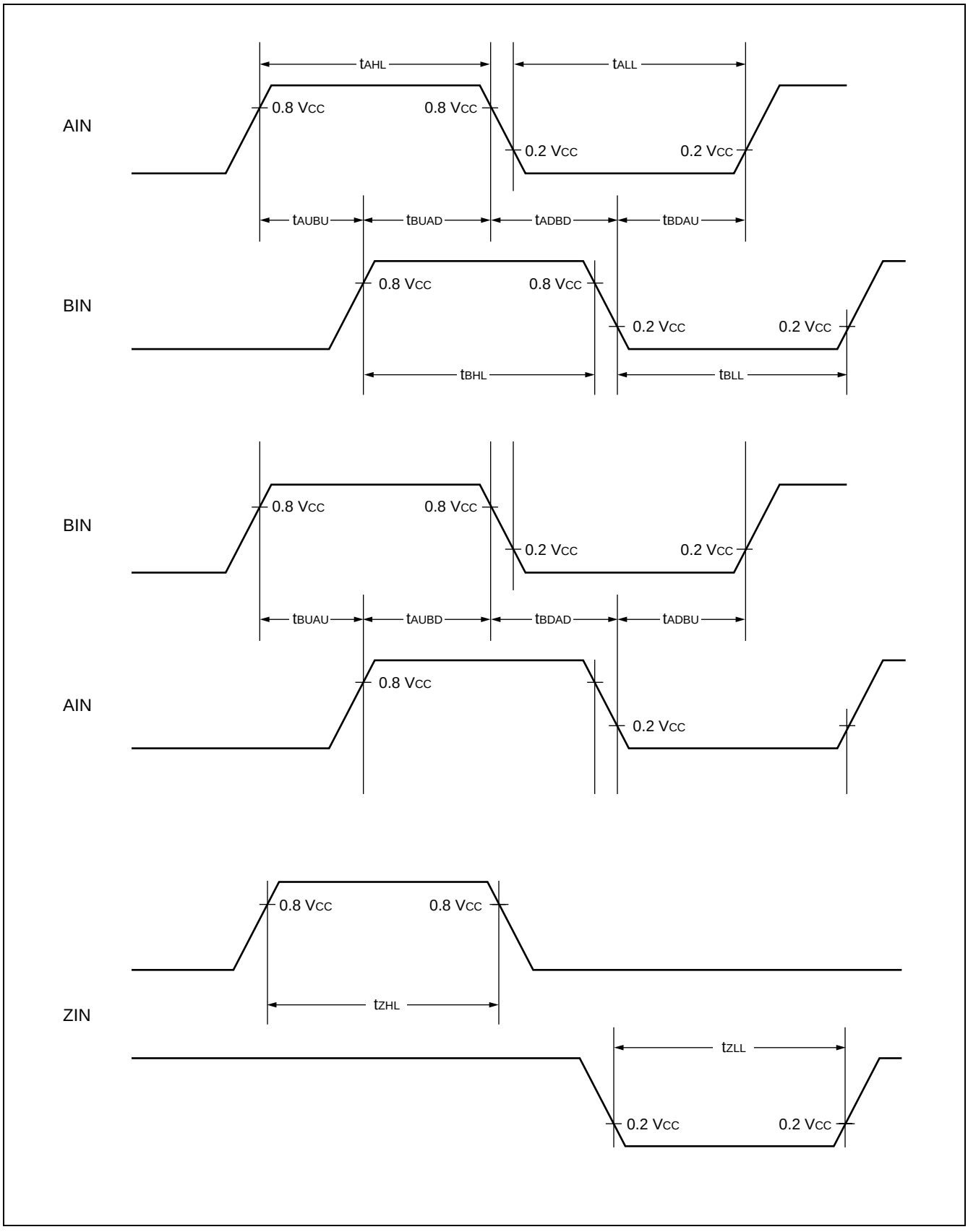


(15) Up/down Counter Timing

(V_{CC} = 2.7 V to 3.6 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
AIN input “H” pulse width	t_{AHL}	AIN0, AIN1, BIN0, BIN1	80 pF load	8 t_{CP}	—	ns	
AIN input “L” pulse width	t_{ALL}			8 t_{CP}	—	ns	
BIN input “H” pulse width	t_{BHL}			8 t_{CP}	—	ns	
BIN input “L” pulse width	t_{BLL}			8 t_{CP}	—	ns	
AIN ↑ → BIN ↑ time	t_{AUBU}			4 t_{CP}	—	ns	
BIN ↑ → AIN ↓ time	t_{BUAD}			4 t_{CP}	—	ns	
AIN ↓ → BIN ↑ time	t_{ADBD}			4 t_{CP}	—	ns	
BIN ↓ → AIN ↑ time	t_{BDAU}			4 t_{CP}	—	ns	
BIN ↑ → AIN ↑ time	t_{BUAU}			4 t_{CP}	—	ns	
AIN ↑ → BIN ↓ time	t_{AUBD}			4 t_{CP}	—	ns	
BIN ↓ → AIN ↑ time	t_{BDAD}			4 t_{CP}	—	ns	
AIN ↓ → BIN ↑ time	t_{ADBU}			4 t_{CP}	—	ns	
ZIN input “H” pulse width	t_{ZHL}	ZIN0, ZIN1		4 t_{CP}	—	ns	
ZIN input “L” pulse width	t_{ZLL}			4 t_{CP}	—	ns	

Notes : • t_{CP} : See (1) Clock Timing Ratings.
• $V_{CC} = V_{CC}3 = V_{CC}5$

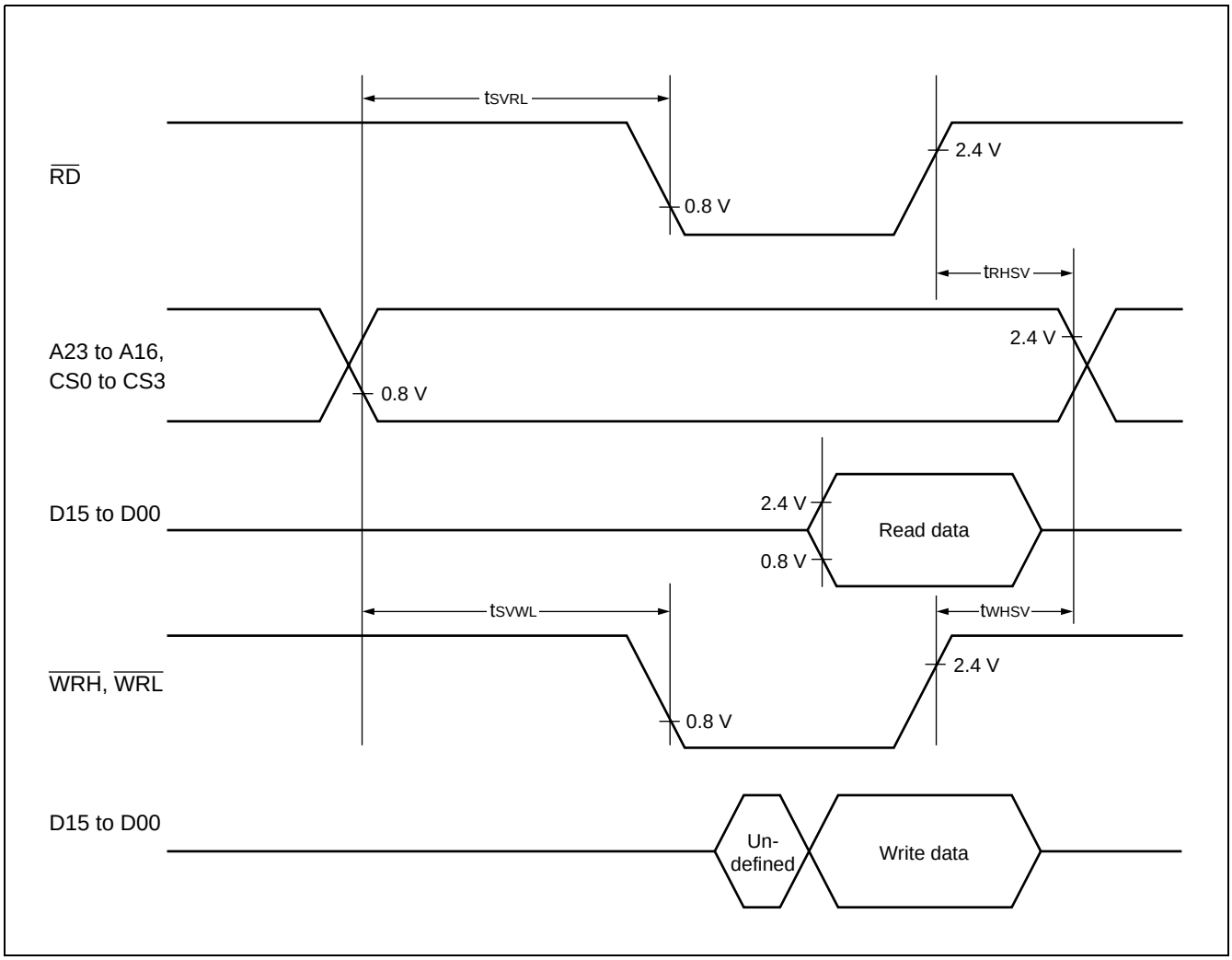

AIN
tAHL
tALL
0.8 VCC
0.8 VCC
0.2 VCC
0.2 VCC
tAUBU
tBUAD
tADBD
tBDAU
BIN
0.8 VCC
0.8 VCC
0.2 VCC
0.2 VCC
tBHL
tBLL
BIN
0.8 VCC
0.8 VCC
0.2 VCC
0.2 VCC
tBUAU
tAUBD
tBDAD
tADBU
AIN
0.8 VCC
0.2 VCC
ZIN
0.8 VCC
0.8 VCC
tZHL
tZLL
0.2 VCC
0.2 VCC

(16) Chip Select Output Timing

(V_{CC} = 2.7 V to 3.6 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Chip select output valid time → $\overline{RD}$ ↓	t_{SVRL}	CS0 to CS3, $\overline{RD}$	—	t_{CP} / 2 – 10	—	ns	
Chip select output valid time → $\overline{WR}$ ↓	t_{SVWL}	CS0 to CS3, $\overline{WRH}$, $\overline{WRL}$	—	t_{CP} / 2 – 10	—	ns	
$\overline{RD}$ ↑ → chip select output valid time	t_{RHSV}	$\overline{RD}$, CS0 to CS3	—	t_{CP} / 2 – 20	—	ns	
$\overline{WR}$ ↑ → chip select output valid time	t_{WHSV}	$\overline{WRH}$, $\overline{WRL}$, CS0 to CS3	—	t_{CP} / 2 – 20	—	ns	

Notes : • t_{CP} : See (1) Clock Timing Ratings.
• $V_{CC} = V_{CC}3 = V_{CC}5$



Note : The chip select output signal changes at the same time due to the structure of the internal bus, leading to the possibility of a bus fight. AC warranty does not apply between ALE output signals and chip select output signals.

5. A/D Converter Electrical Characteristics

(V_{CC} = AV_{CC} = 1.8 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	—	—	—	—	10	bit	
Total error	—	—	—	—	±3.0	LSB	at V_{CC} = AV_{CC} = 2.2 V to 3.6 V
					±4.0	LSB	at V_{CC} = AV_{CC} = 1.8 V to 2.2 V
Linear error	—	—	—	—	±2.5	LSB	at V_{CC} = AV_{CC} = 2.2 V to 3.6 V
					±3.0	LSB	at V_{CC} = AV_{CC} = 1.8 V to 2.2 V
Differential linear error	—	—	—	—	±1.9	LSB	at V_{CC} = AV_{CC} = 2.2 V to 3.6 V
					±2.4	LSB	at V_{CC} = AV_{CC} = 1.8 V to 2.2 V
Zero transition voltage	V_{OT}	AN0 to AN7	AV_{SS} – 1.5 LSB	AV_{SS} + 0.5 LSB	AV_{SS} + 2.5 LSB	mV	at V_{CC} = AV_{CC} = 2.2 V to 3.6 V
			AV_{SS} – 2.0 LSB	AV_{SS} + 0.5 LSB	AV_{SS} + 3.0 LSB	mV	at V_{CC} = AV_{CC} = 1.8 V to 2.2 V
Full scale transition voltage	V_{FST}	AN0 to AN7	AVRH – 3.5 LSB	AVRH – 1.5 LSB	AVRH + 0.5 LSB	mV	at V_{CC} = AV_{CC} = 2.2 V to 3.6 V
			AVRH – 4.0 LSB	AVRH – 1.5 LSB	AVRH + 1.0 LSB	mV	at V_{CC} = AV_{CC} = 1.8 V to 2.2 V
Conversion time	—	—	5.8125*1	—	—	µs	at AVRH ≥ 2.7 V
Analog port input current	I_{AIN}	AN0 to AN7	—	0.1	10	µA	
Analog input voltage	V_{AIN}	AN0 to AN7	AV_{SS}	—	AVRH	V	
Reference voltage	—	AVRH	AV_{SS} + 2.2	—	AV_{CC}	V	at V_{CC} = AV_{CC} = 2.2 V to 3.6 V
			AV_{SS} + 1.8	—	AV_{CC}	V	at V_{CC} = AV_{CC} = 1.8 V to 2.2 V
Supply current	I_A	AV_{CC}	—	1.2	4.4	mA	
	I_{AH}	AV_{CC}	—	—	5*2	µA	
Reference voltage supply current	I_R	AVRH	—	95	170	µA	
	I_{RH}	AVRH	—	—	5*2	µA	
Inter-channel variation	—	AN0 to AN7	—	—	4	LSB	

*1 : At machine clock frequency 16 MHz.

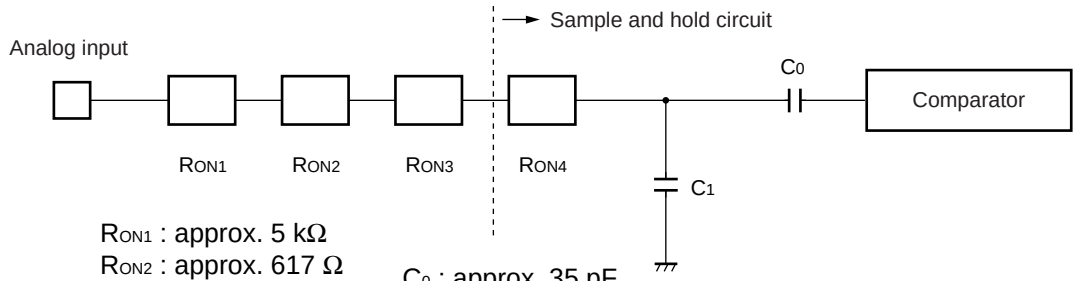
*2 : Current with A/D converter not operating, and CPU in stop mode (V_{CC} = AV_{CC} = AVRH = 3.0 V)

Notes : • $V_{CC} = V_{CC}3 = V_{CC}5$
- The relative error increases as |AVRH − AV_{SS}| is reduced.
- Observe the following conditions in applying output impedance on the external circuits of the analog input.
  Output impedance on the external circuit is recommended to be 6 kΩ or less.
  If external capacitance is used, it is recommended that this be several thousand times the level of internal capacitors in view of the effects of voltage division between the external capacitor and the interior of the chip.
- If the output impedance of the external circuits is too high, the analog voltage sampling time may be insufficient.
  (sampling time = 3.00 µs at machine clock frequency 20 MHz) .

< Reference Data >

- **Analog Input Circuit**

- **Model analog input circuit**



R_{ON1} : approx. 5 kΩ
R_{ON2} : approx. 617 Ω
R_{ON3} : approx. 617 Ω
R_{ON4} : approx. 473 Ω

C_0 : approx. 35 pF
C_1 : approx. 2 pF

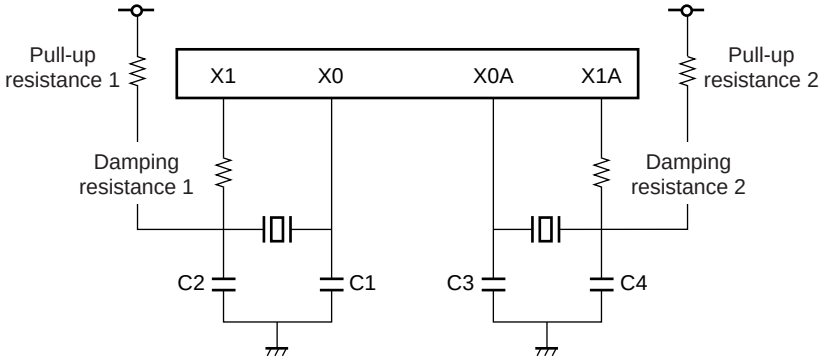
Note : Values shown here are intended as guidelines.

- **A/D Operating Frequency Restrictions**

Supply voltage	A/D conversion time [µs]	Machine clock frequency
3.6 V ≥ AV_{CC} ≥ 3.0 V	4.650	20 MHz
3.6 V ≥ AV_{CC} ≥ 2.7 V	5.813	16 MHz
2.7 V > AV_{CC} ≥ 2.6 V	6.643	14 MHz
2.6 V > AV_{CC} ≥ 2.5 V	7.750	12 MHz
2.5 V > AV_{CC} ≥ 2.4 V	8.455	11 MHz
2.4 V > AV_{CC} ≥ 2.3 V	9.300	10 MHz
2.3 V > AV_{CC} ≥ 2.2 V	11.63	8 MHz
2.2 V > AV_{CC} ≥ 2.1 V	15.50	6 MHz
2.1 V > AV_{CC} ≥ 2.0 V	23.25	4 MHz
2.0 V > AV_{CC} ≥ 1.9 V	46.50	2 MHz
1.9 V > AV_{CC} ≥ 1.8 V	93.00	1 MHz

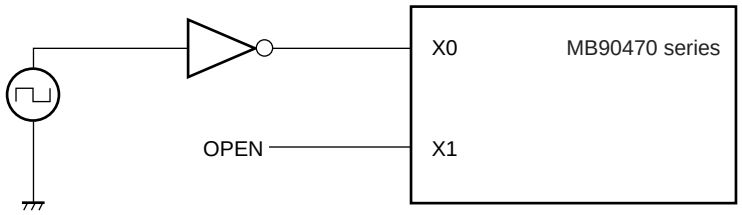
- **Use of the X0/X1, X0A/X1A Pins**

Use with a crystal oscillator



In normal use (V_{CC} = 2 V or higher)
Pull-up resistance 1, 2
Damping resistance 1, 2
C1 to C4
For all pins, consult regarding manufacturer of oscillator.
(Sample operation using V_{CC} = 2 V, f = 5 MHz or less)
Pull-up resistance 1 = 5.1 kΩ
Pull-up resistance 2 = 510 kΩ
Damping resistance 1 = 0 Ω
Damping resistance 2 = 39 kΩ
C1 = C2 = 22 pF
C3 = C4 = 30 pF

- **Sample use of external clock input**



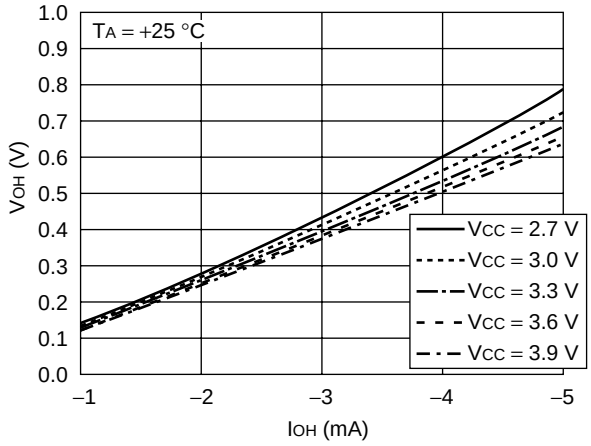
6. Flash Memory Program/Erase Characteristics

Parameter	Conditions	Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time	T_A = + 25 °C, V_{CC} = 3.3 V	—	1	15	s	Excludes 00_H programming prior erasure
Chip erase time		—	7	—	s	Excludes 00_H programming prior erasure
Word (16-bit) programming time		—	16	3600	µs	Excludes system-level overhead
Erase/Program cycle	—	1000	—	—	cycle	
Data hold time	—	100000	—	—	h	

■ SAMPLE CHARACTERISTICS

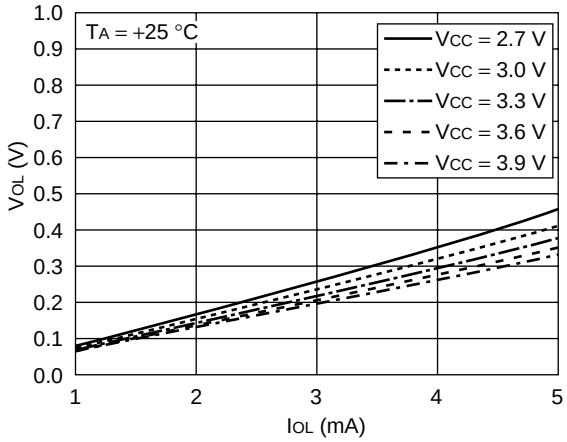
(1) “H” level output voltage

$(V_{CC} - V_{OH})$ – I_{OH}



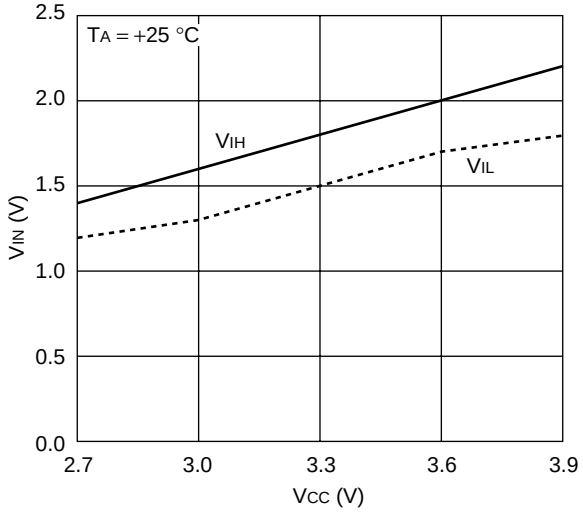
(2) “L” level output voltage

V_{OL} – I_{OL}



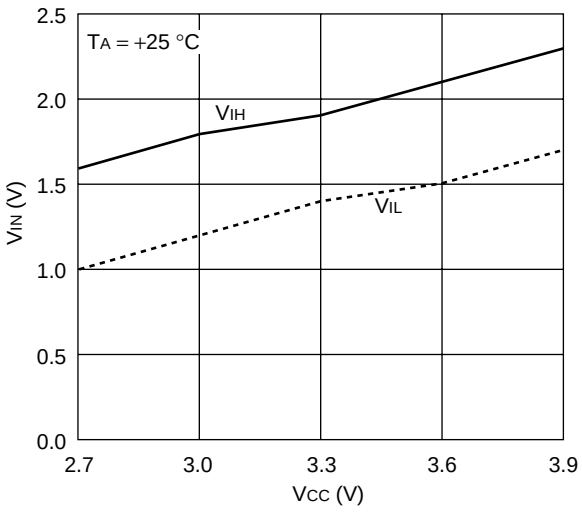
(3) “H” level input voltage/ “L” level input voltage (CMOS input)

V_{IN} – V_{CC}



(4) “H” level input voltage/ “L” level input voltage (hysteresis input)

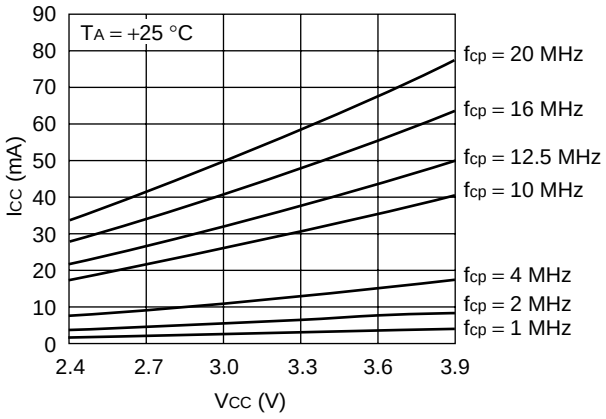
V_{IN} – V_{CC}



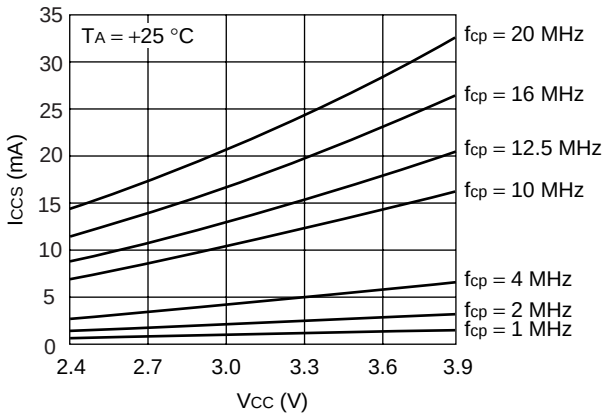
(5) Supply Current (f_{cp} = internal stroke frequency)

- **MASK versions**

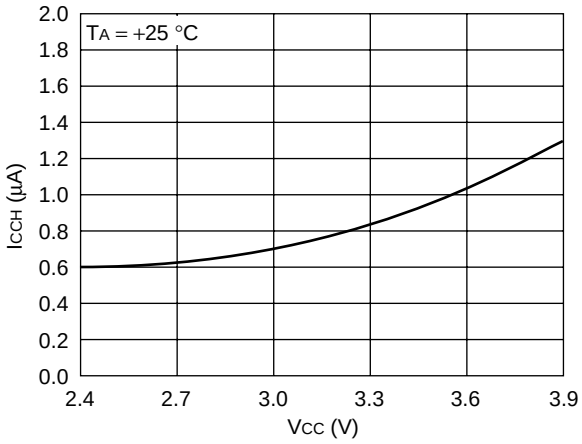
$I_{CC} - V_{CC}$



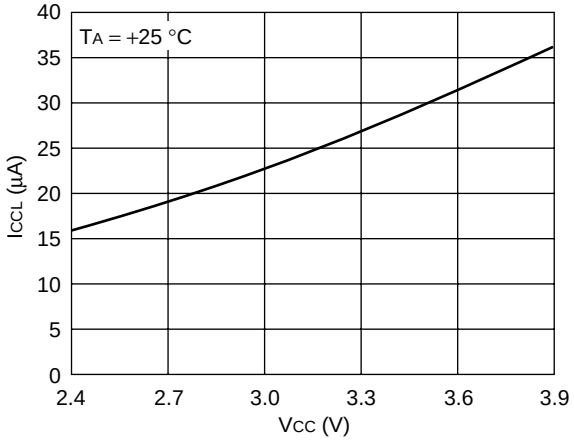
$I_{CCS} - V_{CC}$



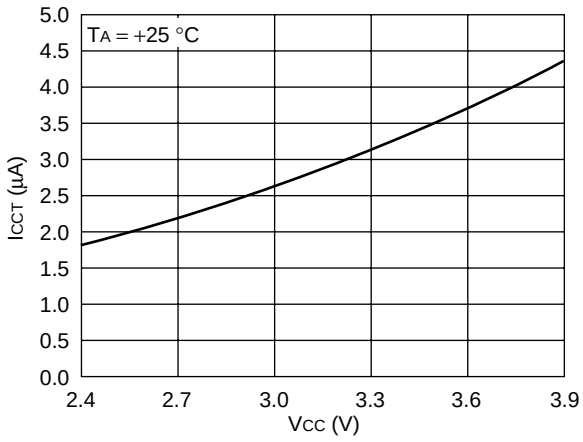
$I_{CCH} - V_{CC}$



$I_{CCL} - V_{CC}$

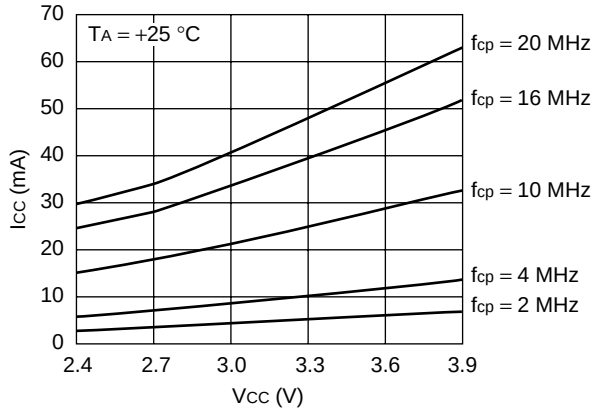


$I_{CCT} - V_{CC}$

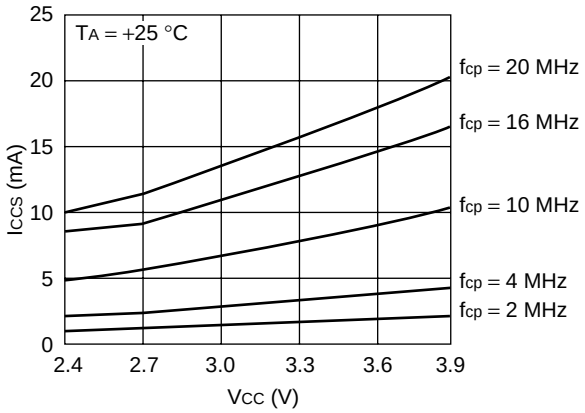


- **FLASH versions**

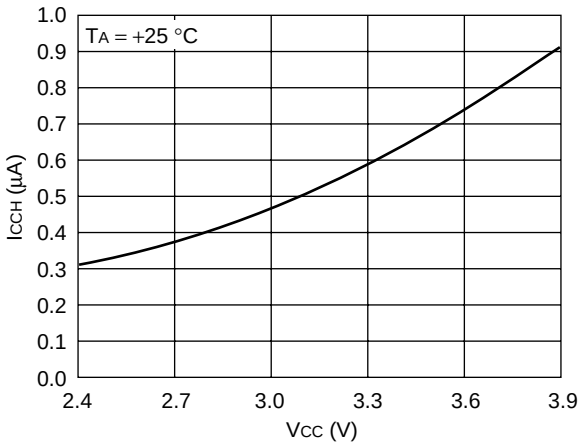
I_{CC} – V_{CC}



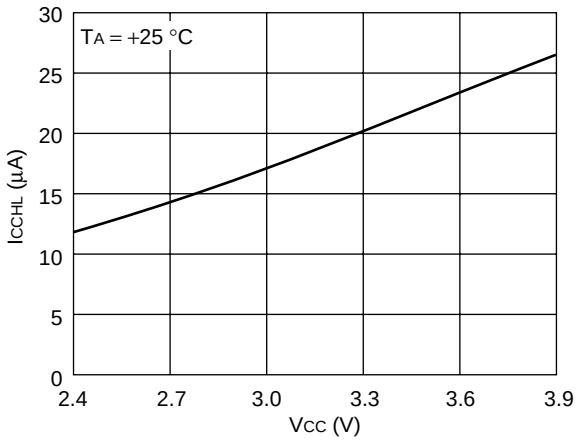
I_{CCS} – V_{CC}



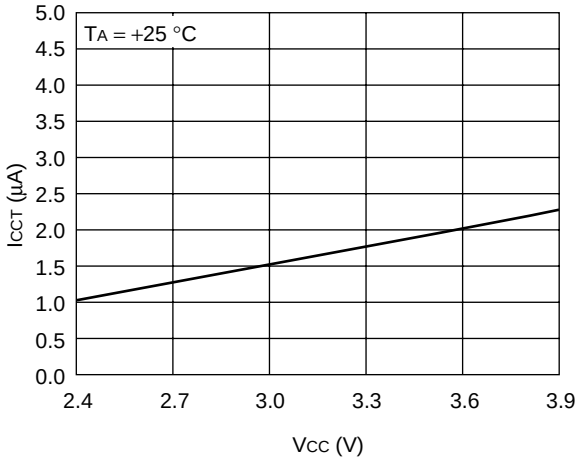
I_{CCH} – V_{CC}



I_{CCL} – V_{CC}



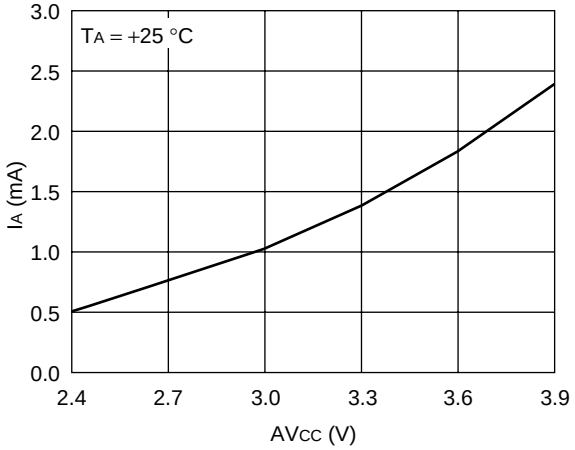
I_{CCT} – V_{CC}



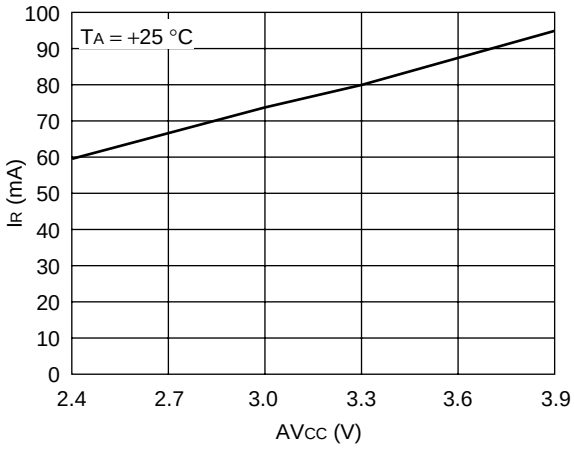
(Continued)

(Continued)

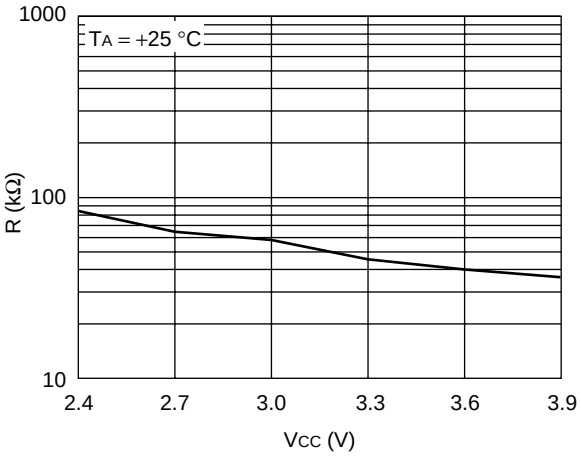
I_A – AV_{CC}



I_R – AV_{CC}



R – V_{CC}



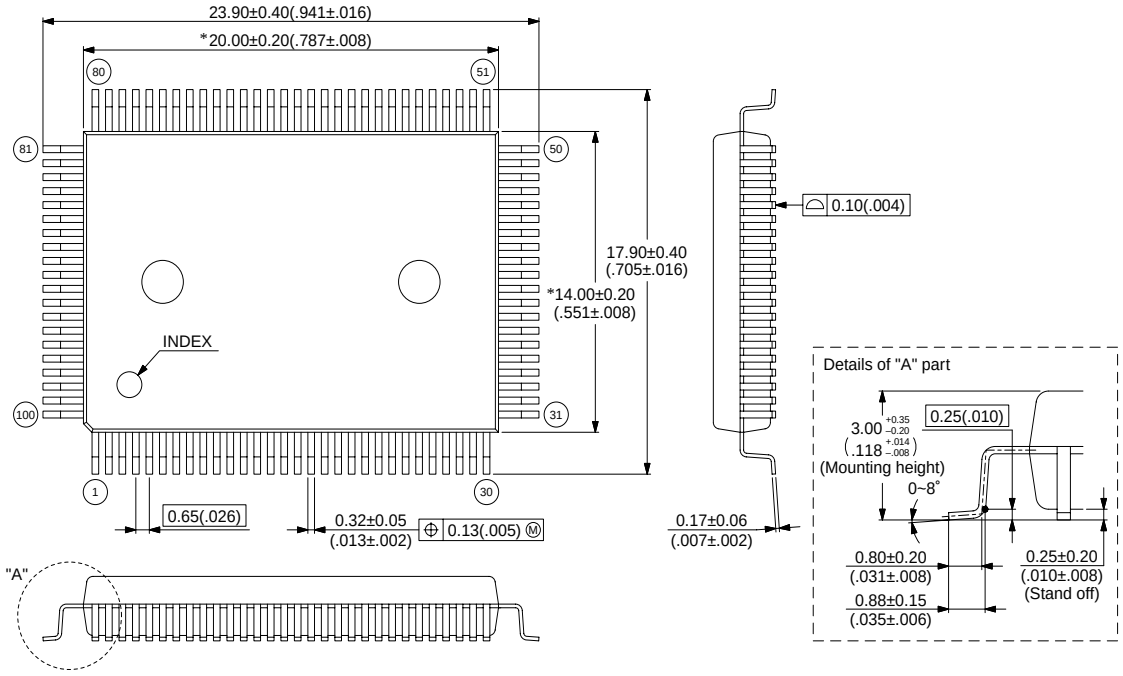
■ ORDERING INFORMATION

Part number	Package	Remarks
MB90473PF MB90474PF MB90477PF MB90478PF MB90F474LPF MB90F474HPF	100-pin plastic QFP (FPT-100P-M06)	
MB90473PFV MB90474PFV MB90477PFV MB90478PFV MB90F474LPFV MB90F474HPFV	100-pin plastic LQFP (FPT-100P-M05)	

■ PACKAGE DIMENSIONS

100-pin plastic QFP
(FPT-100P-M06)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



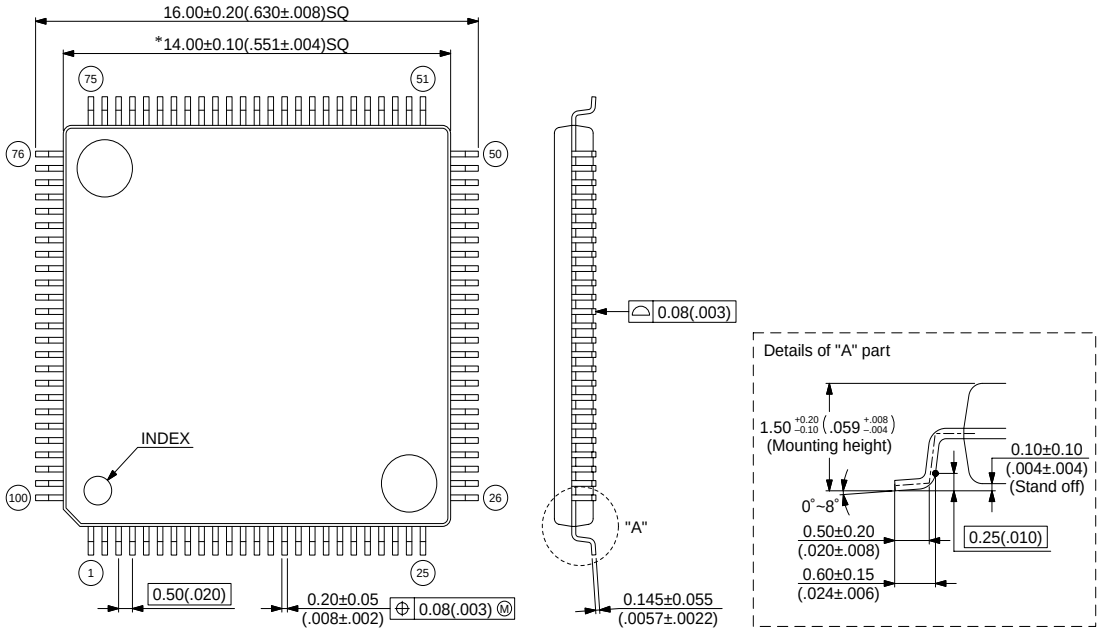
Dimensions in mm (inches)
Note : The values in parentheses are reference values.

(Continued)

(Continued)

100-pin plastic LQFP
(FPT-100P-M05)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches)
Note : The values in parentheses are reference values.

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