DS04-21331-1E

FUJITSU

*DATA SHEET*

# *ASSP for DTS BiCMOS 1.1 GHz/400 MHz PLL Frequency Synthesizer*

# MB15B11

## ■ DESCRIPTION

The MB15B11 is a pulse swallow Phase Locked Loop (PLL) frequency synthesizer LSI. The MB15B11 has dual PLLs, for the 1.1 GHz and 400 MHz bands respectively, and is optimized for systems using IF modulation such as analog cellular communications equipment.
With a supply voltage of 3 V (Typ.) and supply current of 9.5 mA (Typ.), the device enables equipment to operate with low power consumption.

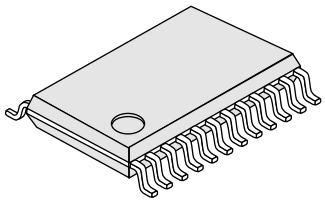
## ■ FEATURES

- Dual internal pulse swallow PLLs
  PLL 1: 400 MHz band
  PLL 2: 1.1 GHz band
- Division ratio set by serial input
  Reference divider: Binary 14-bit reference counter (divide ratio of 8 to 16,383)
  Programmable divider: 1.1 GHz band prescaler (64/65, 128/129), 400 MHz band prescaler (32/33, 64/65)
  Binary 7-bit swallow counter (divide ratio of 0 to 127)
  Binary 11-bit programmable counter (divide ratio of 16 to 2,047)
  * The programmable dividers for PLL1 and PLL2 can be set independently.
- Low voltage operation: 2.7 V to 3.5 V
  The charge pump section uses a separate supply (up to 6.0 V).
- Low current consumption: 9.5 mA (Typ.)

*(Continued)*

## ■ PACKAGE

20-pin, Plastic SSOP

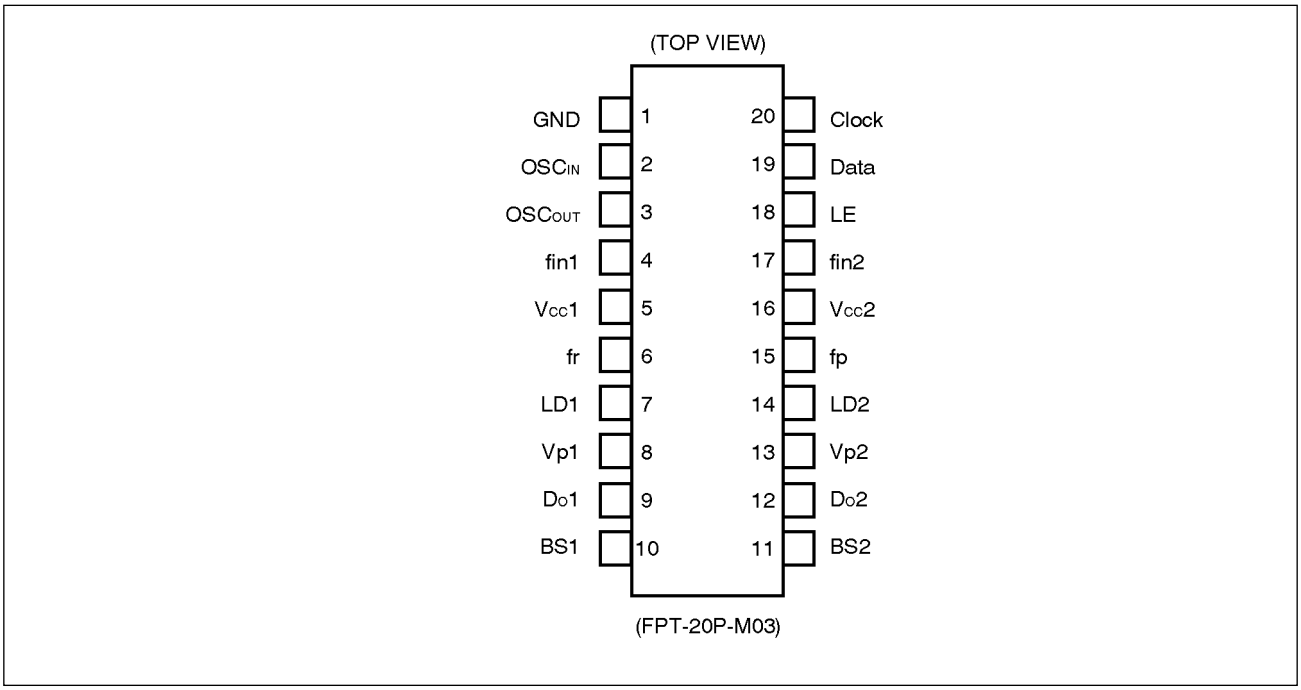


(FPT-20P-M03)

*(Continued)*

- Built-in power saving function
  Power saving current: PLL1 = 100 µA, PLL2 = 100 µA
- Charge pump characteristics based on application
  Separate internal charge pumps are provided for transmit and receive operations.
  Transmit (PLL1): Low sensitivity charge pump (for ease of modulation)
  Receive (PLL2): High sensitivity charge pump (for fast lockup time)
- Internal analog switch
  An internal analog switch is provided to achieve a faster PLL lockup time.
- Phase comparator to support phase conversion
- Wide operating temperature range: Ta = –30°C to +80°C

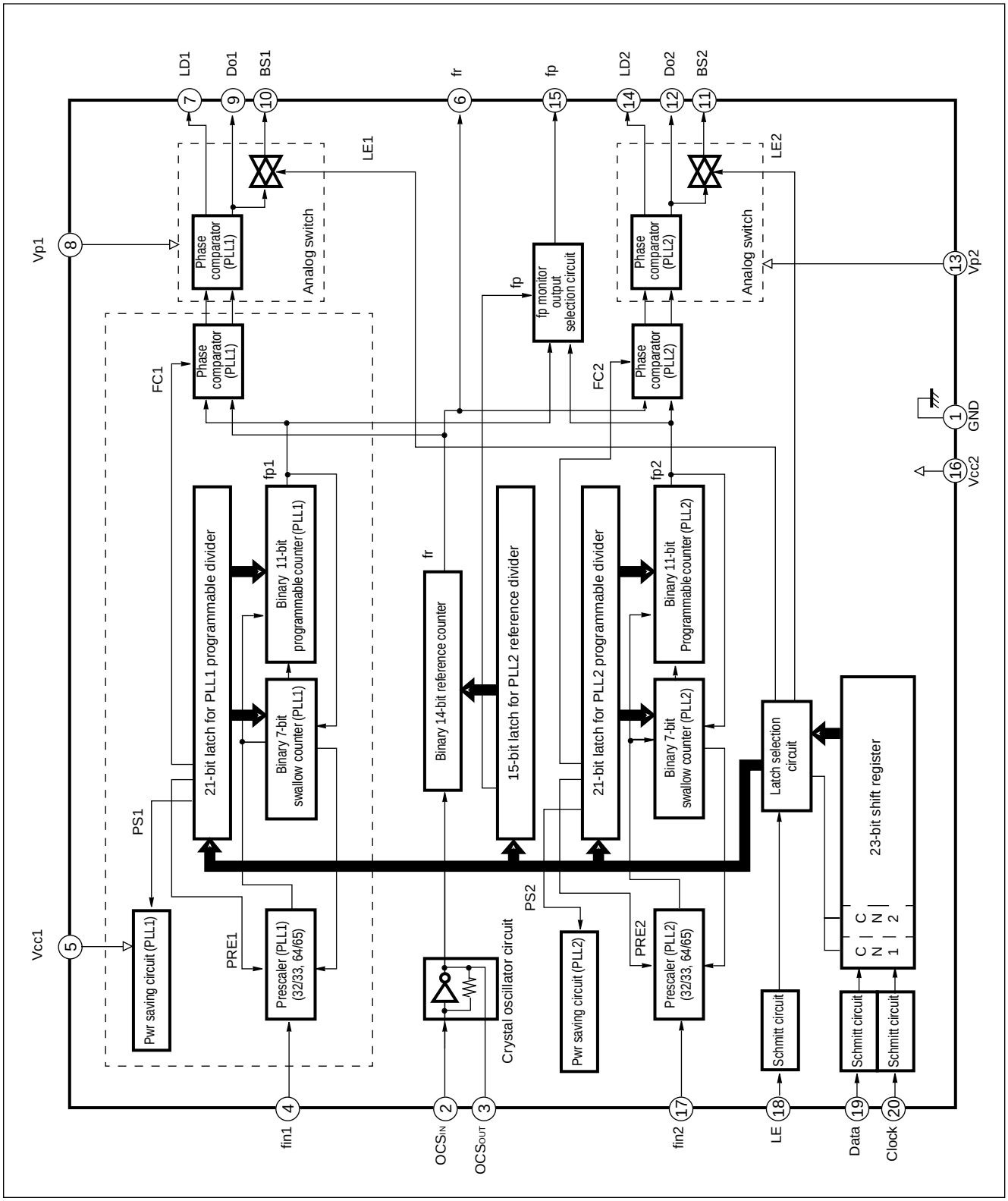
## ■ PIN ASSIGNMENT



## ■ PIN DESCRIPTIONS

| Pin No. | Symbol | I/O | Function |
|---|---|---|---|
| 1 | GND | — | Ground. |
| 2 | $OSC_{IN}$ | I | Crystal oscillator connection pins and reference divider input pins ($OSC_{IN}$ = oscillator circuit input pin, $OSC_{OUT}$ = oscillator circuit output pin). |
| 3 | $OSC_{OUT}$ | O | |
| 4 | $fin_1$ | I | PLL1 prescaler input pin. The input should be AC-coupled. |
| 5 | $V_{CC1}$ | — | PLL1 supply pin.<br>The PLL1 latch data is lost when the power is off. |
| 6 | fr | O | Output monitor pin for the reference divider. |
| 7 | $LD_1$ | O | Lock detect output pin for PLL1.<br>LD = “H” when locked and “L” when unlocked. |
| 8 | $V_{P1}$ | — | Power supply pin for the PLL1 charge pump output and analog switch output. |
| 9 | $D_{O1}$ | O | PLL1 charge pump output pin.<br>The FC bit in the data inverts the phase characteristics. |
| 10 | $BS_1$ | O | PLL1 analog switch output pin.<br>When the switch is on (when LE pin = “H”), this pin outputs the charge pump state. Otherwise, it stays at high impedance. |
| 11 | $BS_2$ | O | PLL2 analog switch output pin.<br>When the switch is on (when LE pin = “H”), this pin outputs the charge pump state. Otherwise, it stays at high impedance. |
| 12 | $D_{O2}$ | O | PLL2 charge pump output pin.<br>The FC bit in the data inverts the phase characteristics. |
| 13 | $V_{P2}$ | — | Power supply pin for the PLL2 charge pump output and analog switch output. |
| 14 | $LD_2$ | O | Lock detect output pin for PLL2.<br>LD = “H” when locked and “L” when unlocked. |
| 15 | fp | O | Comparative divider monitor output pin.<br>The FP data bit setting selects between PLL1 and PLL2 division output.<br>When the FP bit = “H”, outputs for PLL1 (fp1).<br>When the FP bit = “L”, outputs for PLL2 (fp2). |
| 16 | $V_{CC2}$ | — | Supply pin for PLL2, reference divider, shift register, and crystal oscillator circuit.<br>The PLL2 and reference counter latch data is lost when the power is off. |
| 17 | $fin_2$ | I | PLL2 prescaler input pin. The input should be AC-coupled. |
| 18 | LE | I | Input pin for the load enable signal (with schmitt trigger circuit).<br>When LE = “H”, the contents of the shift register are moved to the latches specified by the serial data control bit values.<br>At the same time, the internal analog switch turns on, and the charge pump output signals are output from the BS pins. |
| 19 | Data | I | Serial data input pin (with schmitt trigger circuit).<br>The data’s control bit values selects the data move destination (reference divider, PLL1 programmable divider, or PLL2 programmable divider). |
| 20 | Clock | I | Clock input pin for the 23-bit shift register (with schmitt trigger circuit).<br>Data is read on the rising edge of the clock. |

## ■ BLOCK DIAGRAM



## ■ ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Rating | | Unit | Remarks |
|---|---|---|---|---|---|
| | | Min. | Tax. | | |
| Power supply voltage | $V_{CC}$ | –0.5 | +5.0 | V | |
| | $V_P$ | $V_{CC}$ | 7.0 | V | |
| Output voltage | $V_O$ | –0.5 | $V_{CC}$ + 0.5 | V | |
| Output current | $I_O$ | –10 | +10 | mA | |
| Storage temperature | Tstg | –55 | +125 | °C | |

Note: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ■ RECOMMENDED OPERATING CONDITIONS

| Parameter | Symbol | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Power supply voltage | $V_{CC}$ | 2.7 | 3.0 | 3.5 | V | $V_{CC}1 = V_{CC}2$ |
| | $V_P$ | $V_{CC}$ | — | 6.0 | V | |
| Input voltage | $V_I$ | GND | — | $V_{CC}$ | V | |
| Operating temperature | Ta | –30 | — | +80 | °C | |

**Handling Precautions**

- Transport and store this device in anti-static containers.
- As this is a static-sensitive device; take proper anti-ESD precautions. Ensure that personnel and equipment are properly grounded. Cover workbenches with grounded conductive mats.
- Always turn the power supply off before inserting or removing the device from its socket.
- Protect leads with a conductive sheet when handling or transporting PC boards with devices.

## ■ ELECTRICAL CHARACTERISTICS

($V_{CC}$ = 2.7 V to 3.5 V, Ta = –30°C to +80°C)

| Parameter | | Symbol | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| Power supply current | | $I_{CC1}$ | — | 3.5 (0.1) | — | mA | PLL1, $V_{CC}$ = 3.0 V, Ta = 25°C, PLL-locked. Figures in parentheses ( ) are for the power saving mode. |
| | | $I_{CC2}$ | — | 6.0 (0.1) | — | mA | PLL2, $V_{CC}$ = 3.0 V, Ta = 25°C, PLL-locked. Figures in parentheses ( ) are for the power saving mode. |
| Operating frequency | fin1 | fin1 | 100 | — | 400 | MHz | PLL1, 1000 pF, AC-coupled |
| | fin2 | fin2 | 100 | — | 1100 | MHz | PLL2, 1000 pF, AC-coupled |
| | $OSC_{IN}$ | fosc | — | 12.8 | 20.0 | MHz | |
| Input sensitivity | fin1 | $P_{fin1}$ | –10 | — | 4 | dBm | PLL1, 50 Ω, AC-coupled |
| | fin2 | $P_{fin2}$ | –10 | — | 4 | dBm | PLL2, 50 Ω, AC-coupled |
| | $OSC_{IN}$ | $V_{OSC}$ | 0.5 | — | — | $V_{P-P}$ | |
| Input voltage | Excluding fin and $OSC_{IN}$ | $V_{IH}$ | 0.7 × $V_{CC}$+0.4 | | — | V | |
| | | $V_{IL}$ | — | — | 0.3 × $V_{CC}$–0.4 | V | |
| Input current | Data, Clock, LE | $I_{IH}$ | — | 1.0 | — | µA | |
| | | $I_{IL}$* | — | –1.0 | — | µA | |
| | $OSC_{IN}$ | $I_{OSC}$ | — | ±50 | — | µA | |
| Output voltage | Excluding $D_O$ and $OSC_{OUT}$ | $V_{OH}$ | 2.2 | — | — | V | $V_{CC}$ = 3.0 V |
| | | $V_{OL}$ | — | — | 0.4 | V | |
| High impedance cutoff current | $D_O$, BS | $I_{OFF}$ | — | — | 1.1 | µA | $V_P$ = $V_{CC}$ to 6.0 V $V_{OOP}$ = GND to 6.0 V |
| Output current | Excluding $D_O$ and $OSC_{OUT}$ | $I_{OH}$* | –1.0 | — | — | mA | |
| | | $I_{OL}$ | 1.0 | — | — | mA | |
| | $D_{O1}$ | $I_{OH1}$* | — | –1 | — | mA | $V_P$ = 6.0 V, Ta = 25°C, $V_{OH1}$ = 5 V |
| | | $I_{OL1}$ | — | 12 | — | mA | $V_{CC}$ = 3.0 V, Ta = 25°C, $V_{OL1}$ = 1 V |
| | $D_{O2}$ | $I_{OH2}$* | — | –3 | — | mA | $V_P$ = 6.0 V, Ta = 25°C, $V_{OH2}$ = 5 V |
| | | $I_{OL2}$ | — | 6 | — | mA | $V_{CC}$ = 3.0 V, Ta = 25°C, $V_{OL2}$ = 1 V |
| Analog switch on resistance | | $R_{ON}$ | — | 50 | — | Ω | |

* : The minus (–) sign indicates that the current is flowing out of the device.

## ■ FUNCTIONAL DESCRIPTIONS

**1. Pulse Swallow Function**

Calculate the divide ratio using the following equation:

$$f_{VCO} = [(P \times N) + A] \times f_{OSC} \div R$$

$f_{VCO}$ : Output frequency of external voltage controlled oscillator (VCO)
N : Preset divide ratio of binary 11-bit programmable counter (16 to 2,047)
A : Preset divide ratio of binary 7-bit swallow counter (0 to 127, and A < N)
$f_{OSC}$ : Reference oscillation frequency ($OSC_{IN}$ input frequency)
R : Preset divide ratio of reference counter (8 to 16,383)
P : Prescaler divide ratio of PLL1 (32 or 64) / PLL2 (64 or 128)

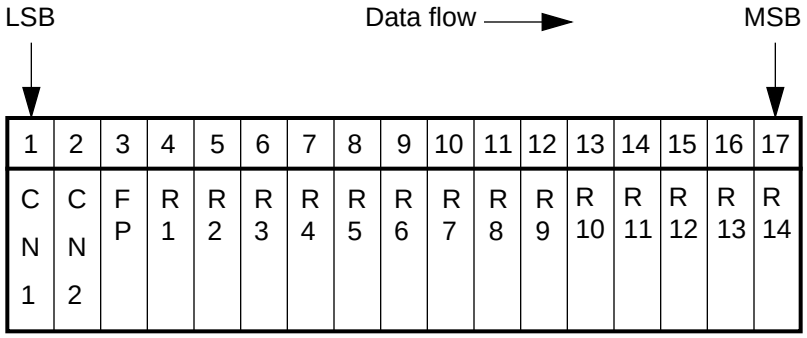
**2. Serial Data Input**

Serial data is entered using three pins (Data, Clock, and LE). The reference divider, PLL1 programmable divider, and PLL2 programmable divider are controlled separately.
Binary serial data is entered through the Data pin.
One bit of serial data is transferred into the shift register on the rising edge of the clock. When the load enable signal is high, the data stored in the shift register is transferred to the latch according to the control bit data setting.

| Control data | Reference counter | PLL1 programmable counter | PLL2 programmable counter |
|---|---|---|---|
| CN1 | L | L | H |
| CN2 | L | H | H |

(1) Shift register configuration

Programmable Reference Counter




| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CN1 | CN2 | FP | R1 | R2 | R3 | R4 | R5 | R6 | R7 | R8 | R9 | R10 | R11 | R12 | R13 | R14 |

R1 to R14 : Divide ratio setting bits for the programmable reference counter (8 to 16,383)
FP : Test purpose bit (selects fp1 or fp2 monitor output)
CN1, 2 : Control bits

Note: Start data input with MSB first.

*(Continued)*

*(Continued)*

- Programmable Counter

LSB → Data flow → MSB

| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CN1 | CN2 | PS | PRE | FC | A1 | A2 | A3 | A4 | A5 | A6 | A7 | N1 | N2 | N3 | N4 | N5 | N6 | N7 | N8 | N9 | N10 | N11 |

N1 to N11 : Divide ratio setting bits for the programmable counter (16 to 2,047)
A1 to A7 : Divide ratio setting bits for the swallow counter (0 to 127)
FC : Phase switching bit for the phase comparator
PRE : Divide ratio setting bit for the prescaler
PS : Power saving control bit
CN1, 2 : Control bits

Note: Start data input with MSB first.

(2) Data setting

- Binary 14-bit reference counter

| Divide ratio (R) | R14 | R13 | R12 | R11 | R10 | R9 | R8 | R7 | R6 | R5 | R4 | R3 | R2 | R1 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 9 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| • | • | • | • | • | • | • | • | • | • | • | • | • | • | • |

Note: A divide ratio less than 8 is prohibited. (Setting range = 8 to 16,383)

- Binary 11-bit programmable counter

| Divide ratio (N) | N11 | N10 | N9 | N8 | N7 | N6 | N5 | N4 | N3 | N2 | N1 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 16 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 17 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| • | • | • | • | • | • | • | • | • | • | • | • |

Note: A divide ratio less than 16 is prohibited. (Setting range = 16 to 2,047)

- Binary 7-bit swallow counter

| Divide ratio (A) | A7 | A6 | A5 | A4 | A3 | A2 | A1 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| • | • | • | • | • | • | • | • |

(Setting range = 0 to 127)

• PRE: Prescaler

| | PRE = "H" | PRE = "L" |
|---|---|---|
| PLL1 prescaler divide ratio | Divide by 32/33 | Divide by 64/65 |
| PLL2 prescaler divide ratio | Divide by 64/65 | Divide by 128/129 |

Note: Set the programmable divide ratios for PLL1 and PLL2 from the serial data.

• PS: Power saving control

| | PS = "H" | PS = "L" |
|---|---|---|
| PLL1 | On | Off |
| PLL2/Common circuits | On | Off |

Notes:
- Set the comparative divider values for PLL1 and PLL2 from the serial data.
- The common circuits are the crystal oscillator circuit and the reference counter.
- When turning on the power, always set PS to "L" once.

Intermittent operation reduces the overall circuit power consumption by only operating the internal circuit when required (the circuit halts when not required). However, simply switching the circuit from the halted to the operating state results in a large error signal output from the phase comparator. This is because the phase relationship between the reference frequency (fr) and the comparative frequency (fp) inputs to the phase comparator is undefined during such a start-up condition, even if the two frequencies are the same. As a result, the PLL loses its locked state. To prevent this problem, an intermittent operation control circuit is provided to forcibly align the phases on startup and therefore minimize the variation in the locked frequency.

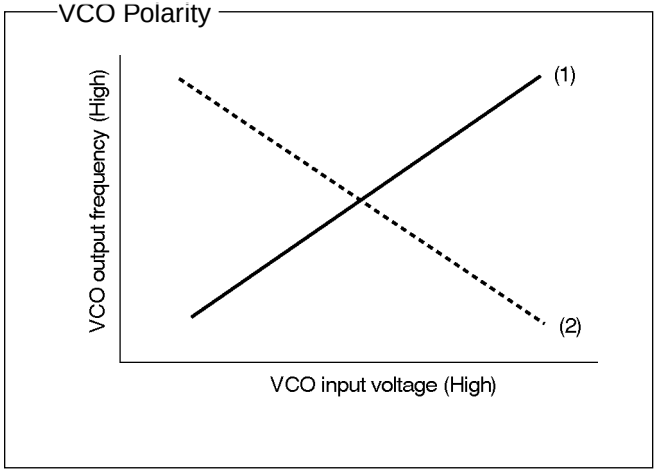
• FC: Phase switching bit for the phase comparator

This bit sets the charge pump output polarity ($D_O$) as follows.

| | FC = "H" | FC = "L" |
|---|---|---|
| fr > fp | H | L |
| fr < fp | L | H |
| fr =fp | Z | Z |
| VCO polarity | (1) | (2) |

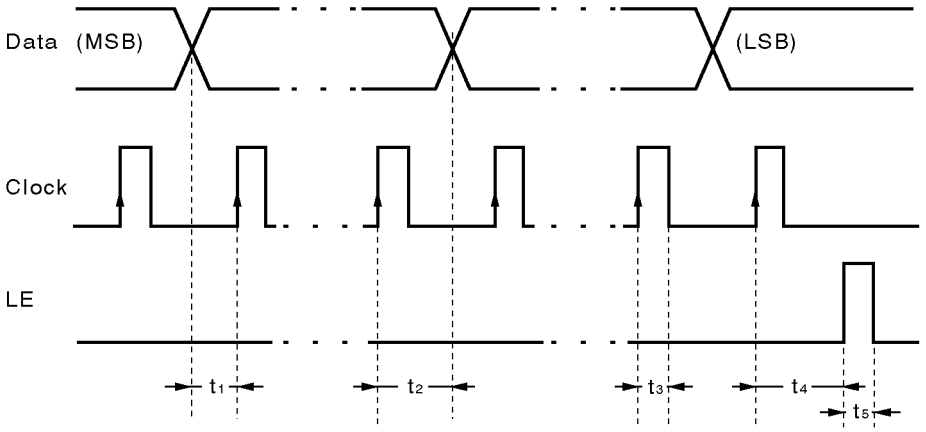
Z: High impedance

Notes:
- When designing the PLL frequency synthesizer, set the FC bit according to the VCO polarity.
- Set the comparative divider values for PLL1 and PLL2 from the serial data.
- Take note of the polarity when using an active lowpass filter.



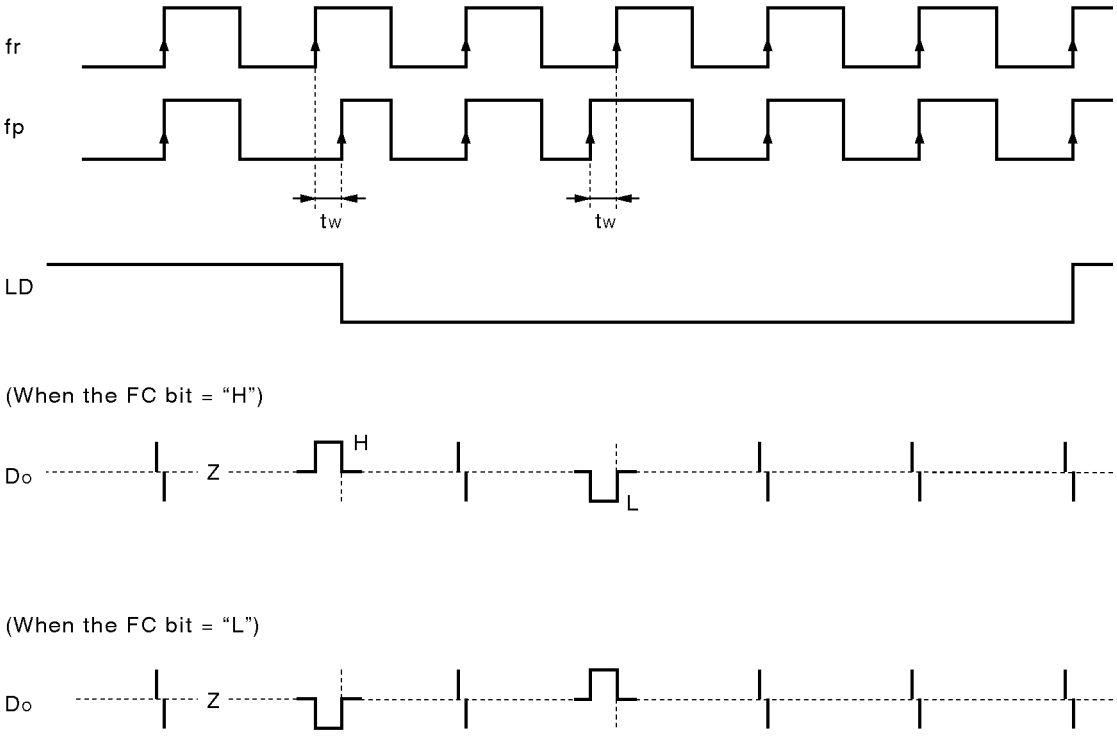
(3) Serial data input timing

- $t_1 > 100ns$, $t_2 > 1000ns$, $t_3 > 300ns$, $t_4 > 100ns$, $t_5 > 800ns$




Note: Data is loaded on the rising edge of the clock.

**3. Phase Comparator Output Waveform**




Notes: • The phase detection range is $-2\pi$ to $+2\pi$.

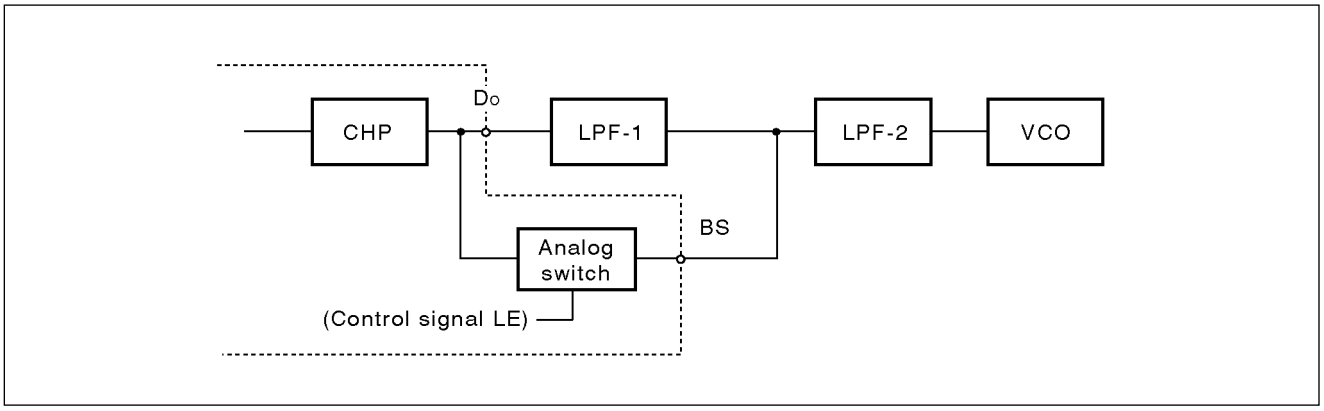
• The LD output becomes "L" when the phase error is more than $t_w$ and "H" when the phase error is less than $t_w$ and continues to be so for three cycles or more.
($t_w$ = 625 ns to 1250 ns for $f_{osc}$ = 12.8 MHz)

**4. Analog Switch**

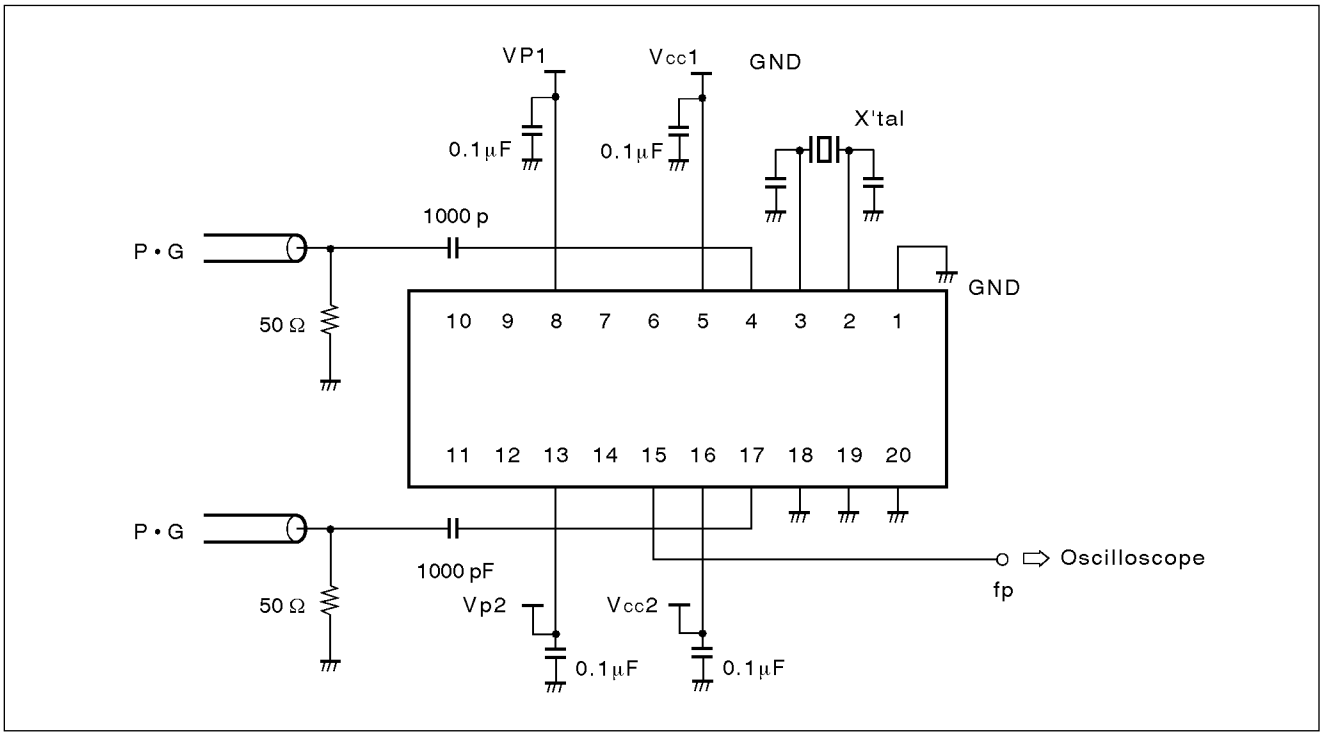
The analog switch is set on or off by the control data and LE signal settings. When the switch is on, the BSC1 and BSC2 pins output the charge pump outputs ($D_O1$ and $D_O2$). (These pins take high impedance when the switch is off.)

| | Setting the PLL1 programmable divider (CN1 = "L", CN2 = "H") | | Setting the PLL2 programmable divider (CN1 = "H", CN2 = "H") | |
|---|---|---|---|---|
| | **LE = "H"** | **LE = "L"** | **LE = "H"** | **LE = "L"** |
| PLL1 analog switch | On | Off | Off | Off |
| PLL2 analog switch | Off | Off | On | Off |

As shown in the following example, placing the analog switch midway through the LPF (LPF1 + LPF2) allows the LPF time constant to be reduced during PLL channel switching so as to reduce lock up time.



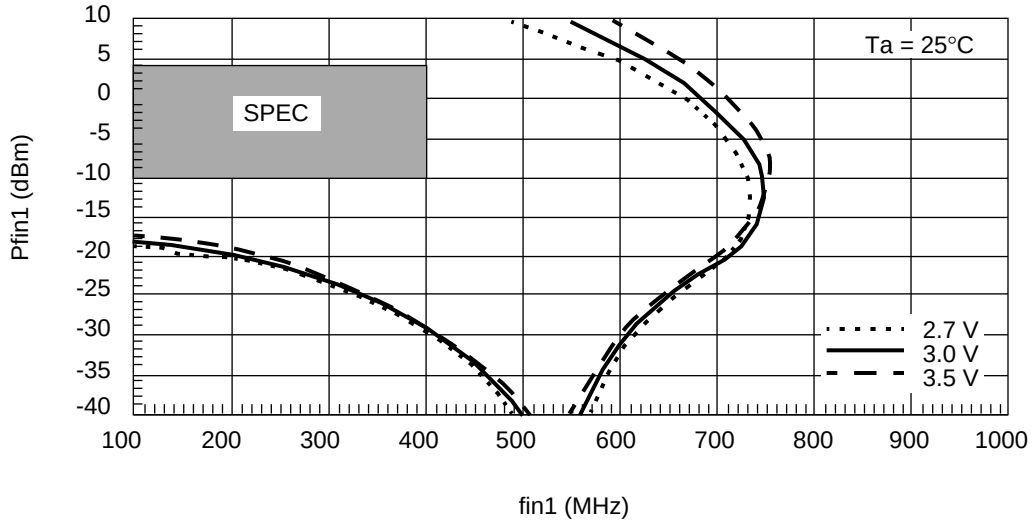
## ■ TEST CIRCUIT EXAMPLE (Prescaler Input Sensitivity Measurement)



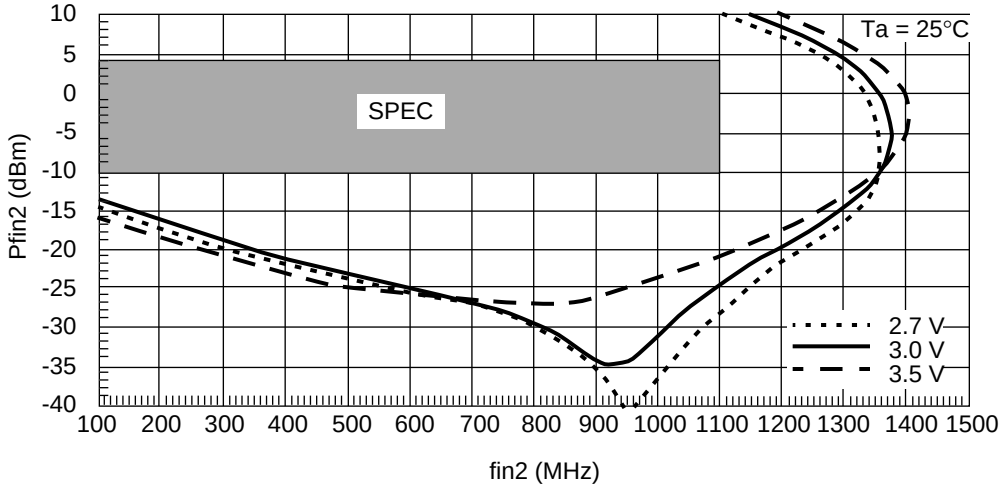
## ■ TYPICAL CHARACTERISTIC CURVES

### 1. fin Input Sensitivity Characteristics

**PLL1 Input Sensitivity vs. Input Frequency**

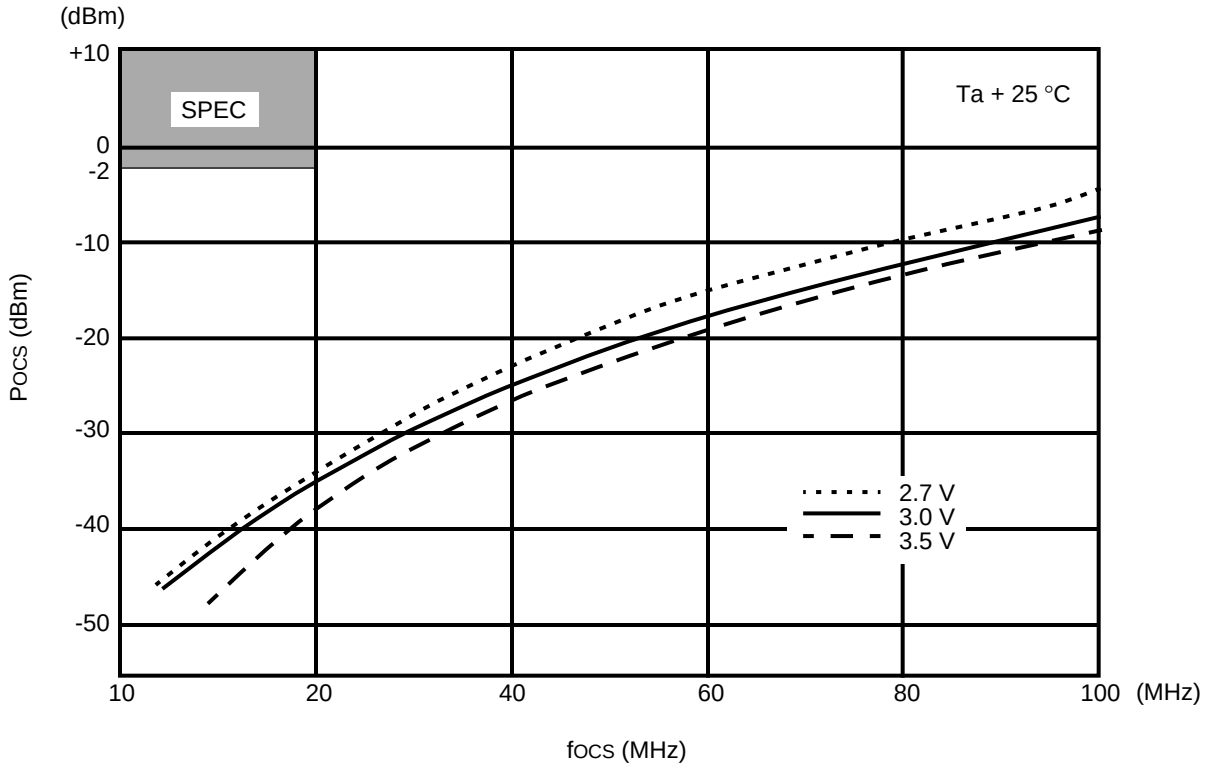



**PLL2 Input Sensitivity vs. Input Frequency**



**2. $OSC_{IN}$ Input Sensitivity Characteristics**

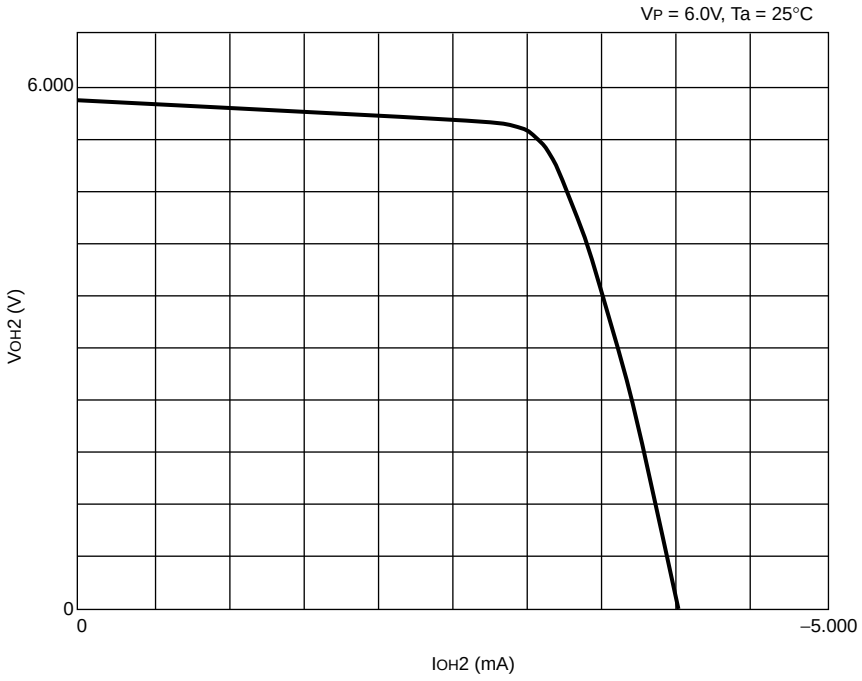
**Input Sensitivity vs. Input Frequency**



### 3. $D_O$ Output Current Characteristics

**“H” level output current vs. “H” level output voltage (PLL1)**

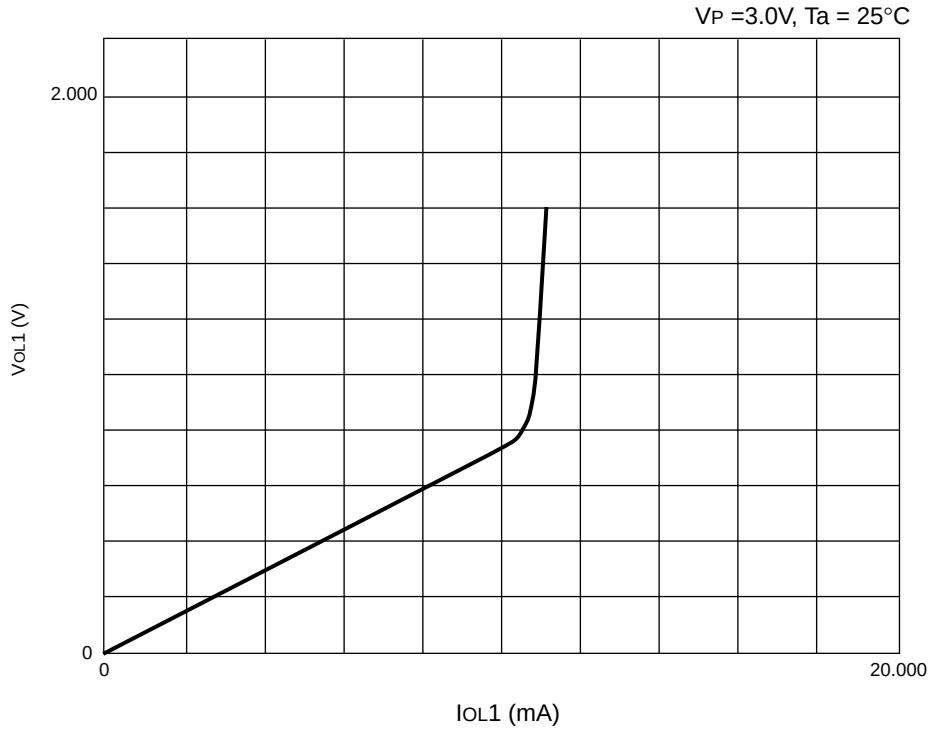

**“H” level output current vs. “H” level output voltage (PLL2)**




*(Continued)*

*(Continued)*

**“L” Level Output Current vs. “L” Level Output Voltage (PLL1)**

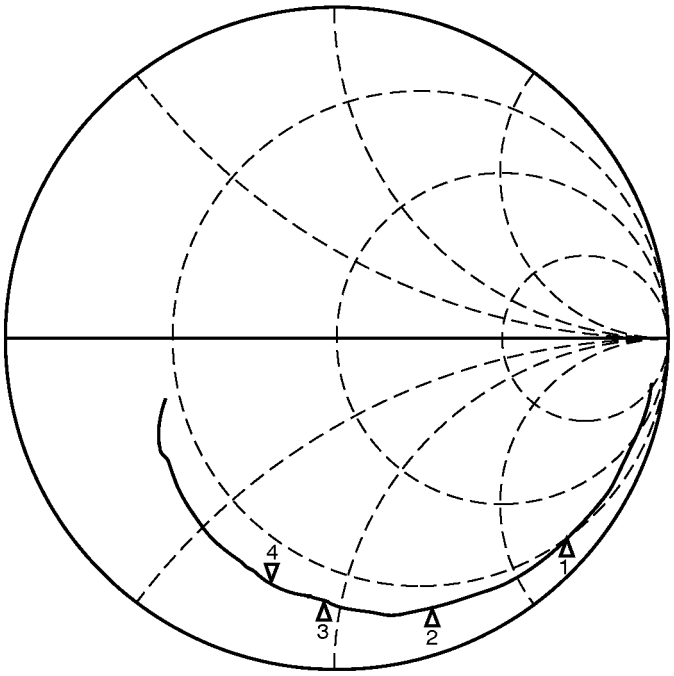



**“L” Level Output Current vs. “L”Level Output Voltage (PLL2)**

**4. Input Impedance Characteristics**

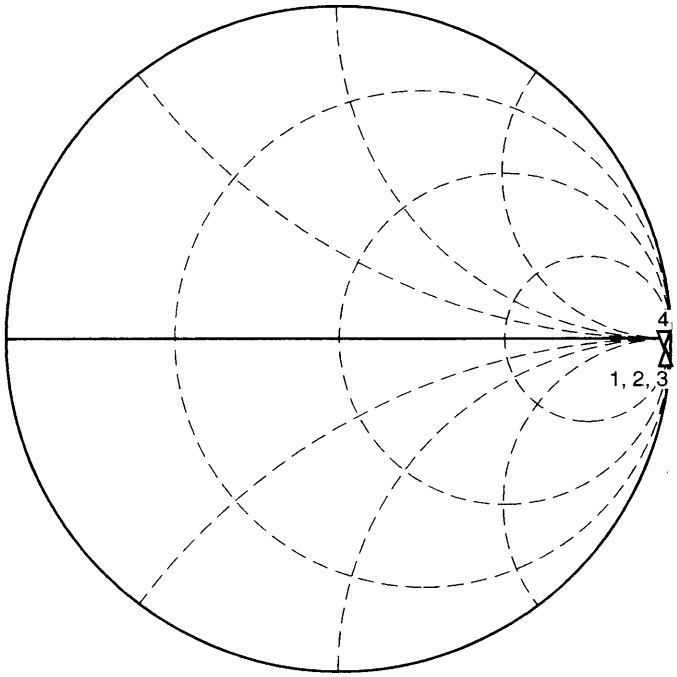
**fin Input Impedance Characteristics**

**fin**

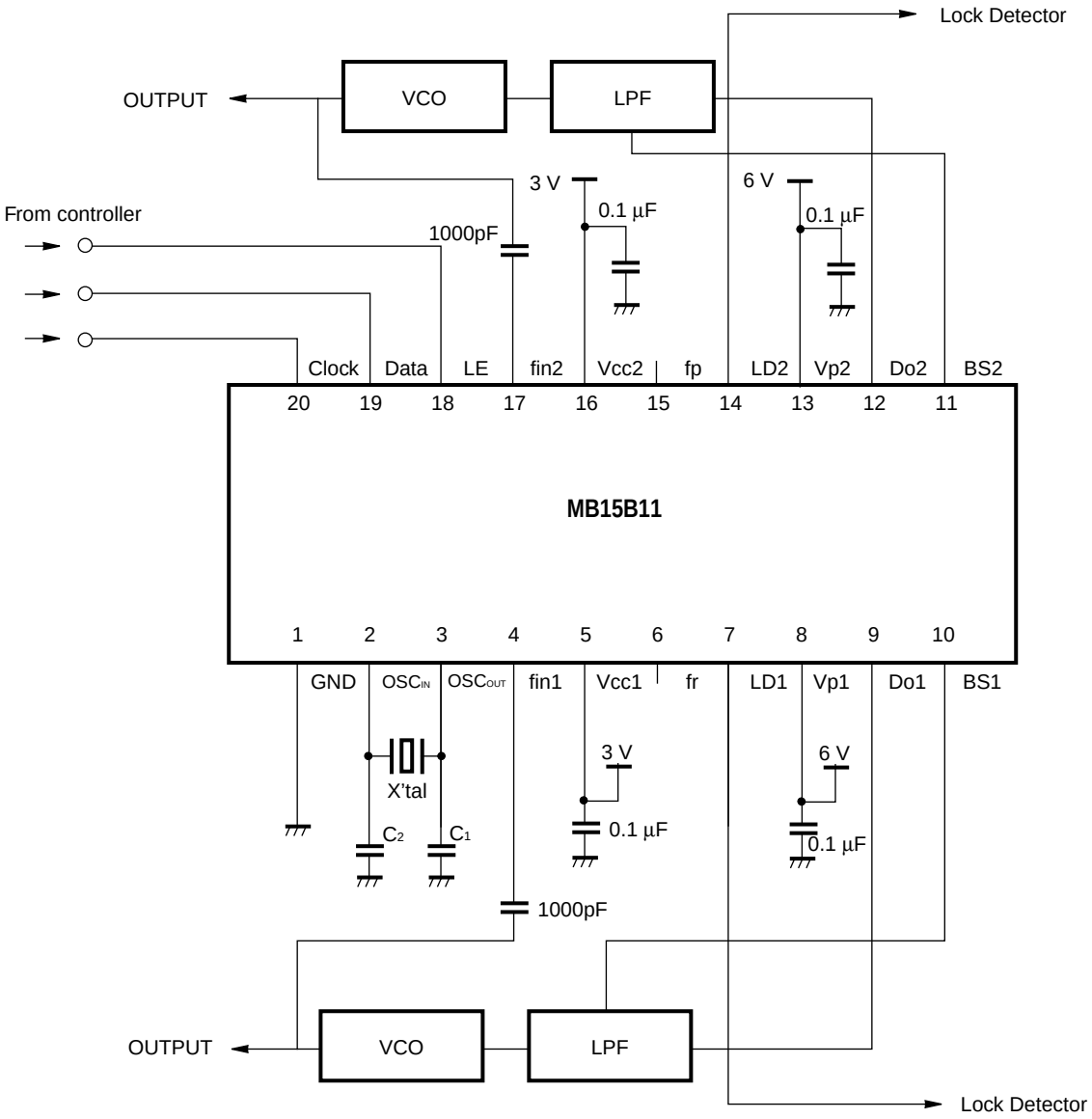



**$OSC_{IN}$ Input Impedance Characteristics**

**$OSC_{IN}$**



## ■ APPLICATION EXAMPLE

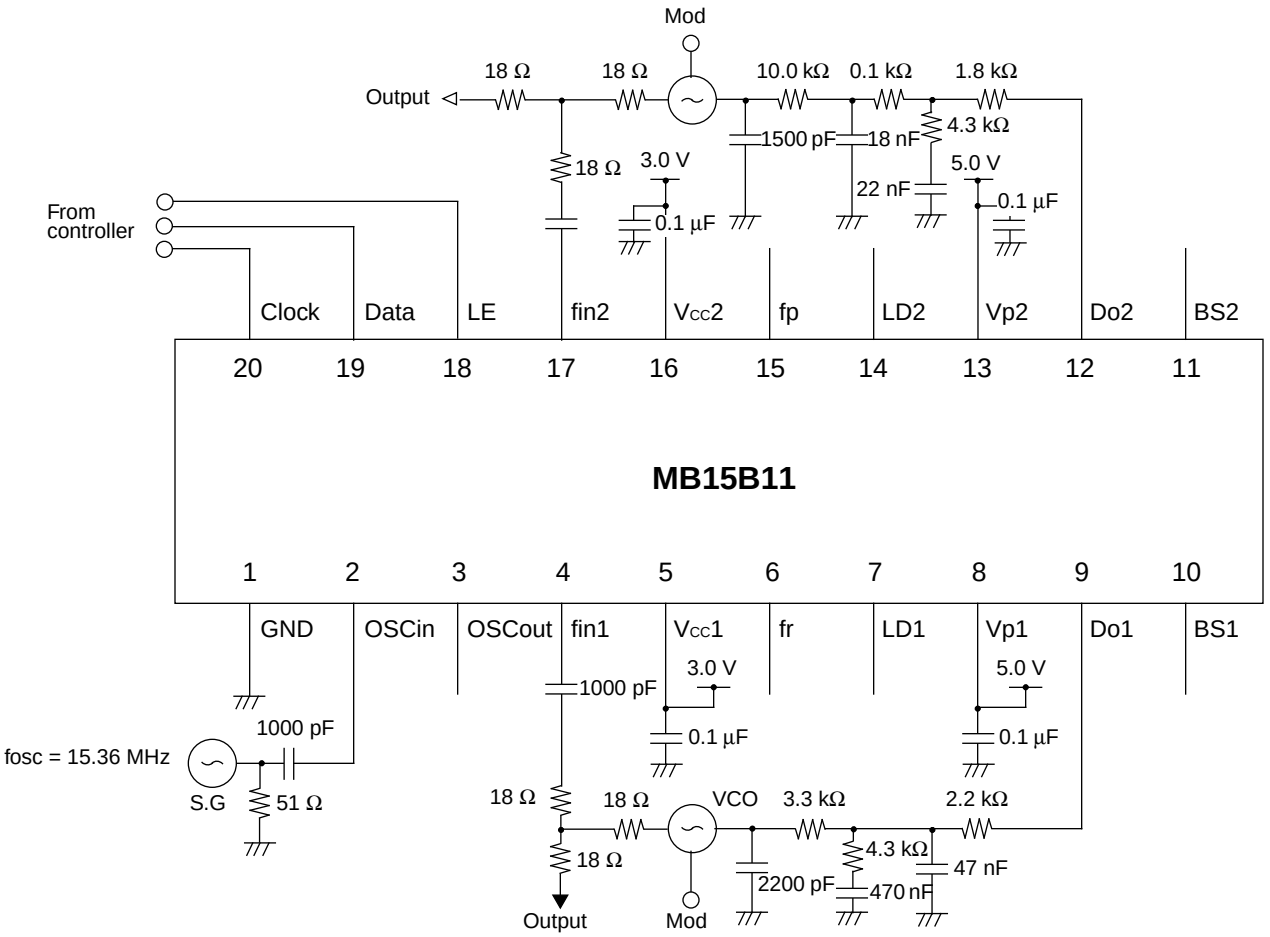



X'tal :12.8 MHz
Clock, Data, LE : Internal schmitt trigger circuits (Insert a pull-down resistor if an input is open.)
C1, C2 : Determined by the crystal oscillator.
Vp1, Vp2 : Up to 6 V

*(Continued)*

*(Continued)*

**AMPS Application**



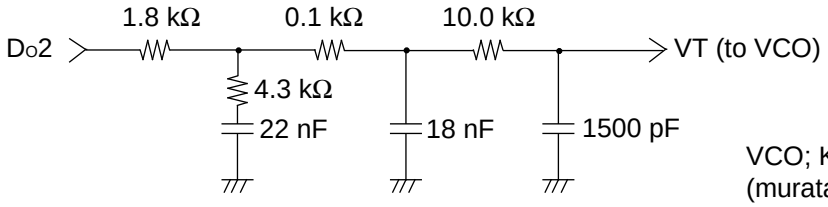
## ■ APPLICATION INFORMATION (AMPS)

### PLL Characteristics (Rx mode)

fr = 30 kHz/$V_{CC}$ = 3.0 V, Vp = 5.0 V, $V_{VCO}$ = 5.0 V

| Parameter | | Measured Value | Conditions |
|---|---|---|---|
| Hopping time | Lch → Hch | 18.4 mS | 825.6 MHz → 850.5 MHz, within ± 800 Hz |
| | Hch ← Lch | 16.4 mS | 850.5 MHz → 825.6 MHz, within ± 800 Hz |
| Spurious level | | 79 dBc | ± 30 kHz offset at 835.20 MHz |
| Phase noise | | 73 dBc/Hz | ± 1 kHz offset at 835.20 MHz |

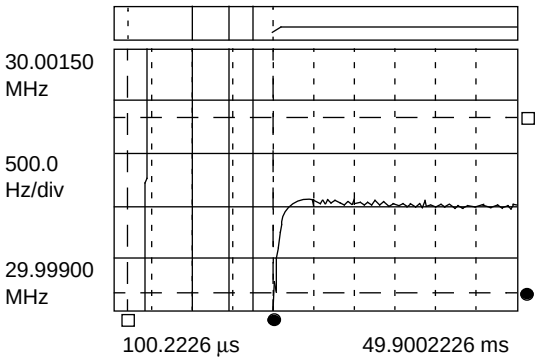
### Loop Filter Schematics (Rx mode)



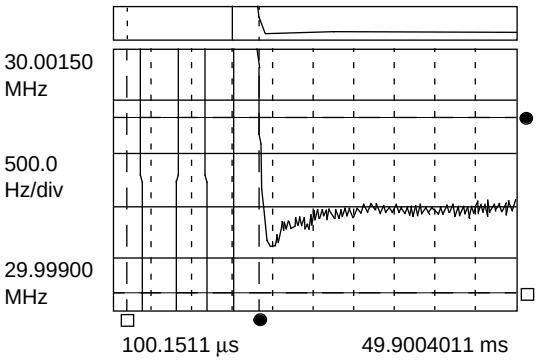

VCO; Kv = 9.7 MHz/V
(murata MQC505-836)

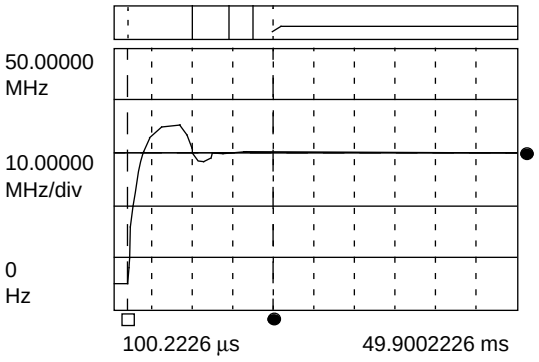
### PLL Hopping Time (Rx mode)

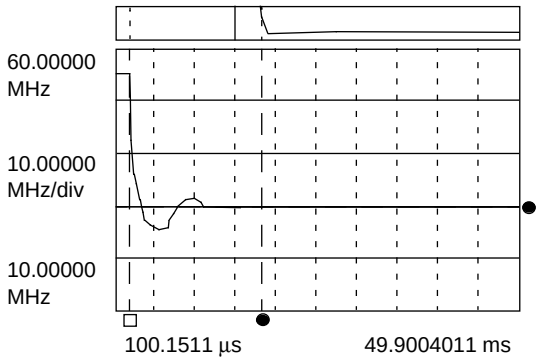
825.60 MHz → 850.50 MHz, within ± 800 Hz
Lch → Hch 18.4 mS




850.50 MHz → 825.60 MHz, within ± 800 Hz
Hch → Lch 16.4 mS



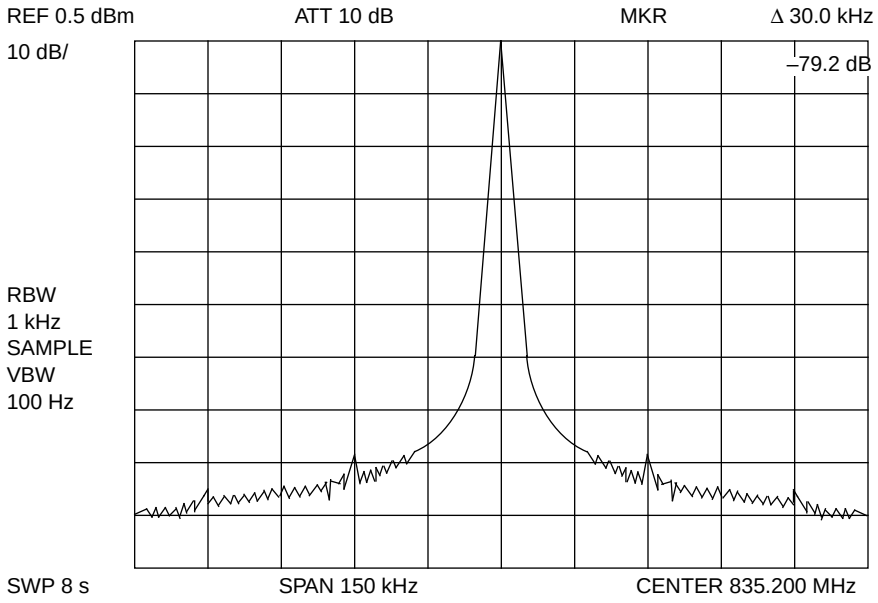



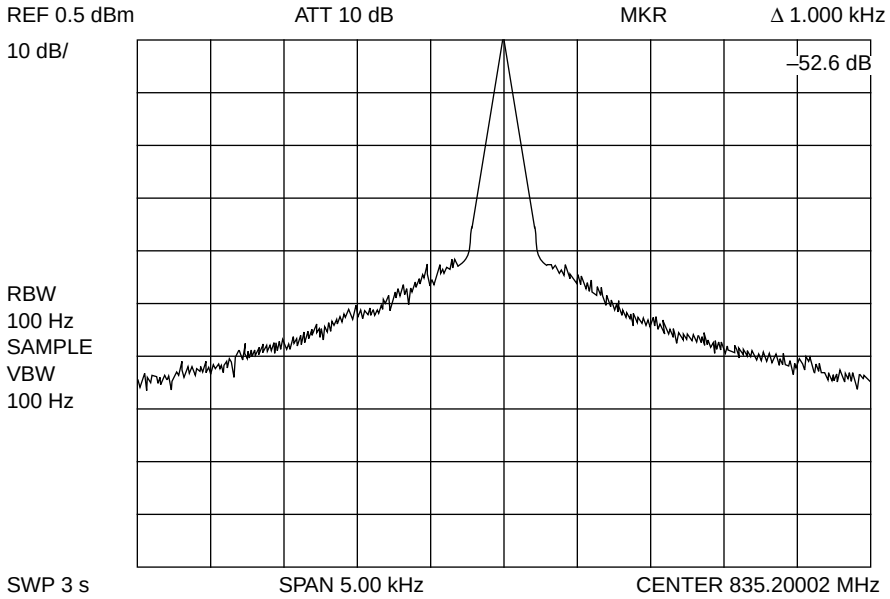

*(Continued)*

*(Continued)*

### Spurious Level (Rx mode)




### Phase Noise (Rx mode)




*(Continued)*

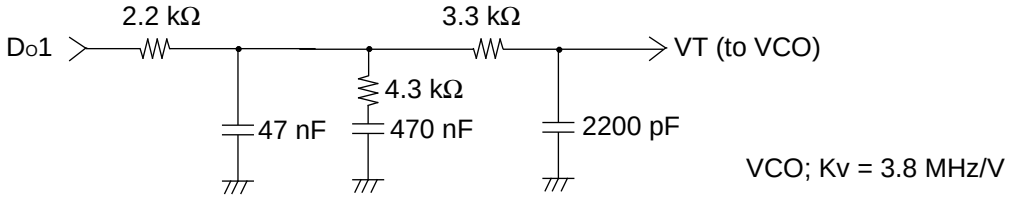
*(Continued)*

### PLL Characteristics (Tx mode)

fr = 30 kHz/$V_{CC}$ = 3.0 V, Vp = 5.0 V, $V_{VCO}$ = 5.0 V

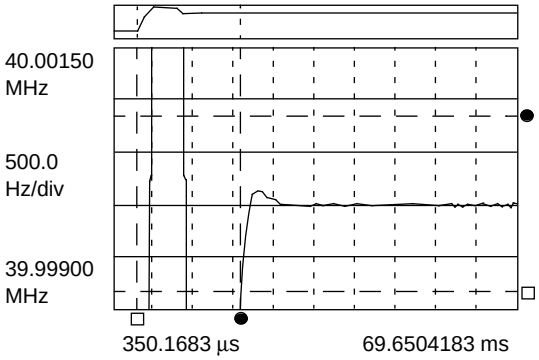
| Parameter | | Measured Value | Conditions |
|---|---|---|---|
| Hopping time | Lch → Hch | 17.5 mS | 376.8 MHz → 385.8 MHz, within ± 800 Hz |
| | Hch ← Lch | 18.9 mS | 385.8 MHz → 376.8 MHz, within ± 800 Hz |
| Spurious level | | 87 dBc | ± 30 kHz offset at 382.20 MHz |
| Phase noise | | 81 dBc/Hz | ± 1 kHz offset at 382.20 MHz |

### Loop Filter Schematics (Tx mode)

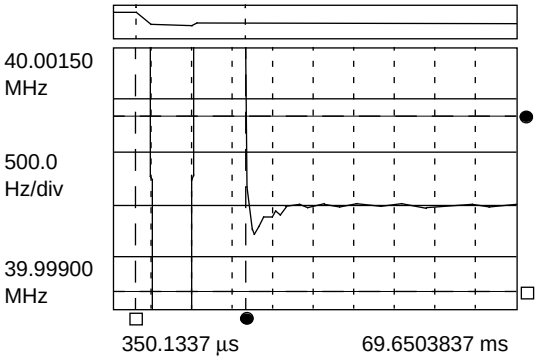


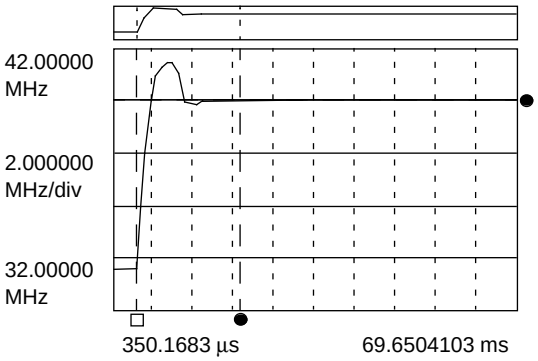

### PLL Hopping Time (Tx mode)

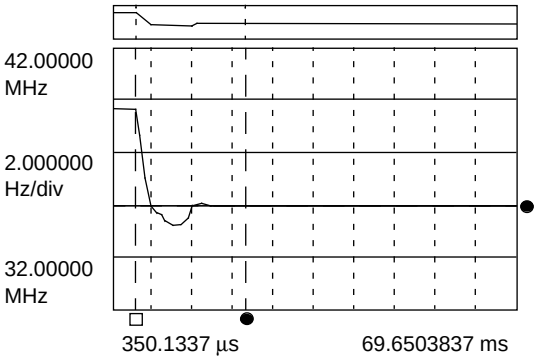
376.80 MHz → 385.80 MHz, within ± 800 Hz
Lch → Hch 17.5 mS




385.80 MHz → 376.80 MHz, within ± 800 Hz
Hch → Lch 18.9 mS



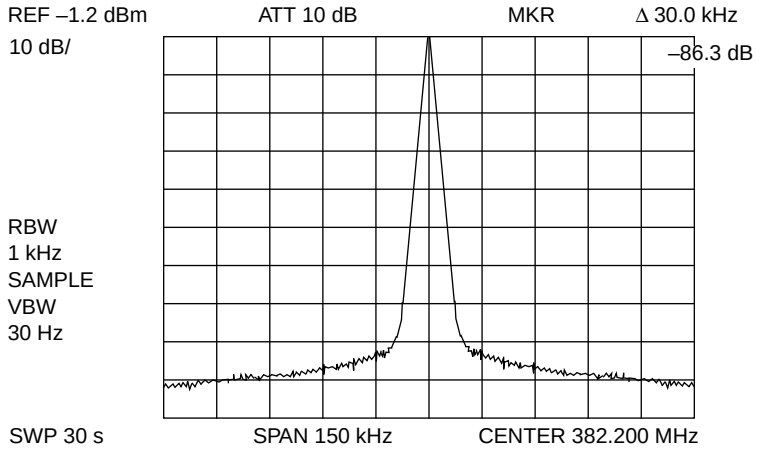



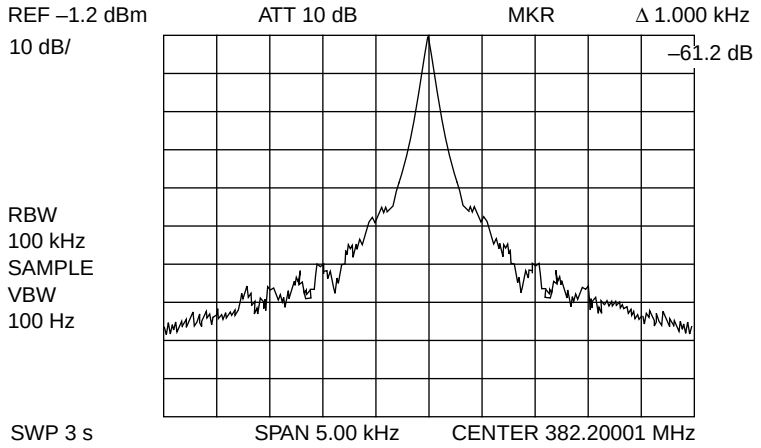

*(Continued)*

*(Continued)*

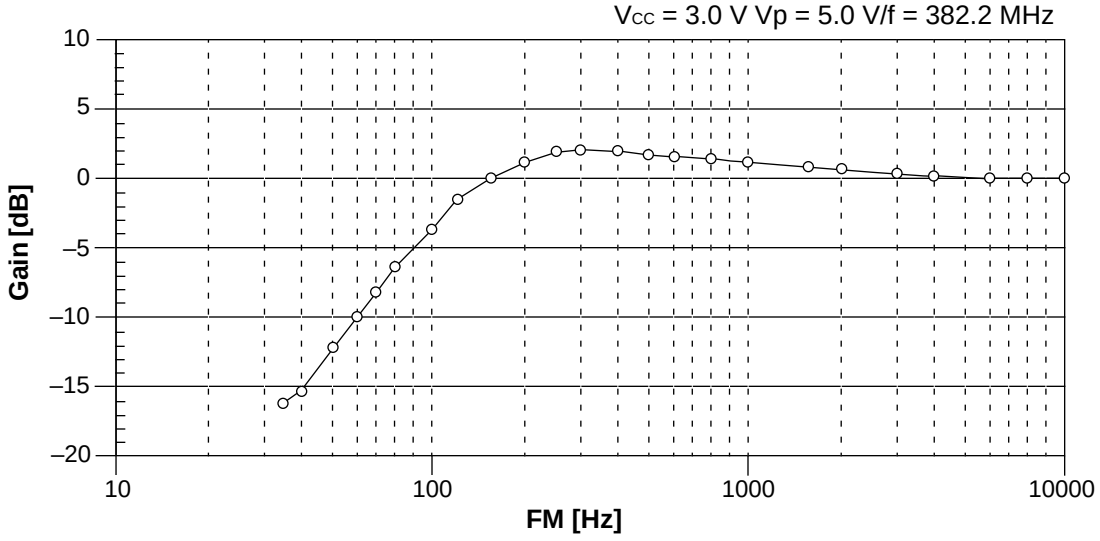
### Spurious Level (Tx mode)




### Phase Noise (Tx mode)




### Modulation Linearity (Tx mode)



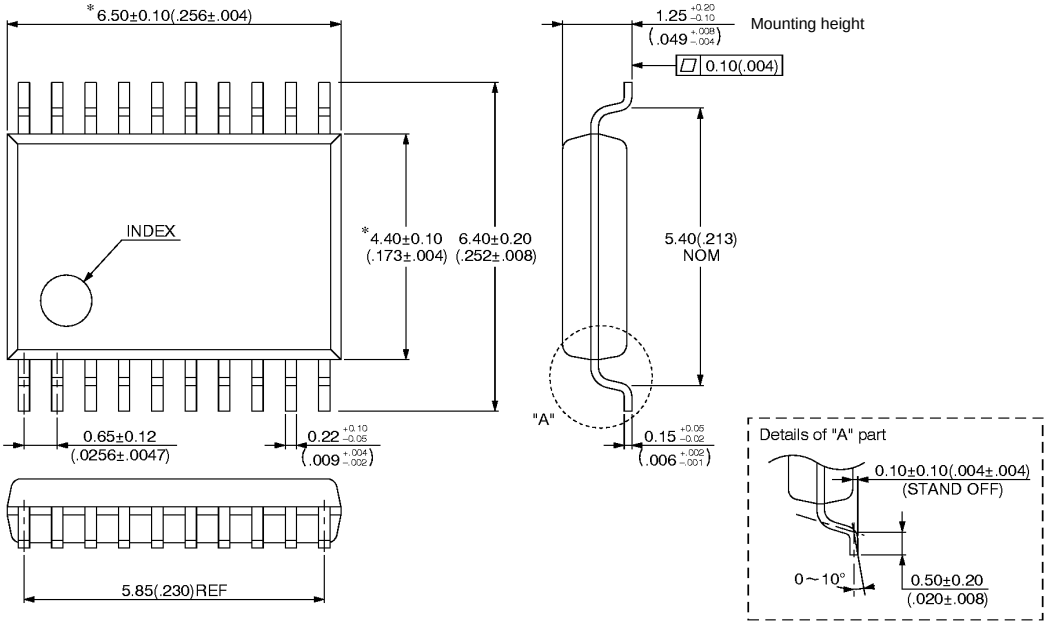
## ■ ORDERING INFORMATION

| Part number | Package | Remarks |
|---|---|---|
| MB15B11PFV | 20-pin, plastic SSOP<br>(FPT-20P-M03) | |

## ■ PACKAGE DIMENSIONS

20-pin, plastic SSOP
(FPT-20P-M03)

*: These dimensions do not include resin protrusion.






Dimensions in mm (inches)

## http://www.fujitsumicro.com

### Customer Response Center:

For semiconductor products, flat panel displays, and PC cards in the U.S., Canada, and Mexico, please contact the Fujitsu Microelectronics Customer Response Center (CRC). The CRC provides a single point of contact for resolving customer issues and answering technical questions.

**Web:** Click on Tech Support in the FMI home page, then submit our form.

**Tel:** Telephone: 1-800-866-8608 Monday through Friday, 7 to 5 PST. Outside U.S., Canada, and Mexico, call: 010-1-408-922-9000 and ask for the Customer Response Center. *(Note: Country code may vary.)*

**Fax:** (408) 922-9179

**E-Mail:** fmicrc@fmi.fujitsu.com

**CP-TC-DS-20297-7/96**