

## FSTUD16211

### 24-Bit Bus Switch with -2V Undershoot Protection and Level Shifting

#### General Description

The Fairchild Switch FSTUD16211 provides 24-bits of high-speed CMOS TTL-compatible bus switching. The low on resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise. A diode to  $V_{CC}$  has been integrated into the circuit to allow for level shifting between 5V inputs and 3.3V outputs.

The device is organized as a 12-bit or 24-bit bus switch. When  $\overline{OE}_1$  is LOW, the switch is ON and Port 1A is connected to Port 1B. When  $\overline{OE}_2$  is LOW, Port 2A is connected to Port 2B. When  $\overline{OE}_{1/2}$  is HIGH, a high impedance state exists between the A and B Ports. The A and B Ports have "undershoot hardened" circuit protection to support an extended range to 2.0V below ground. Fairchild's integrated Undershoot Hardened Circuit (UHC™) senses undershoot at the I/O's, and responds by preventing voltage differentials from developing and turning on the switch.

#### Features

- Undershoot hardened to -2V (A and B Ports)
- Voltage level shifting
- 4Ω switch connection between two ports
- Minimal propagation delay through the switch
- Low  $I_{CC}$
- Zero bounce in flow-through mode
- Control inputs compatible with TTL level
- See Applications Note AN-5008 for details
- Also packaged in plastic Fine-Pitch Ball Grid Array (FBGA) (Preliminary)

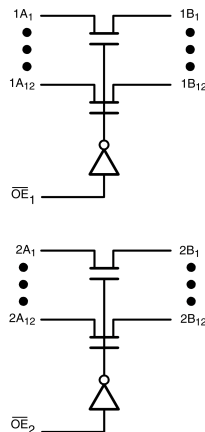
#### Ordering Code:

| Order Number             | Package Number          | Package Description   |
|--------------------------|-------------------------|---|
| FSTUD16211GX<br>(Note 1) | BGA54A<br>(Preliminary) | 54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide [TAPE and REEL] |
| FSTUD16211MTD            | MTD56                   | 56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide         |

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

**Note 1:** BGA package available in Tape and Reel only.

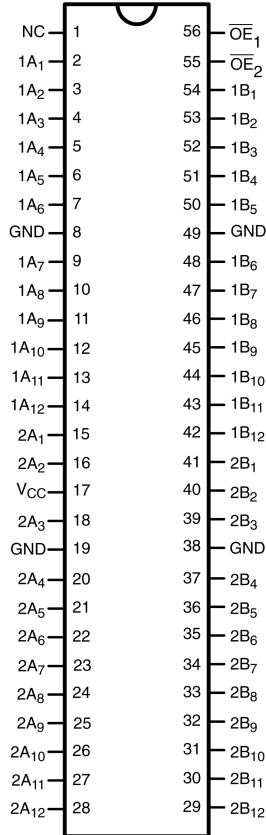
#### Logic Diagram



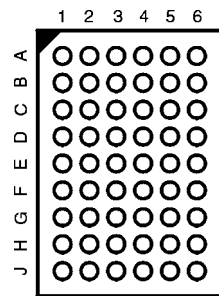
UHC™ is a trademark of Fairchild Semiconductor Corporation.

## Connection Diagrams

Pin Assignment for TSSOP



Pin Assignment for FBGA



(Top Thru View)

## Pin Descriptions

| Pin Name                           | Description        |
|------------------------------------|--------------------|
| $\overline{OE}_1, \overline{OE}_2$ | Bus Switch Enables |
| 1A, 2A                             | Bus A              |
| 1B, 2B                             | Bus B              |
| NC                                 | No Connect         |

## Pin Assignment for FBGA

|          | 1                | 2                | 3                | 4                | 5                | 6                |
|----------|------------------|------------------|------------------|------------------|------------------|------------------|
| <b>A</b> | 1A <sub>2</sub>  | 1A <sub>1</sub>  | NC               | OE <sub>2</sub>  | 1B <sub>1</sub>  | 1B <sub>2</sub>  |
| <b>B</b> | 1A <sub>4</sub>  | 1A <sub>3</sub>  | 1A <sub>7</sub>  | OE <sub>1</sub>  | 1B <sub>3</sub>  | 1B <sub>4</sub>  |
| <b>C</b> | 1A <sub>6</sub>  | 1A <sub>5</sub>  | GND              | 1B <sub>7</sub>  | 1B <sub>5</sub>  | 1B <sub>6</sub>  |
| <b>D</b> | 1A <sub>10</sub> | 1A <sub>9</sub>  | 1A <sub>8</sub>  | 1B <sub>8</sub>  | 1B <sub>9</sub>  | 1B <sub>10</sub> |
| <b>E</b> | 1A <sub>12</sub> | 1A <sub>11</sub> | 2A <sub>1</sub>  | 2B <sub>1</sub>  | 1B <sub>11</sub> | 1B <sub>12</sub> |
| <b>F</b> | 2A <sub>4</sub>  | 2A <sub>3</sub>  | 2A <sub>2</sub>  | 2B <sub>2</sub>  | 2B <sub>3</sub>  | 2B <sub>4</sub>  |
| <b>G</b> | 2A <sub>6</sub>  | 2A <sub>5</sub>  | V <sub>CC</sub>  | GND              | 2B <sub>5</sub>  | 2B <sub>6</sub>  |
| <b>H</b> | 2A <sub>8</sub>  | 2A <sub>7</sub>  | 2A <sub>9</sub>  | 2B <sub>9</sub>  | 2B <sub>7</sub>  | 2B <sub>8</sub>  |
| <b>J</b> | 2A <sub>12</sub> | 2A <sub>11</sub> | 2A <sub>10</sub> | 2B <sub>10</sub> | 2B <sub>11</sub> | 2B <sub>12</sub> |

## Truth Table

| Inputs            |                   | Inputs/Outputs |         |
|-------------------|-------------------|----------------|---------|
| $\overline{OE}_1$ | $\overline{OE}_2$ | 1A, 1B         | 2A, 2B  |
| L                 | L                 | 1A = 1B        | 2A = 2B |
| L                 | H                 | 1A = 1B        | Z       |
| H                 | L                 | Z              | 2A = 2B |
| H                 | H                 | Z              | Z       |

| Absolute Maximum Ratings (Note 2)                  |                  | Recommended Operating Conditions (Note 5) |                  |
|--|------------------|---|------------------|
| Supply Voltage ( $V_{CC}$ )                        | -0.5V to +7.0V   | Power Supply Operating ( $V_{CC}$ )       | 4.5V to 5.5V     |
| DC Switch Voltage ( $V_S$ ) (Note 3)               | -2.0V to +7.0V   | Input Voltage ( $V_{IN}$ )                | 0V to 5.5V       |
| DC Input Control Pin Voltage ( $V_{IN}$ ) (Note 4) | -0.5V to +7.0V   | Output Voltage ( $V_{OUT}$ )              | 0V to 5.5V       |
| DC Input Diode Current ( $I_{IK}$ ) $V_{IN} < 0V$  | -50 mA           | Input Rise and Fall Time ( $t_r, t_f$ )   |                  |
| DC Output ( $I_{OUT}$ )                            | 128 mA           | Switch Control Input                      | 0 ns/V to 5 ns/V |
| DC $V_{CC}/GND$ Current ( $I_{CC}/I_{GND}$ )       | +/- 100 mA       | Switch I/O                                | 0 ns/V to DC     |
| Storage Temperature Range ( $T_{STG}$ )            | -65°C to +150 °C | Free Air Operating Temperature ( $T_A$ )  | -40 °C to +85 °C |

**Note 2:** The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum rating. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**Note 3:**  $V_S$  is the voltage observed/applied at either A or B Ports across the switch.

**Note 4:** The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

**Note 5:** Unused control inputs must be held HIGH or LOW. They may not float.

### DC Electrical Characteristics

| Symbol          | Parameter                        | $V_{CC}$<br>(V) | $T_A = -40\text{ °C to }+85\text{ °C}$ |                 |      | Units | Conditions   |
|-----------------|----------------------------------|-----------------|--|-----------------|------|-------|--|
|                 |                                  |                 | Min                                    | Typ<br>(Note 6) | Max  |       |  |
| $V_{IK}$        | Clamp Diode Voltage              | 4.5             |  |                 | -1.2 | V     | $I_{IN} = -18\text{ mA}$   |
| $V_{IH}$        | HIGH Level Input Voltage         | 4.5-5.5         | 2.0                                    |                 |      | V     |  |
| $V_{IL}$        | LOW Level Input Voltage          | 4.5-5.5         |  |                 | 0.8  | V     |  |
| $V_{OH}$        | HIGH Level                       | 4.5-5.5         | See Figure 4                           |                 |      | V     |  |
| $I_I$           | Input Leakage Current            | 5.5             |  |                 | ±1.0 | µA    | $0 \leq V_{IN} \leq 5.5V$  |
|                 |                                  | 0               |  |                 | 10   | µA    | $V_{IN} = 5.5V$  |
| $I_{OZ}$        | OFF-STATE Leakage Current        | 5.5             |  |                 | ±1.0 | µA    | $0 \leq A, B \leq V_{CC}$  |
| $R_{ON}$        | Switch On Resistance<br>(Note 7) | 4.5             |  | 4               | 7    | Ω     | $V_{IN} = 0V, I_{IN} = 64\text{ mA}$   |
|                 |                                  | 4.5             |  | 4               | 7    | Ω     | $V_{IN} = 0V, I_{IN} = 30\text{ mA}$   |
|                 |                                  | 4.5             |  | 35              | 50   | Ω     | $V_{IN} = 2.4V, I_{IN} = 15\text{ mA}$   |
| $I_{CC}$        | Quiescent Supply Current         | 5.5             |  |                 | 1.5  | mA    | $OE_1 = OE_2 = GND$<br>$V_{IN} = V_{CC}$ or $GND, I_{OUT} = 0$                 |
|                 |                                  |                 |  |                 | 10   | µA    | $OE_1 = OE_2 = V_{CC}$<br>$V_{IN} = V_{CC}$ or $GND, I_{OUT} = 0$              |
| $\Delta I_{CC}$ | Increase in $I_{CC}$ per Input   | 5.5             |  |                 | 2.5  | mA    | One Input at 3.4V<br>Other Inputs at $V_{CC}$ or $GND$                         |
| $V_{IKU}$       | Voltage Undershoot               | 5.5             |  |                 | -2.0 | V     | $0.0\text{ mA} \geq I_{IN} \geq -50\text{ mA}$<br>$\overline{OE}_{1,2} = 5.5V$ |

**Note 6:** Typical values are at  $V_{CC} = 5.0V$  and  $T_A = +25^\circ C$

**Note 7:** Measured by the voltage drop between A and B pins at the indicated current through the switch. On Resistance is determined by the lower of the voltages on the two (A or B) pins.

## AC Electrical Characteristics

| Symbol                | Parameter                             | $T_A = -40\text{ }^\circ\text{C to } +85\text{ }^\circ\text{C}$ ,<br>$C_L = 50\text{pF}$ , $R_U = R_D = 500\Omega$ |      | Units | Conditions   | Figure No.   |
|-----------------------|---------------------------------------|--|------|-------|--|--------------|
|                       |                                       | $V_{CC} = 4.5 - 5.5\text{V}$   |      |       |  |              |
|                       |                                       | Min  | Max  |       |  |              |
| $t_{PHL}$ , $t_{PLH}$ | Propagation Delay Bus to Bus (Note 8) |  | 0.25 | ns    | $V_I = \text{OPEN}$  | Figures 2, 3 |
| $t_{PZH}$ , $t_{PZL}$ | Output Enable Time                    | 1.5  | 5.5  | ns    | $V_I = 7\text{V}$ for $t_{PZL}$<br>$V_I = \text{OPEN}$ for $t_{PZH}$ | Figures 2, 3 |
| $t_{PHZ}$ , $t_{PLZ}$ | Output Disable Time                   | 1.5  | 6.5  | ns    | $V_I = 7\text{V}$ for $t_{PLZ}$<br>$V_I = \text{OPEN}$ for $t_{PHZ}$ | Figures 2, 3 |

**Note 8:** This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On Resistance of the switch and the 50pF load capacitance, when driven by an ideal voltage source (zero output impedance).

### Capacitance (Note 9)

| Symbol         | Parameter                            | Typ | Max | Units | Conditions                          |
|----------------|--------------------------------------|-----|-----|-------|-------------------------------------|
| $C_{IN}$       | Control pin Input Capacitance        | 3.5 |     | pF    | $V_{CC} = 5.0\text{V}$              |
| $C_{I/O\ OFF}$ | Input/Output Capacitance "OFF State" | 5.5 |     | pF    | $V_{CC} = 5.0\text{V}$ , Switch OFF |

**Note 9:**  $T_A = +25\text{ }^\circ\text{C}$ ,  $f = 1\text{ MHz}$ , Capacitance is characterized but not tested.

### Undershoot Characteristic (Note 10)

| Symbol     | Parameter                        | Min | Typ            | Max | Units | Conditions |
|------------|----------------------------------|-----|----------------|-----|-------|------------|
| $V_{OUTU}$ | Output Voltage During Undershoot | 2.5 | $V_{OH} - 0.3$ |     | V     | Figure 1   |

**Note 10:** This test is intended to characterize the device's protective capabilities by maintaining output signal integrity during an input transient voltage undershoot event.

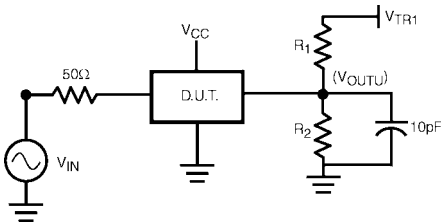
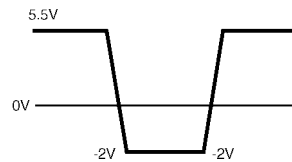


FIGURE 1.

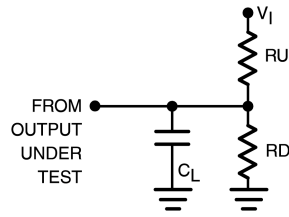
### Device Test Conditions

| Parameter   | Value        | Units    |
|-------------|--------------|----------|
| $V_{IN}$    | see Waveform | V        |
| $R_1 = R_2$ | 100K         | $\Omega$ |
| $V_{TRI}$   | 11.0         | V        |
| $V_{CC}$    | 5.5          | V        |

### Transient Input Voltage ( $V_{IN}$ ) Waveform



## AC Loading and Waveforms

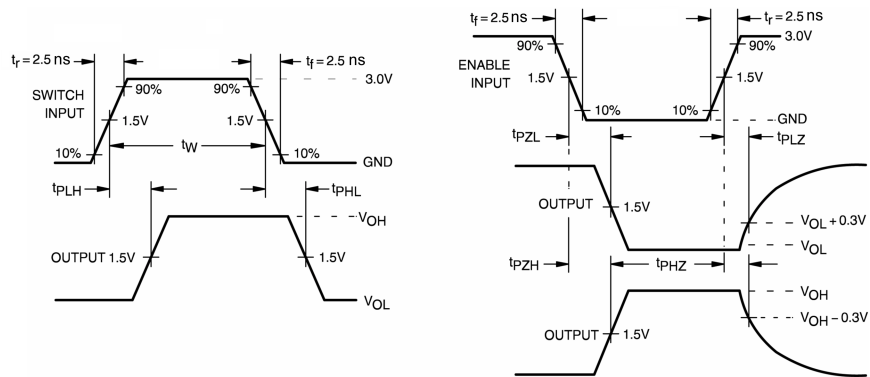


**Note:** Input driven by  $50\Omega$  source terminated in  $50\Omega$

**Note:**  $C_L$  includes load and stray capacitance

**Note:** Input PRR = 1.0 MHz,  $t_W = 500$  ns

**FIGURE 2. AC Test Circuit**



**FIGURE 3. AC Waveforms**

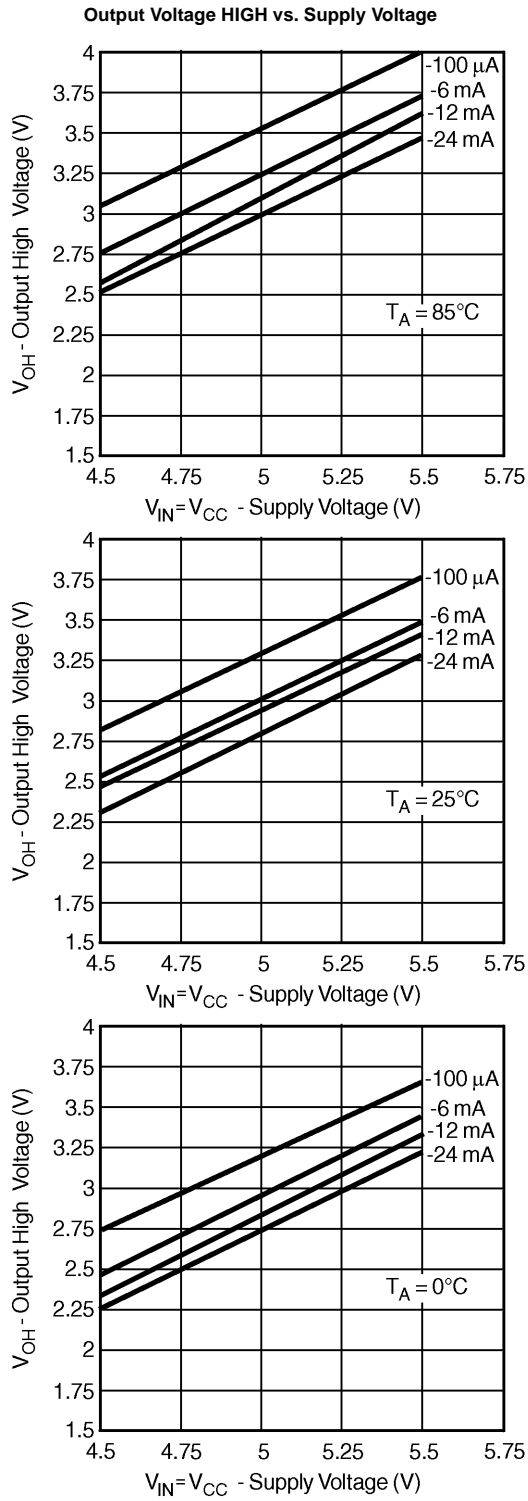
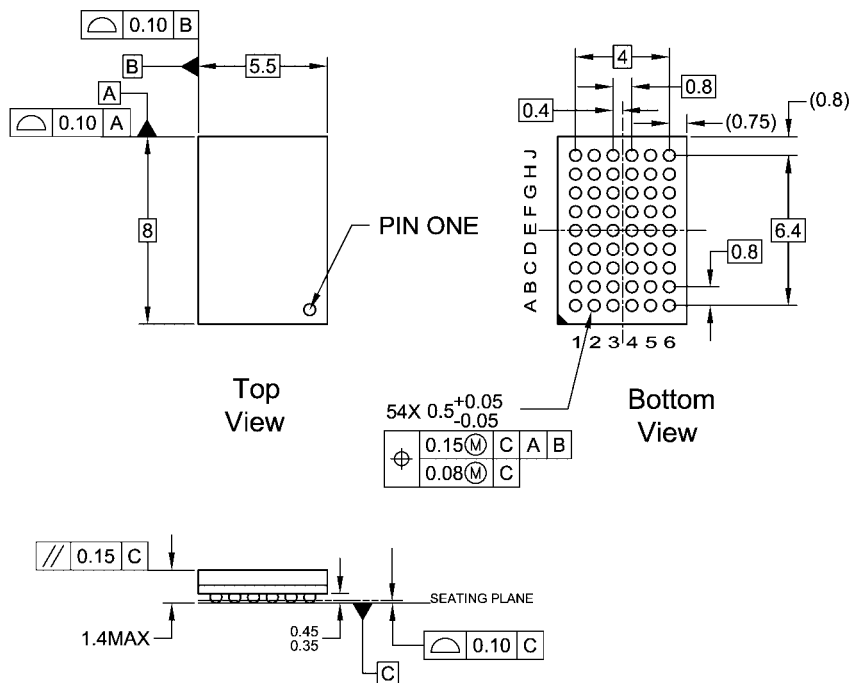


FIGURE 4.

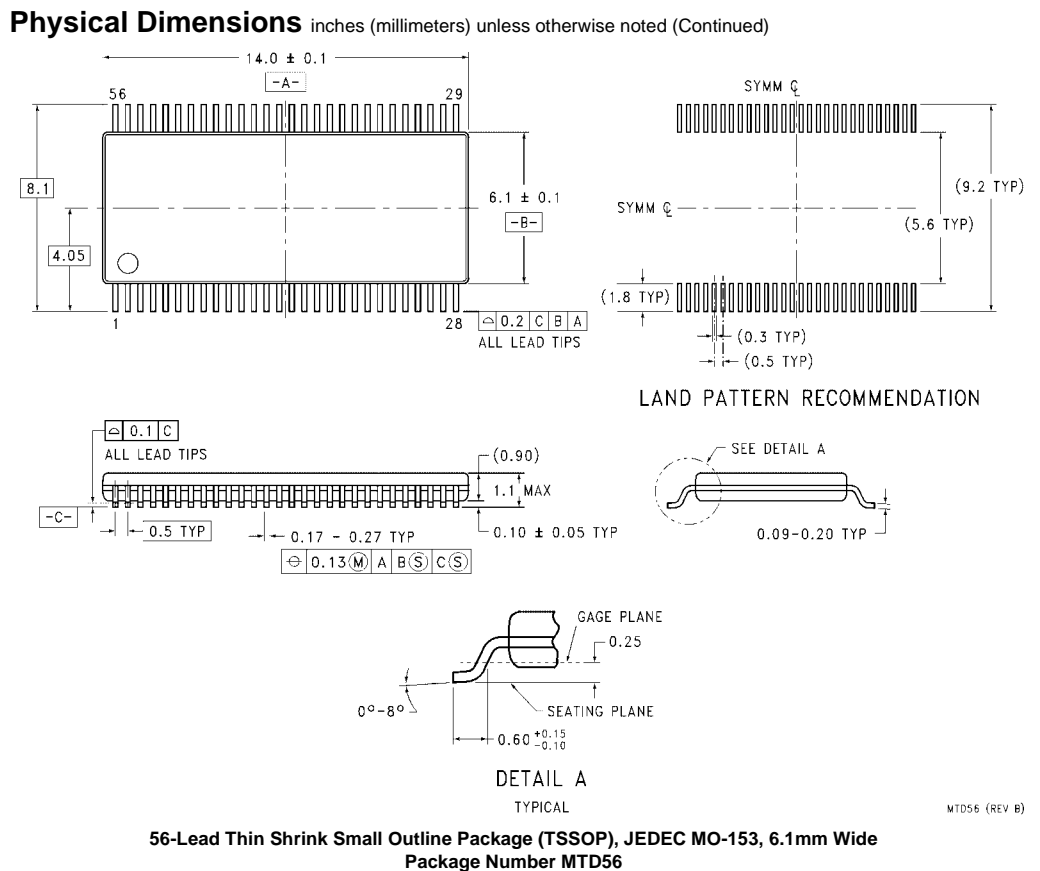
**Physical Dimensions** inches (millimeters) unless otherwise noted



- NOTES:
- A. THIS PACKAGE CONFORMS TO JEDEC M0-205
  - B. ALL DIMENSIONS IN MILLIMETERS
  - C. LAND PATTERN RECOMMENDATION: NSMD (Non Solder Mask Defined)  
.35MM DIA PADS WITH A SOLDERMASK OPENING OF .45MM CONCENTRIC TO PADS
  - D. DRAWING CONFORMS TO ASME Y14.5M-1994

BGA54ArevD

**54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC M0-205, 5.5mm Wide  
Package Number BGA54A  
Preliminary**



## Technology Description

The Fairchild Switch family derives from and embodies Fairchild's proven switch technology used for several years in its 74LVX3L384 (FST3384) bus switch product.

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

### LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

[www.fairchildsemi.com](http://www.fairchildsemi.com)