

ST2221C

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16-Bit Constant Current LED Drivers



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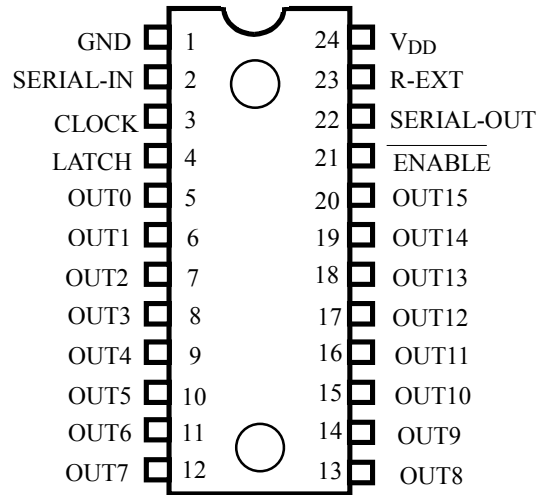
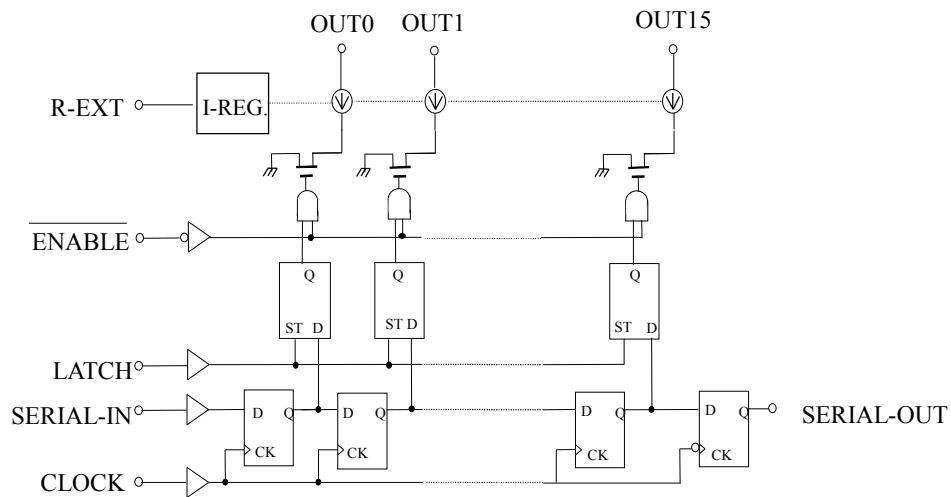
16-Bit Constant Current LED Drivers

General Description

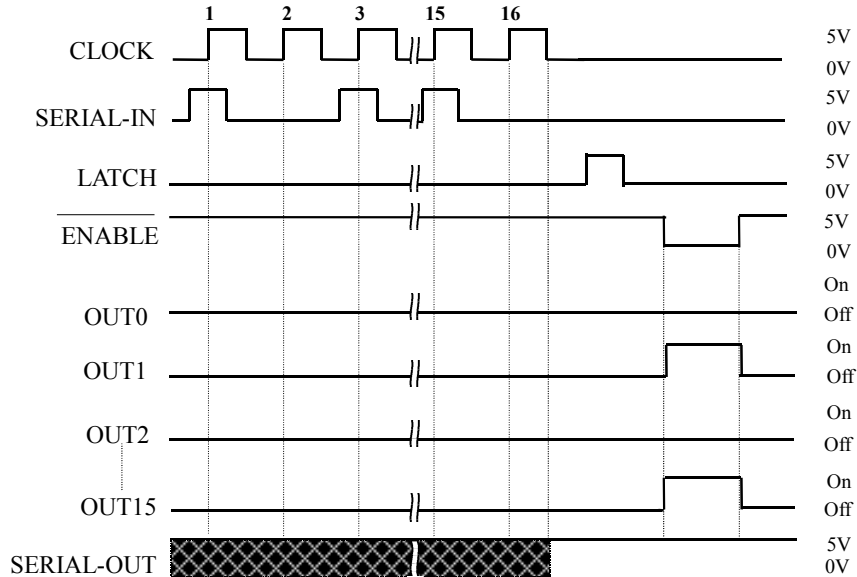
The ST2221C is specifically designed for LED and LED DISPLAY constant current drivers. The value of constant current can be varied using an external resistor ($I_{out} = 5 \sim 120\text{mA}$). The devices include a 16-bit shift registers, latches, and constant current drivers on a single Silicon CMOS chip.

Features

- Constant Current Output : Current with one resistor for 5mA to 120mA
- Maximum Clock Frequency : 25MHz (Cascade Operation)
- 5V CMOS Compatible Input
- Package : DIP24 , SOP24, SSOP24
- Constant Current Matching: ($T_a = 25^\circ\text{C}$, $V_{DD} = 5.0\text{V}$)
 - Bit-to-Bit: $\pm 6.0\%$, Chip-to-Chip : $\pm 10.0\%$,
@ $I_{OUT} = 5 \sim 40\text{mA}$
 - Bit-to-Bit: $\pm 6.0\%$, Chip-to-Chip : $\pm 10.0\%$,
@ $I_{OUT} = 40 \sim 120\text{mA}$

Pin Connection (Top view)

Block Diagram


Timing Diagram



(Note) Latches are level sensitive (not edge triggered).

LATCH-terminal = H level, latches become transparent; LATCH-terminal = L level, latches hold data.

ENABLE-terminal = H level, all outputs (OUT0~15) are off.

An external resistor is connected between R-EXT and GND for setting up the value of constant current.

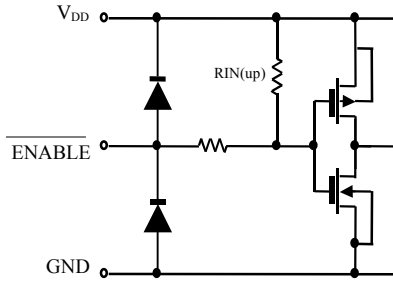
SERIAL-OUT changes state on the falling edges of clock.

Pin Description

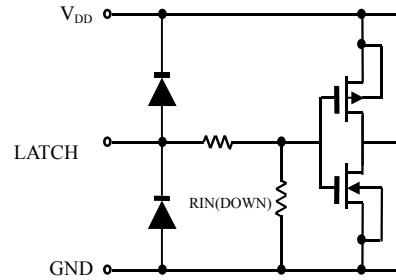
PIN No.	PIN NAME	FUNCTION
1	GND	Ground terminal
2	SERIAL-IN	Input terminal of a data shift register
3	CLOCK	Input terminal of a clock for shift register
4	LATCH	Input terminal of data strobe
5~20	OUT0~15	Output terminals
21	ENABLE	Input terminal of output enable (active low)
22	SERIAL-OUT	Output terminal of a data shift register
23	R-EXT	Input terminal of an external resistor
24	V _{DD}	5V Supply voltage terminal

Equivalent Circuit of Inputs and Outputs

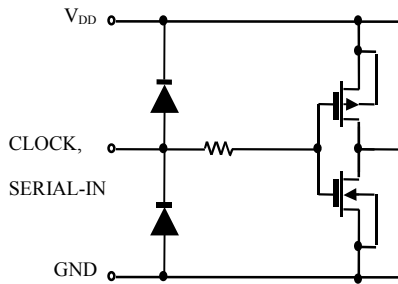
1. ENABLE terminal



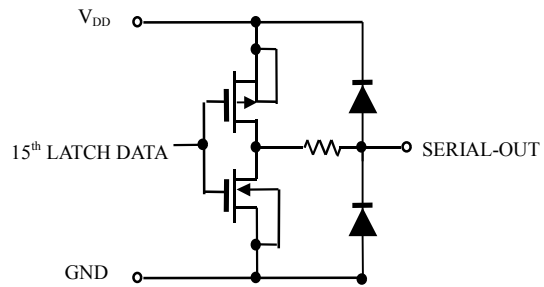
2. LATCH terminal



3. CLOCK, SERIAL-IN terminal



4. SERIAL-OUT terminal



Maximum Ratings ($T_a = 25^\circ\text{C}$, $T_{j(\text{max})} = 140^\circ\text{C}$)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	VDD	0 ~ 7.0	V
Input Voltage	VIN	-0.4 ~ VDD+0.4	V
Output Current	IOUT	120	mA
Output Voltage	VOUT	-0.5 ~ 9.5	V
Clock Frequency	fCLK	25	MHz
GND Terminal Current	IGND	1920	mA
Power Dissipation	PD	2.87 (DIP-24 : $T_a=25^\circ\text{C}$)	W
		1.45 (SOP-24 : $T_a=25^\circ\text{C}$)	
		1.27 (SSOP-24 : $T_a=25^\circ\text{C}$)	
Thermal Resistance	Rth(j-a)	40.0 (DIP-24)	$^\circ\text{C}/\text{W}$
		79.2 (SOP-24)	
		90.2 (SSOP-24)	
Storage Temperature	Tstg	-55 ~ 150	$^\circ\text{C}$

Recommended Operating Condition

CHARACTERISTIC	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	VDD	—	4.5	5.0	5.5	V
Output Voltage	VOUT	—	—	—	9	V
Output Current	Io	OUTn	5	—	115	mA
	IOH	SERIAL-OUT	—	—	1.0	
	IOL	SERIAL-OUT	—	—	-1.0	
Input Voltage	VIH	—	0.7VDD	—	VDD+0.3	V
	VIL	—	-0.3	—	0.3VDD	
LATCH Pulse Width	tw LAT	VDD = 4.5 ~ 5.5 V	15	—	—	ns
CLOCK Pulse Width	tw CLK		15	—	—	ns
Set-up Time for DATA	tsetup(D)		20	—	—	ns
Hold Time for DATA	thold(D)		20	—	—	ns
Set-up Time for LATCH	tsetup(L)		15	—	—	ns
Clock Frequency	fCLK	Cascade operation	—	—	25	MHz
Power Dissipation	PD	$T_a = 85^\circ\text{C}$ (DIP-24)	—	—	1.37	W
		$T_a = 85^\circ\text{C}$ (SOP-24)	—	—	0.69	
		$T_a = 85^\circ\text{C}$ (SSOP-24)	—	—	0.61	

Electrical Characteristics (VDD = 5.0 V, Ta = 25°C unless otherwise noted)

CHARACTERISTIC	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Input Voltage "H" Level	VIH	—	0.7VDD	—	VDD	V
Input Voltage "L" Level	VIL	—	GND	—	0.3VDD	
Output Leakage Current	IOH	VOH = 9.5 V	—	—	1.0	µA
Output Voltage (S - OUT)	VOL	IOL = 1.0 mA	—	—	0.4	V
	VOH	IOH = -1.0 mA	4.6	—	—	
Output Current (Bit-Bit)	IOL1	VOUT = 0.7±0.25V REXT = 910Ω	—	3	6	%
	IOL2	VOUT = 0.7±0.25V REXT = 360Ω	—	3	6	
Output Current (Chip-Chip)	IOL3	VOUT = 0.7V REXT = 910Ω	—	5	10	
	IOL4	VOUT = 0.7V REXT = 360Ω	—	5	10	
Supply Voltage Regulation	% / VDD	REXT = 470Ω, Ta = -40 ~ 85°C	—	1.5	5.0	% / V
Pull-Up Resistor	RIN(up)	—	150	300	600	KΩ
Pull-Down Resistor	RIN(down)	—	100	200	400	KΩ
Supply Current "OFF"	IDD(off)1	REXT = OPEN, OUT0~7 = off	—	0.3	0.6	mA
	IDD(off)2	REXT = 470Ω, OUT0~7 = off	3.9	5.5	7.7	
	IDD(off)3	REXT = 250Ω, OUT0~7 = off	7.2	10.1	14.1	
Supply Current "ON"	IDD(on)1	REXT = 470Ω, OUT0~7 = on	3.9	5.5	7.7	mA
	IDD(on)2	REXT = 250Ω, OUT0~7 = on	7.2	10.1	14.1	

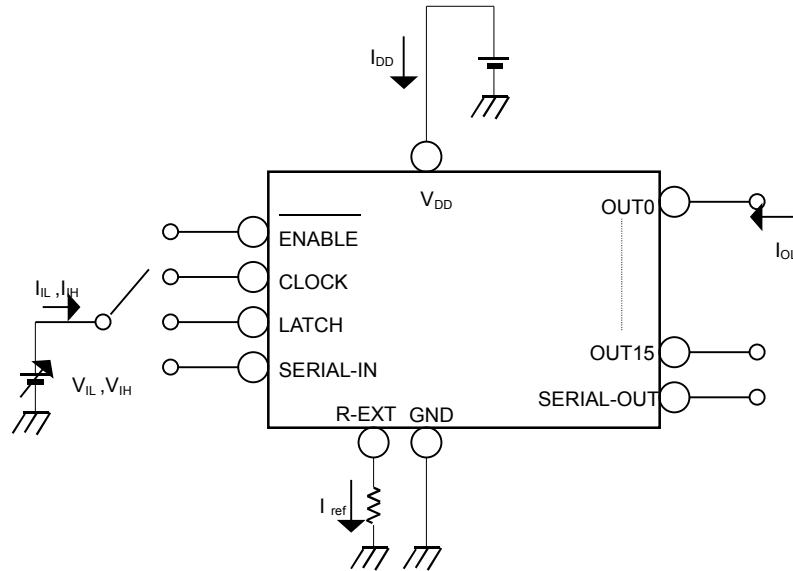
Switching Characteristics (Ta = 25 °C unless otherwise noted)

CHARACTERISTIC	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Propagation Delay Time ("L" to "H")	SIN-OUTn	VDD=5.0V VIH=VDD VIL=GND REXT=470Ω ¹ VL=3.0V RL=65Ω CL=13pF	—	150	300	ns
	LATCH-OUTn		—	150	300	
	ENABLE-OUTn		—	150	300	
	CLK-SOUT		—	15	20	
Propagation Delay Time ("H" to "L")	SIN-OUTn	VDD=5.0V VIH=VDD VIL=GND REXT=470Ω ¹ VL=3.0V RL=65Ω CL=13pF	—	30	60	ns
	LATCH-OUTn		—	30	60	
	ENABLE-OUTn		—	30	60	
	CLK-SOUT		—	15	20	
Output Current Rise Time	tor		—	170	340	ns
Output Current Fall Time	tof		—	20	40	ns

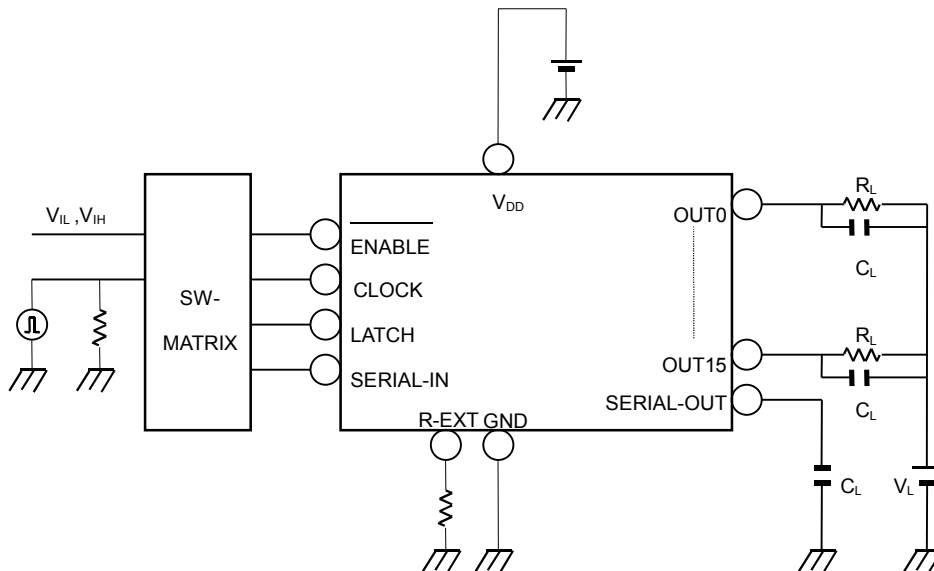
¹ Delay time t_{PLH} and Rise Time tor will both increase as the Rext value increased.

Test Circuit

DC characteristic

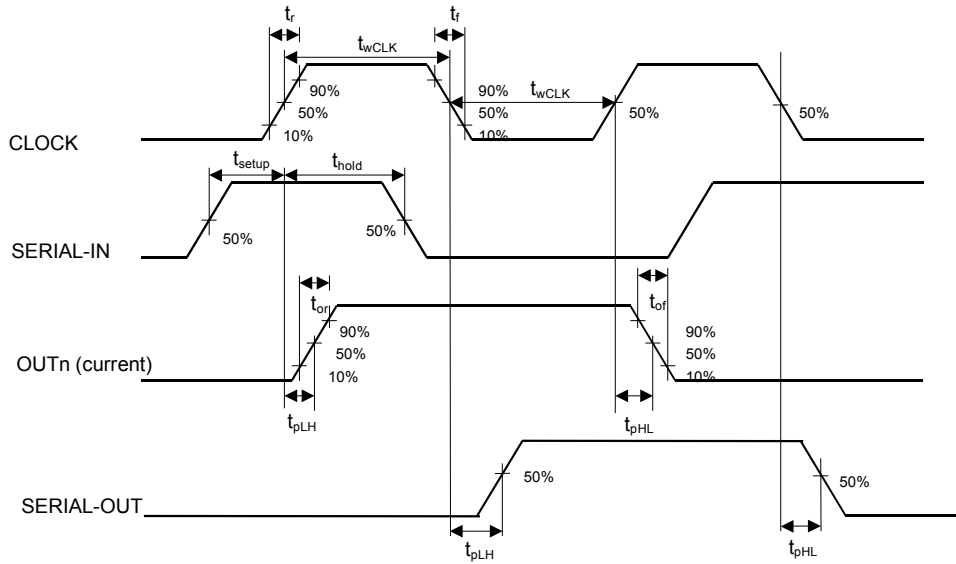


AC characteristic

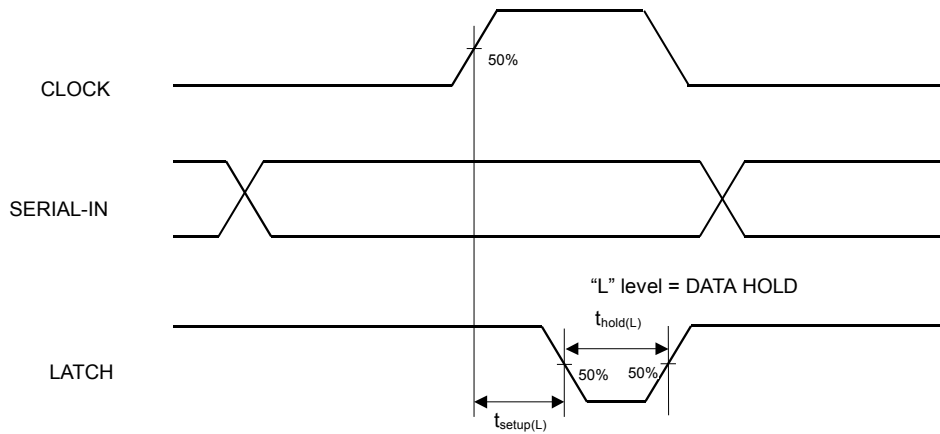


Timing Diagram

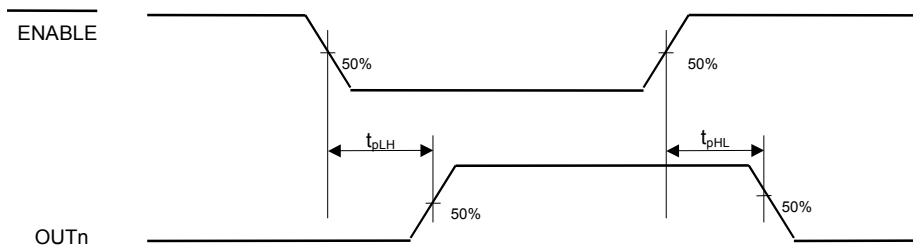
1. CLOCK-SERIAL-IN, SERIAL-OUT, OUT_n

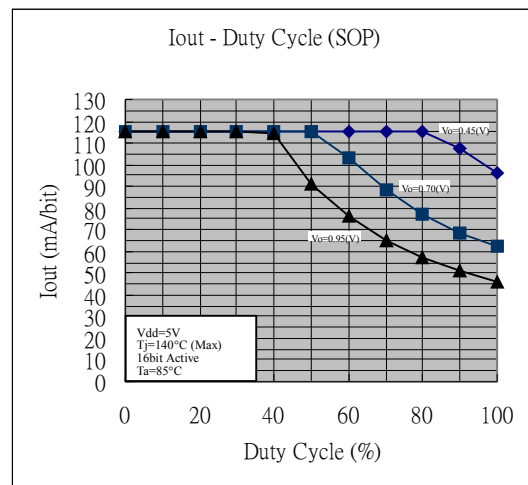
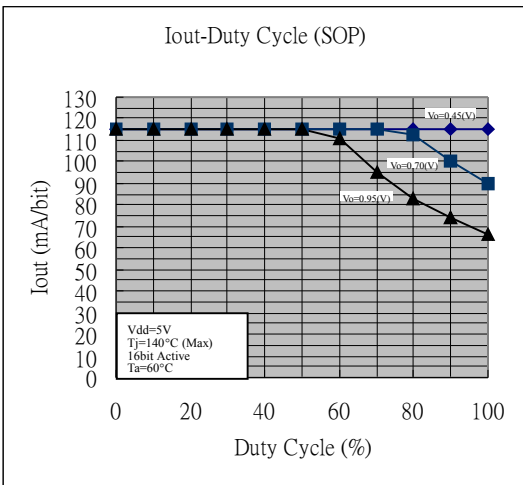
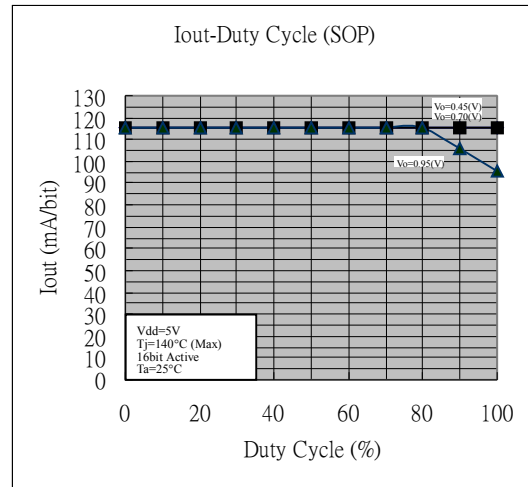
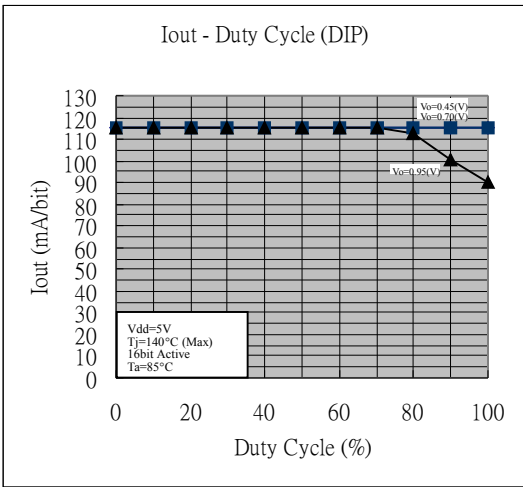
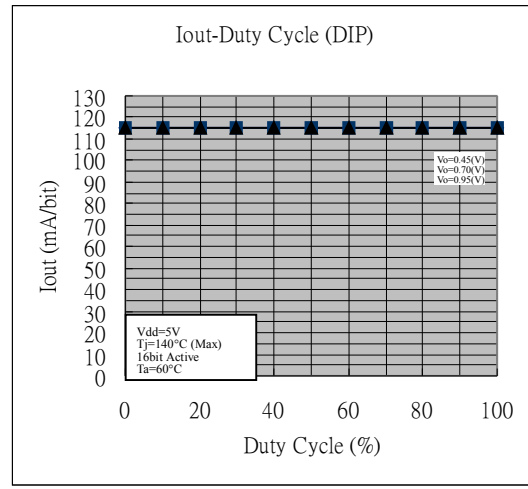
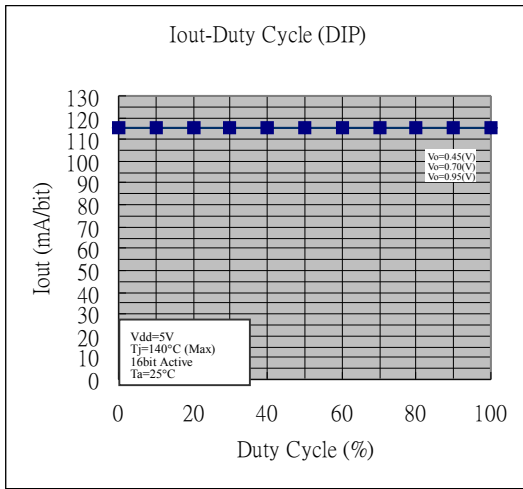


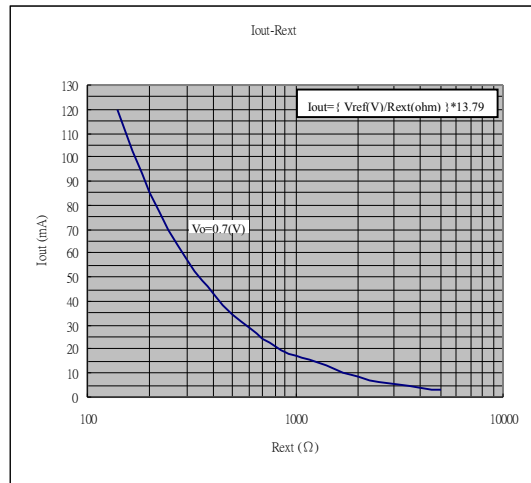
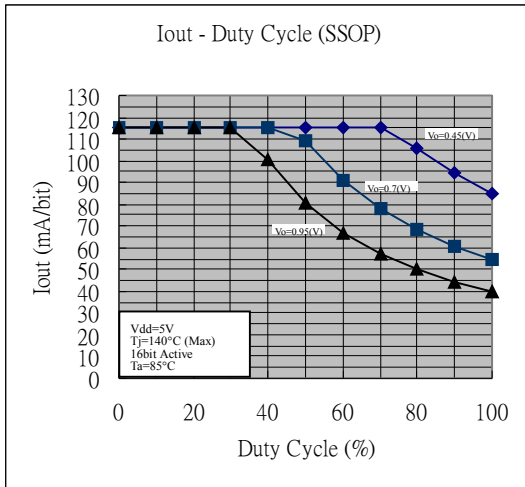
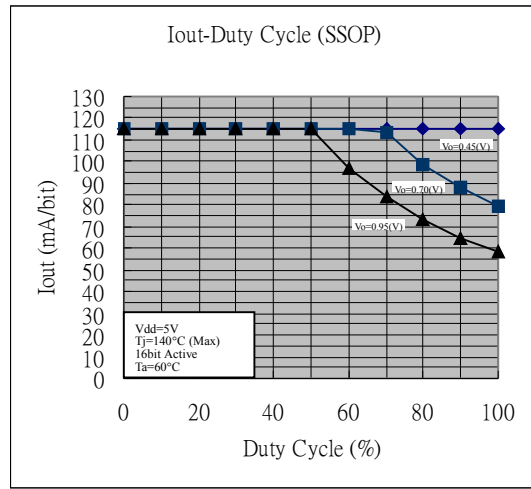
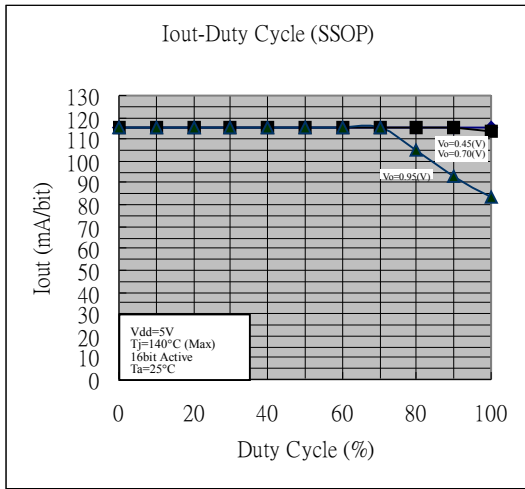
2. CLOCK-LATCH

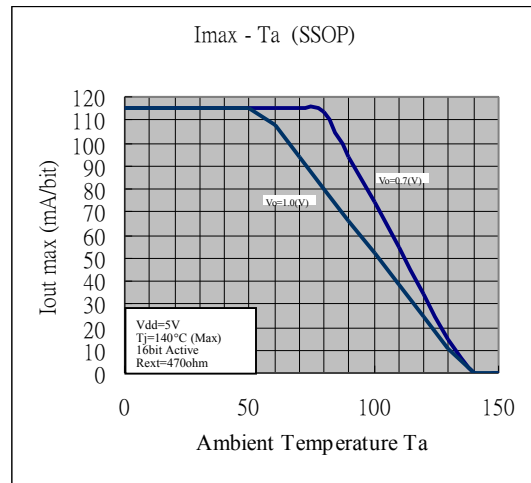
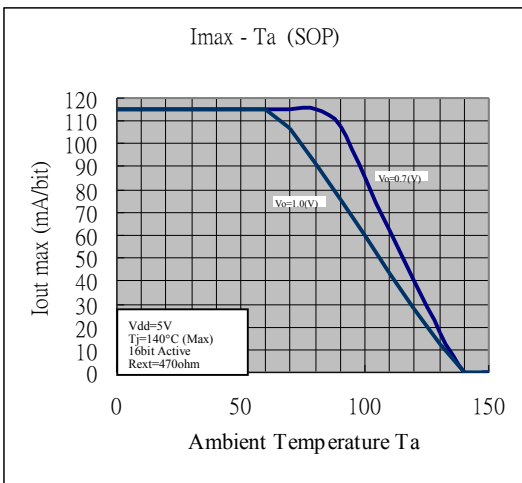
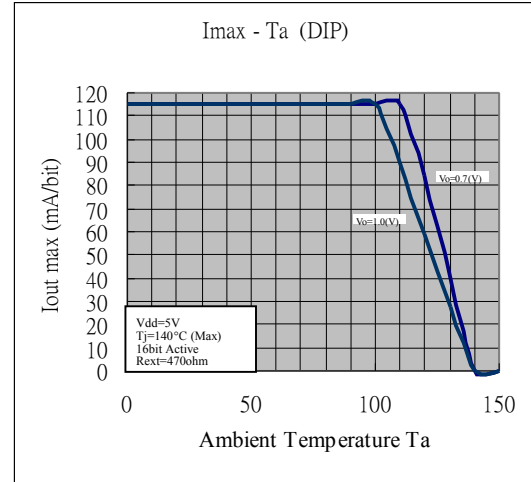
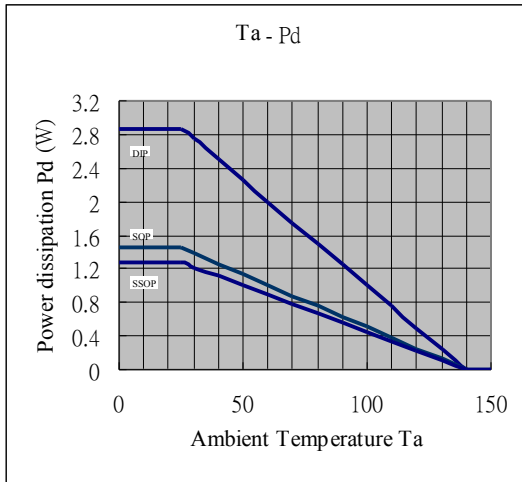


3. ENABLE-OUT_n









Note

As the power dissipation of a semiconductor chip is limited its package and ambient temperature, this device requires a maximum output current be calculated for a given operating condition. The maximum allowable power consumption (Pd (max)) of this device is calculated as follows:

$$Pd(max)(Watt) = \frac{(T_j \text{ (junction temperature) (max)} - T_a \text{ (ambient temperature)}) (^\circ C)}{R_{th} (^\circ C / Watt)}$$

Based on the Pd (max), the maximum allowable current can be calculated as follows:

$$I_{out} = (Pd - V_{DD} \cdot I_{DD}) / (\# \text{ outputs} \cdot V_o \cdot \text{Duty})$$

System Configuration Example

[1] Output current (I_{OUT})

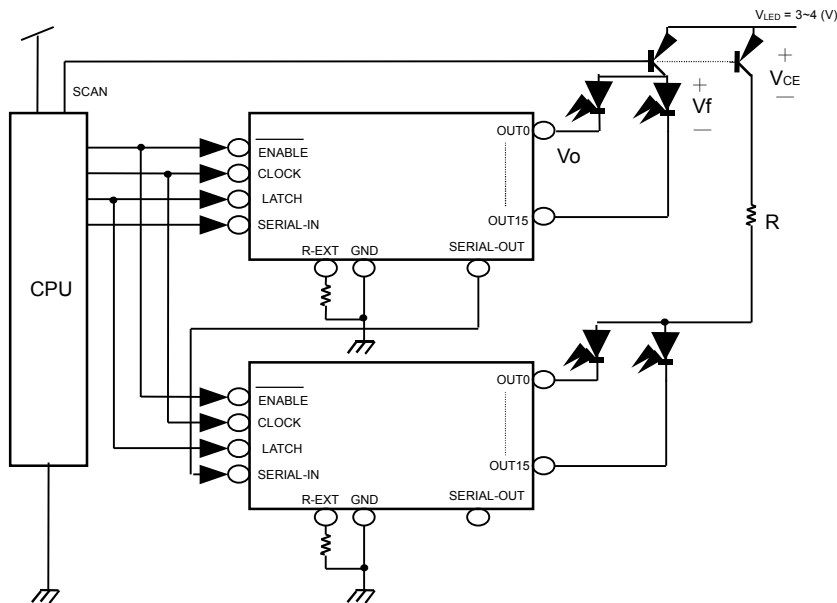
Sink current is set by the external resistor as shown in the figure (I_{out} vs. R_{ext}).

[2] LED supply voltage (V_{LED}) setup

$$V_{LED} = V_{CE} (T_r V_{sat}) + V_f (\text{LED forward voltage}) + V_O (\text{IC supply voltage})$$

To prevent too much power dissipated by the device due to higher V_{LED} , an additional R can be used to reduce the V_{out} when the outputs consume current:

$$R = \frac{V_{LED} - V_{CE} - V_f - V_O(\text{min})}{I_O(\text{max}) * Bit(\text{max})}$$



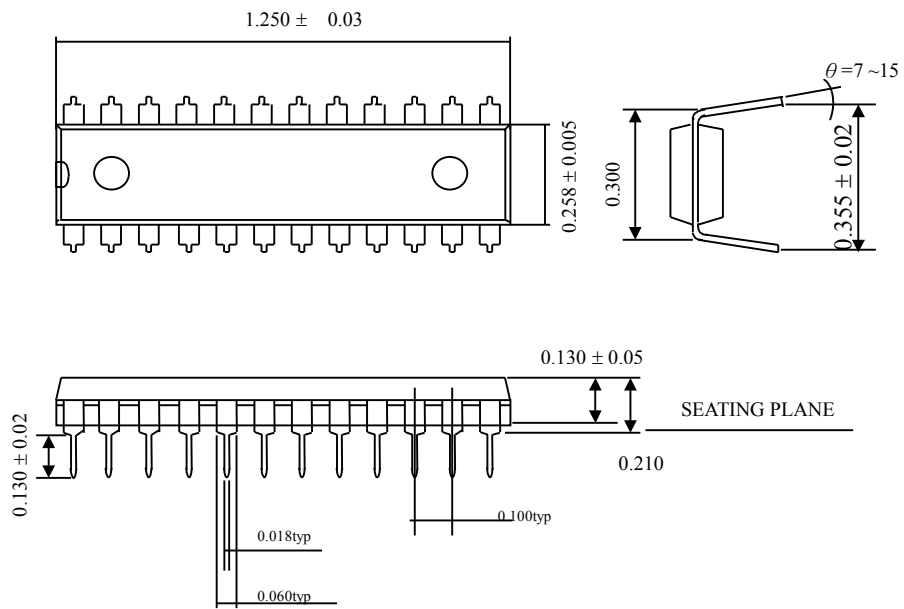
Note

This device has only one ground pin shared by signal, output sink current, and power ground. It is advisable to pattern the ground layout with minimized inductance such that the switching noise induced by the input signals and the output sink current would not cause chip malfunction. To prevent the drivers' outputs from damage by overshoot stress, it is also advisable not to turn off the drivers and scan transistors simultaneously.

Package Outline

P-DIP 24

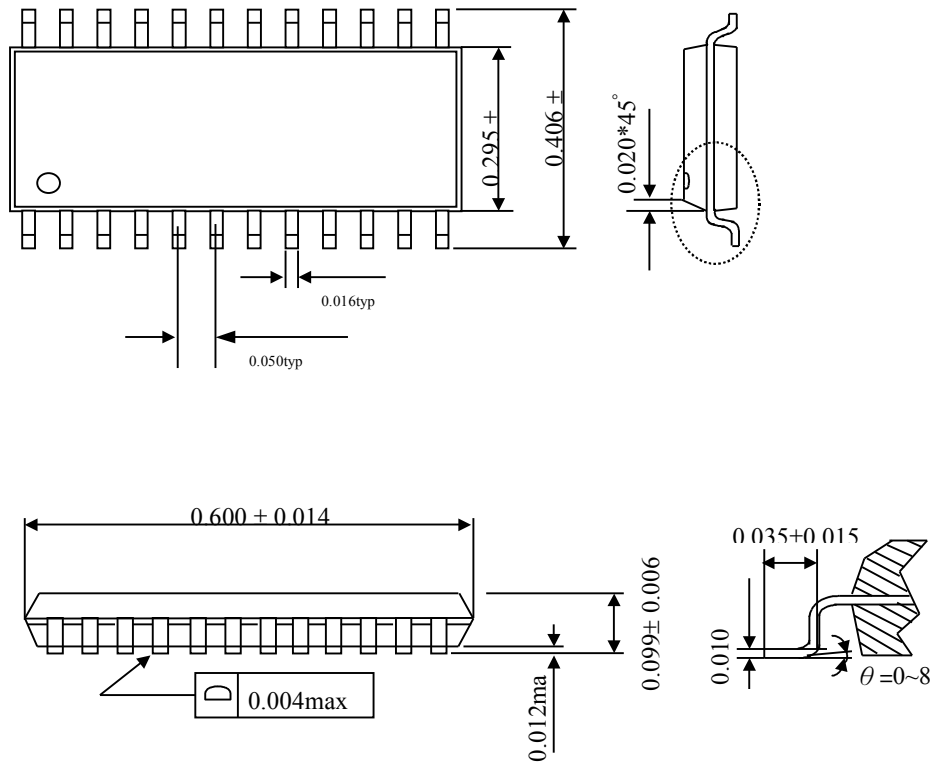
UNIT : INCH



Package Outline

SOP24

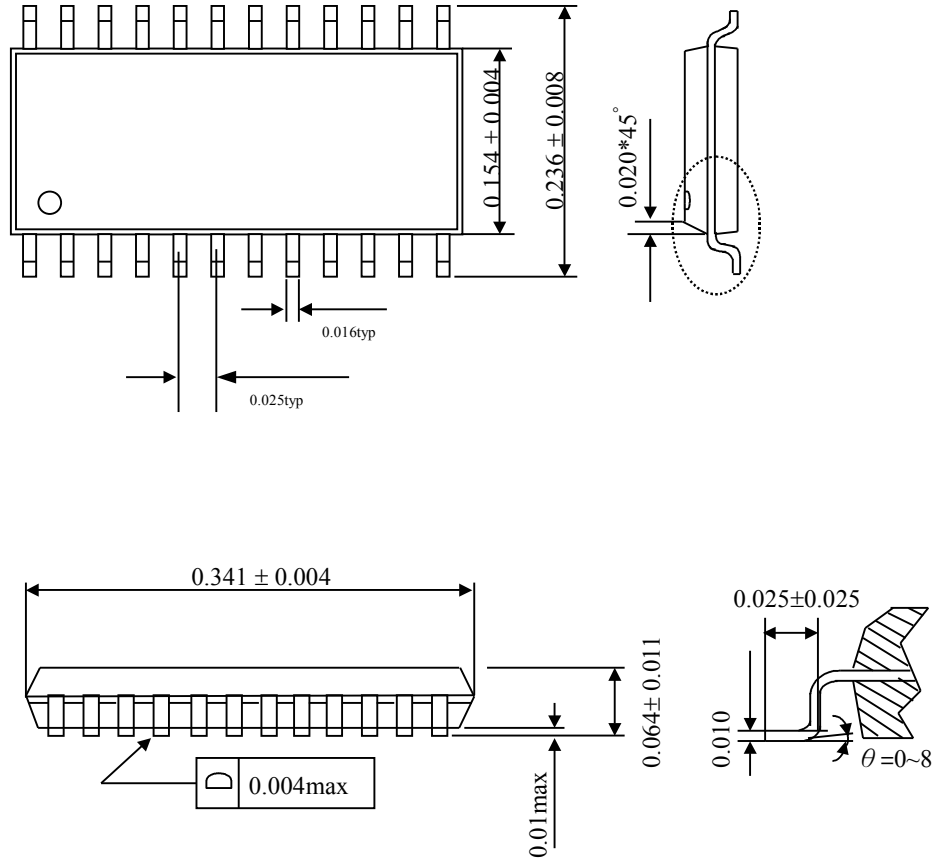
UNIT : INCH



Package Outline

SSOP24

UNIT : INCH



The products listed herein are designed for ordinary electronic applications, such as electrical appliances, audio-visual equipment, communications devices and so on. Hence, it is advisable that the devices should not be used in medical instruments, surgical implants, aerospace machinery, nuclear power control systems, disaster/crime-prevention equipment and the like. Misusing those products may directly or indirectly endanger human life, or cause injury and property loss.

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