DMN3210

N-CHANNEL ENHANCEMENT MODE FIELD EFFECT TRANSISTOR

NEW PRODUCT

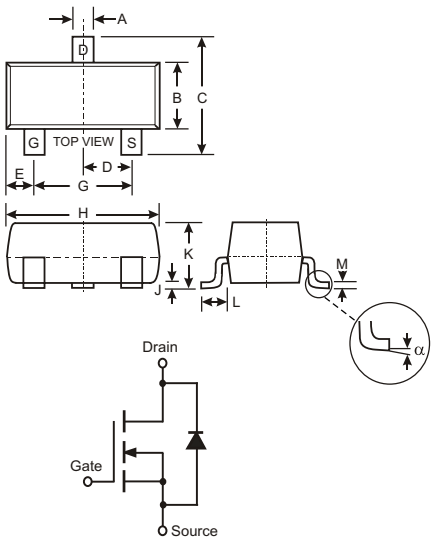
UNDER DEVELOPMENT

Features

- Low Gate Threshold Voltage
- Ultra Low On-Resistance
- Low Input/Output Capacitance
- Low Input/Output Leakage
- Fast Switching Speed

Mechanical Data

- Case: SOT-23, Molded Plastic
- Case material - UL Flammability Rating 94V-0
- Moisture sensitivity: Level 1 per J-STD-020A
- Terminals: Solderable per MIL-STD-202, Method 208
- Terminal Connections: See Diagram
- Marking: U0, See Page 5
- Weight: 0.008 grams (approx.)
- Ordering Information, See page 5



SOT-23		
Dim	**Min**	**Max**
A	0.37	0.51
B	1.20	1.40
C	2.30	2.50
D	0.89	1.03
E	0.45	0.60
G	1.78	2.05
H	2.80	3.00
J	0.013	0.10
K	0.903	1.10
L	0.45	0.61
M	0.085	0.180
α	0°	8°
All Dimensions in mm		

Maximum Ratings @ T_A = 25°C unless otherwise specified

Characteristic	Symbol	DMN3210	Units
Drain-Source Voltage	V_{DSS}	30	V
Gate-Source Voltage	V_{GSS}	±12	V
Drain Current (Note 1) Continuous	I_D	1.7	A
Pulsed Drain Current (Note 3)	I_{DM}	15	A
Total Power Dissipation (Note 1)	P_d	540	mW
Thermal Resistance, Junction to Ambient (Note 1) t ≤10s	$R_{\theta JA}$	230	°C/W
Operating and Storage Temperature Range	T_j, T_{STG}	-55 to +150	°C

Note: 1. Per mounting conditions described in Note 2.
2. The value of $R_{\theta JA}$ is measured with the device mounted on 1 in² FR-4 PC board with 2 oz. Copper, in a still air environment at T_A = 25°C. The current rating is based on the t ≤10s Thermal Resistance rating.
3. Repetitive Rating, pulse width limited by junction temperature.

Electrical Characteristics @ $T_A = 25°C$ unless otherwise specified

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
STATIC PARAMETERS						
Drain-Source Breakdown Voltage	BV_{DSS}	30	—	—	V	$I_D = 250\mu A$, $V_{GS} = 0V$
Zero Gate Voltage Drain Current $T_J = 25°C$ $T_J = 55°C$	I_{DSS}	—	—	1 5	μA	$V_{DS} = 24V$, $V_{GS} = 0V$
Gate-Body Leakage Current	I_{GSS}	—	—	100	nA	$V_{DS} = 0V$, $V_{GS} = +12V$
Gate Threshold Voltage	$V_{GS(th)}$	0.6	1	1.4	V	$V_{DS} = V_{GS}$, $I_D = 250\mu A$
On State Drain Current	$I_{D(ON)}$	10	—	—	A	$V_{GS} = 4.5V$, $V_{DS} = 5V$
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	70 80 115	85 100 140	mΩ	$V_{GS} = 10V$, $I_D = 4A$ $V_{GS} = 4.5V$, $I_D = 3A$ $V_{GS} = 2.5V$, $I_D = 2A$
Forward Transconductance	g_{FS}	—	8	—	S	$V_{DS} = 5V$, $I_D = 4A$
Diode Forward Voltage	V_{SD}	—	0.8	1	V	$I_S = 1A$, $V_{GS} = 0V$
Maximum Body-Diode Continuous Current	I_S	—	—	2.5	A	
DYNAMIC PARAMETERS						
Input Capacitance	C_{iss}	—	390	—	pF	$V_{GS} = 0V$, $V_{DS} = 15V$, f = 1MHz
Output Capacitance	C_{oss}	—	54.5	—	pF	
Reverse Transfer Capacitance	C_{rss}	—	41	—	pF	
Gate Resistance	R_g	—	3	—	Ω	$V_{GS} = 0V$, $V_{DS} = 0V$, f = 1MHz
SWITCHING PARAMETERS						
Total Gate Charge	Q_g	—	0.6	—	nC	$V_{GS} = 4.5V$, $V_{DS} = 15V$, $I_D = 4A$
Gate Source Charge	Q_{gs}	—	1.38	—	nC	
Gate Drain Charge	Q_{gd}	—	4.34	—	nC	
Turn-On Delay Time	$t_{D(on)}$	—	3.3	—	ns	$V_{GS} = 10V$, $V_{DS} = 15V$, $R_L = 3.75\Omega$, $R_{GEN} = 6\Omega$
Turn-On Rise Time	t_r	—	1	—	ns	
Turn-Off Delay Time	$t_{D(off)}$	—	21.7	—	ns	
Turn-Off Fall Time	t_f	—	2.1	—	ns	
Body Diode Reverse Recovery Time	t_{rr}	—	12	—	ns	$I_F = 4A$, di/dt = 100A/μs
Body Diode Reverse Recovery Charge	Q_{rr}	—	6.3	—	nC	$I_F = 4A$, di/dt = 100A/μs

Note: 4. The static characteristics in Figures 1-6, 12, 14 are obtained using 80μs pulses, duty cycle 0.5% max.
5. These tests are performed with device mounted on 1 in^2 FR-4 PC board with 2 oz. copper, in a still air environment at $T_A = 25°C$. The SOA curve provides a single pulse rating.

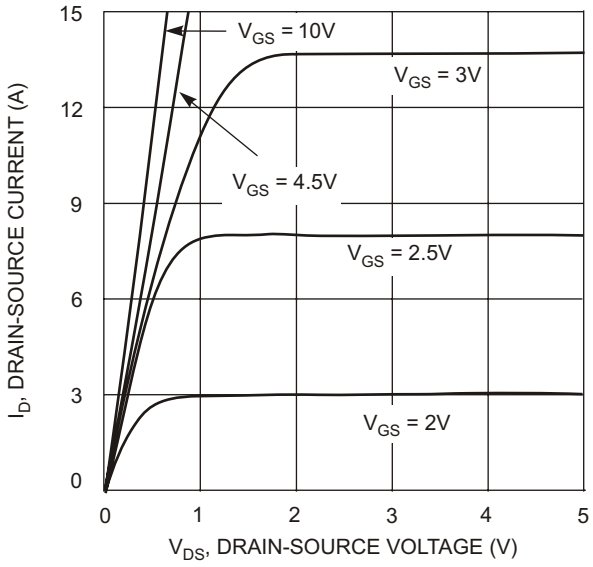


Fig. 1 On-Region Characteristics

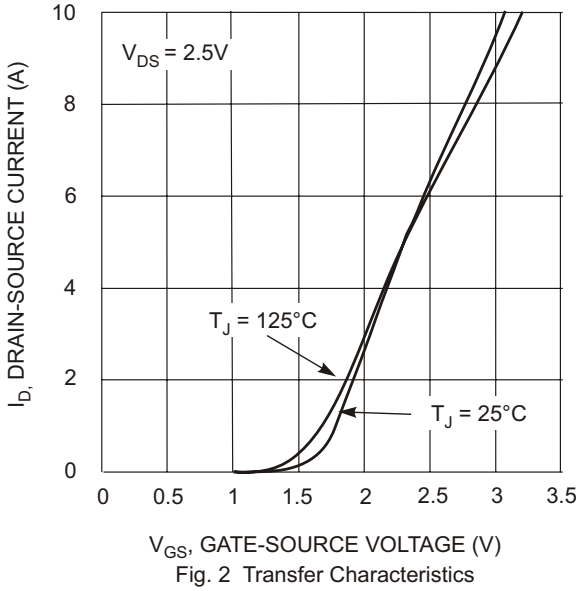


Fig. 2 Transfer Characteristics

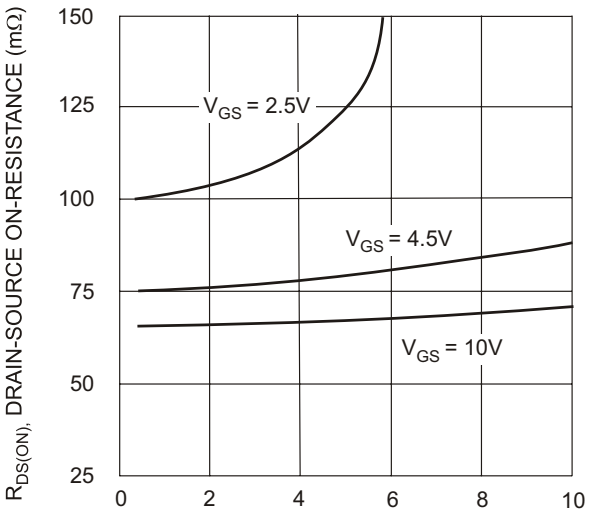


Fig. 3 On-Resistance vs. Drain Current and Gate Voltage

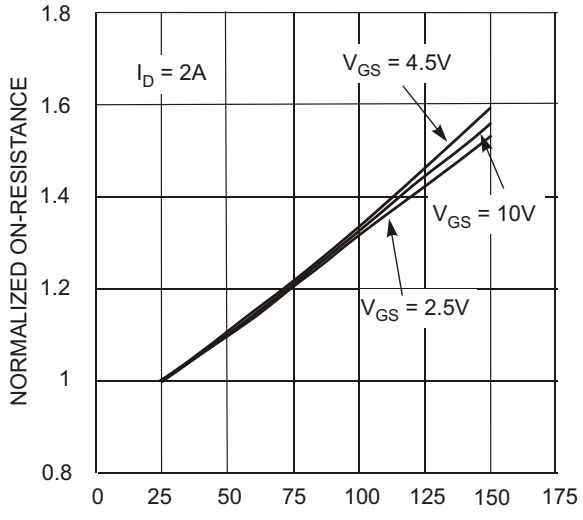


Fig. 4 On-Resistance vs. Junction Temperature

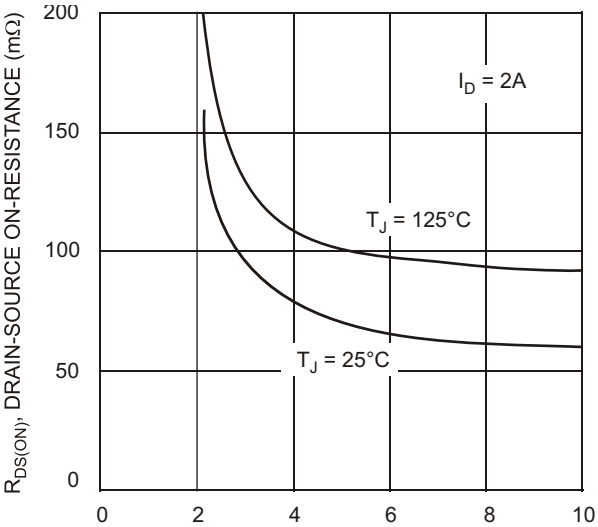


Fig. 5 On-Resistance vs. Gate-Source Voltage

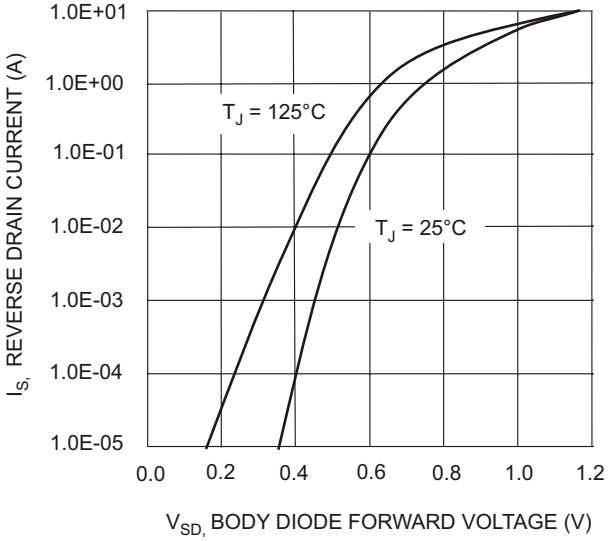


Fig. 6 Body-Diode Forward Voltage Variation with Source Current and Temperature

UNDER DEVELOPMENT

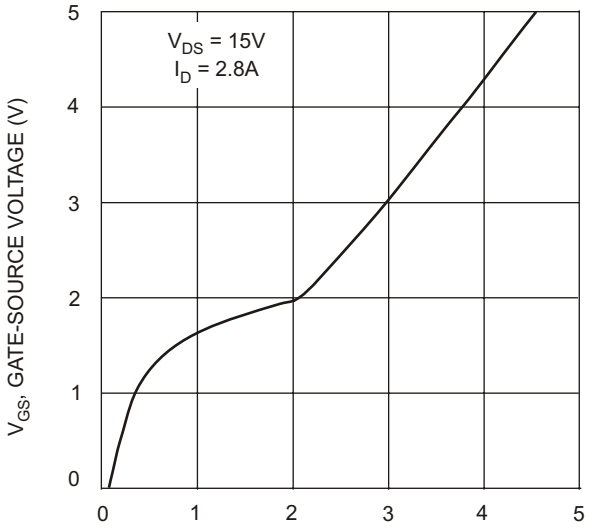


Fig. 7 Gate-Charge Characteristics

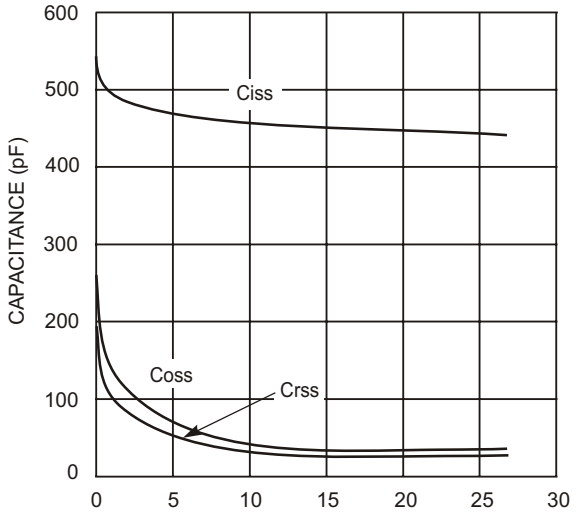


Fig. 8 Capacitance Characteristics

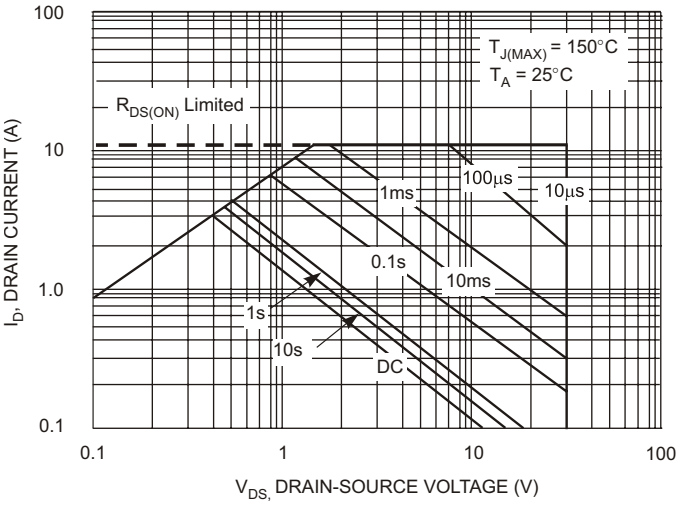


Fig. 9 Maximum Forward Biased Safe Operating Area (Note 5)

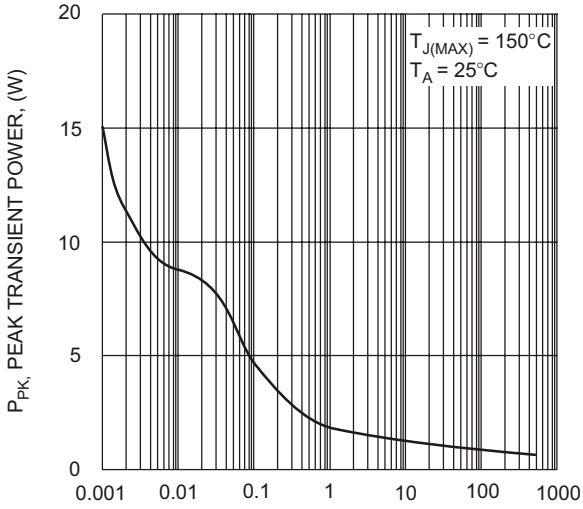


Fig. 10 Single Pulse Power Rating Junction-to Ambient (Note 5)

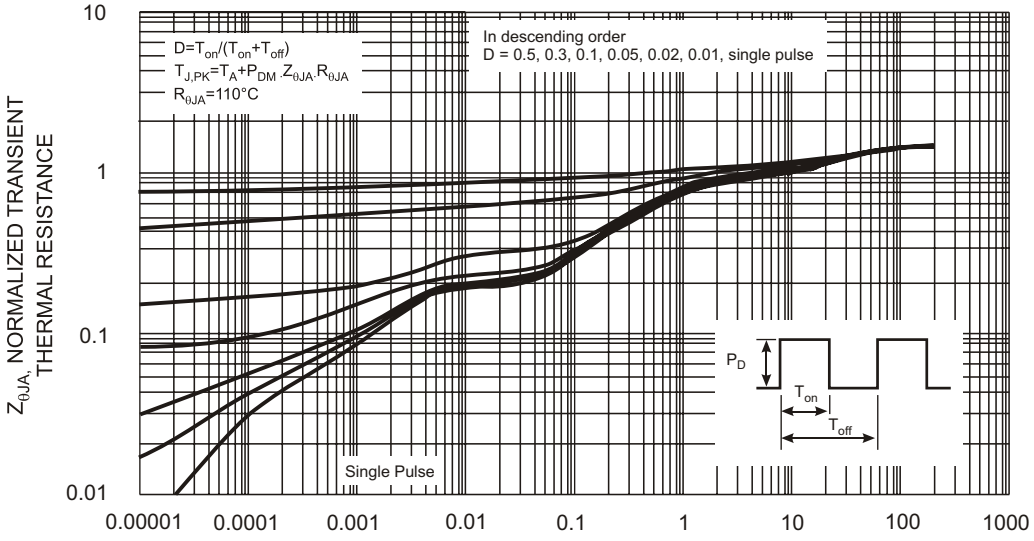


Fig. 11 Normalized Maximum Transient Thermal Impedance

UNDER DEVELOPMENT

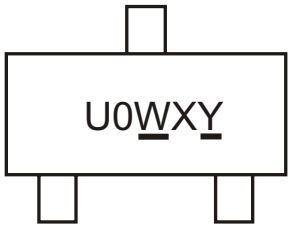
NEW PRODUCT

Ordering Information (Note 6)

Device	Packaging	Shipping
DMN3210-7	SOT-23	3000/Tape & Reel

Notes: 6. For Packaging Details, go to our website at http://www.diodes.com/datasheets/ap02007.pdf.

Marking Information



U0 = Product Type Marking Code
W = Week and Year Code Marking
XY = Lot Code Marking
Y = Assembly Location, Diodes China

Week Code Key

Week	0 - 1	2 - 3	4 - 5	6 - 7	8 - 9	10 - 11	12 - 13	14 - 15	16 - 17
Code	A	B	C	D	E	F	G	H	J

Week	18 - 19	20 - 21	22 - 23	24 - 25	26 - 27	28 - 29	30 - 31	32 - 33	34 - 35
Code	K	L	N	O	P	R	S	T	U

Week	36 - 37	38 - 39	40 - 41	42 - 43	44 - 45	46 - 47	48 - 49	50 - 51	52 - 53
Code	V	X	Y	Z	1	2	3	4	5

Year Code Key

Year	2002	2003	2004	2005
Code	W	$\overline{W}$	$\underline{\overline{W}}$	$\dot{W}$

UNDER DEVELOPMENT