# 256Kx36/512Kx18 Flow-Thru SRAM with NoBL™ Architecture

## Features

- **Zero Bus Latency, no dead cycles between write and read cycles**
- **Fast clock speed: 133, 117, and 100 MHz**
- **Fast access time: 6.5, 7.0, 7.5, and 8.0 ns**
- **Internally synchronized registered outputs eliminate the need to control $\overline{OE}$**
- **Single 3.3V –5% and +5% power supply $V_{CC}$**
- **Separate $V_{CCQ}$ for 3.3V or 2.5V I/O**
- **Single R/$\overline{W}$ (READ/WRITE) control pin**
- **Positive clock-edge triggered, address, data, and control signal registers for fully pipelined applications**
- **Interleaved or linear 4-word burst capability**
- **Individual byte write ($\overline{BWa}$–$\overline{BWd}$) control (may be tied LOW)**
- **$\overline{CKE}$ pin to enable clock and suspend operations**
- **Three chip enables for simple depth expansion**
- **SNOOZE MODE for low power standby**
- **JTAG boundary scan**
- **Low profile 119-bump, 14-mm x 22-mm BGA (Ball Grid Array) and 100-pin TQFP packages**

## Functional Description

The CY7C1355A/GVT71256ZB36 and CY7C1357A/ GVT71512ZB18 SRAMs are designed to eliminate dead cycles when transitions from READ to WRITE or vice versa. These SRAMs are optimized for 100 percent bus utilization and achieves Zero Bus Latency (ZBL)/No Bus Latency (No-BL). They integrate 262,144x36 and 524,288x18 SRAM cells, respectively, with advanced synchronous peripheral circuitry and a 2-bit counter for internal burst operation. These employ high-speed, low power CMOS designs using advanced triple-layer polysilicon, double-layer metal technology. Each memory cell consists of four transistors and two high valued resistors.

All synchronous inputs are gated by registers controlled by a positive-edge-triggered Clock Input (CLK). The synchronous inputs include all addresses, all data inputs, depth-expansion Chip Enables ($\overline{CE}$, $\overline{CE_2}$, and $CE_2$), Cycle Start Input (ADV/$\overline{LD}$), Clock Enable ($\overline{CKE}$), Byte Write Enables ($\overline{BWa}$, $\overline{BWb}$, $\overline{BWc}$, and $\overline{BWd}$), and read-write control (R/$\overline{W}$). $\overline{BWc}$ and $\overline{BWd}$ apply to CY7C1355A/GVT71256ZB36 only.

Address and control signals are applied to the SRAM during one clock cycle, and one cycle later, its associated data occurs, either read or write.

A Clock Enable ($\overline{CKE}$) pin allows operation of the CY7C1355A/CY7C1357A/GVT71256ZB36/GVT71512ZB18 to be suspended as long as necessary. All synchronous inputs are ignored when ($\overline{CKE}$) is HIGH and the internal device registers will hold their previous values.

There are three Chip Enable pins ($\overline{CE}$, $CE_2$, $\overline{CE_2}$) that allow the user to deselect the device when desired. If any one of these three are not active when ADV/$\overline{LD}$ is LOW, no new memory operation can be initiated and any burst cycle in progress is stopped. However, any pending data transfers (read or write) will be completed. The data bus will be in high-impedance state one cycle after chip is deselected or a write cycle is initiated.

The CY7C1355A/GVT71256ZB36 and CY7C1357A/ GVT71512ZB18 have an on-chip 2-bit burst counter. In the burst mode, the CY7C1355A/GVT71256ZB36 and CY7C1357A/GVT71512ZB18 provide four cycles of data for a single address presented to the SRAM. The order of the burst sequence is defined by the MODE input pin. The MODE pin selects between linear and interleaved burst sequence. The ADV/$\overline{LD}$ signal is used to load a new external address (ADV/$\overline{LD}$=LOW) or increment the internal burst counter (ADV/$\overline{LD}$=HIGH)
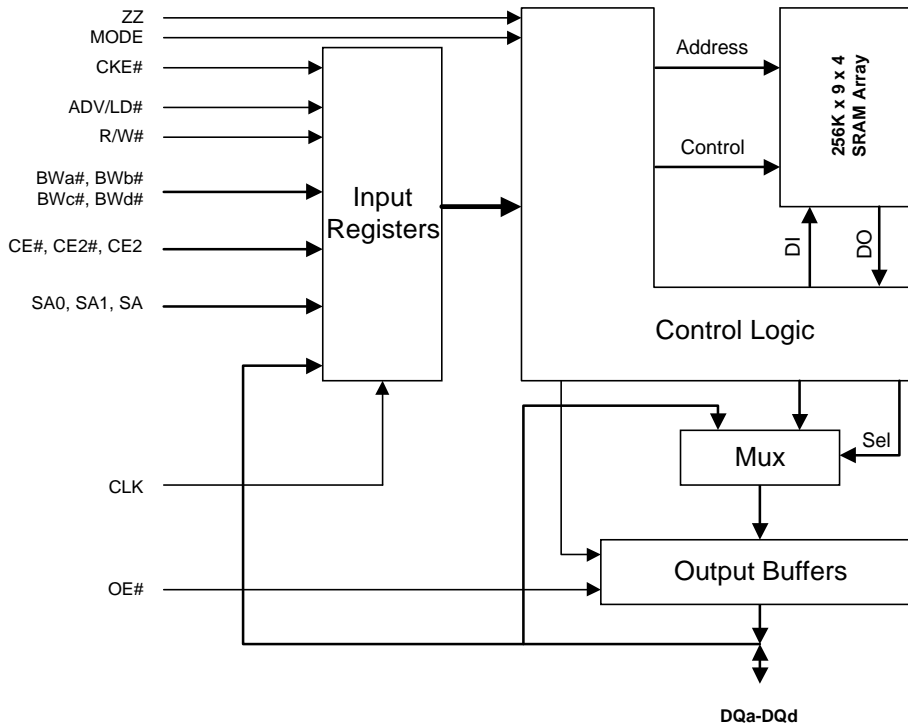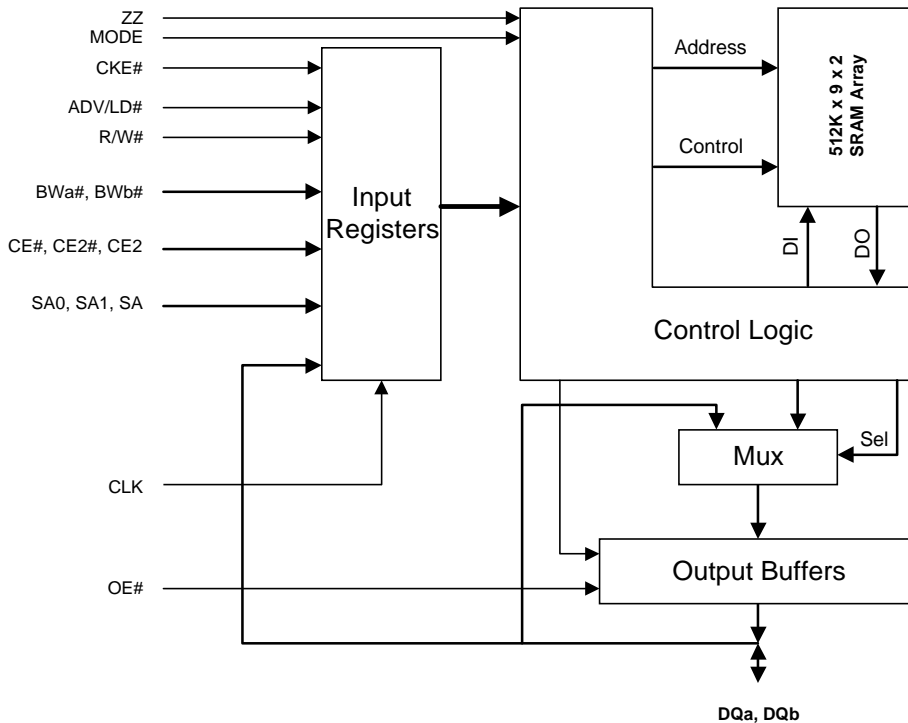
Output Enable ($\overline{OE}$), Snooze Enable (ZZ) and burst sequence select (MODE) are the asynchronous signals. $\overline{OE}$ can be used to disable the outputs at any given time. ZZ may be tied to LOW if it is not used.

Four pins are used to implement JTAG test capabilities. The JTAG circuitry is used to serially shift data to and from the device. JTAG inputs use LVTTL/LVCMOS levels to shift data during this testing mode of operation.

## Selection Guide

| | 7C1355A-133/ 71256ZB36-6.5 7C1357A-133/ 71512ZB18-6.5 | 7C1355A-117/ 71256ZB36-7 7C1357A-117/ 71512ZB18-7 | 7C1355A-100/ 71256ZB36-7.5 7C1357A-100/ 71512ZB18-7.5 | 7C1355A1-100/ 71256ZB36-8 7C1357A1-100/ 71512ZB18-8 |
|---|---|---|---|---|
| Maximum Access Time (ns) | 6.5 | 7 | 7.5 | 8 |
| Maximum Operating Current (mA) | 410 | 385 | 350 | 350 |
| Maximum CMOS Standby Current (mA) | 30 | 30 | 30 | 30 |

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**Functional Block Diagram 256Kx36**[1]

ZZ
MODE
CKE#
ADV/LD#
R/W#
BWa#, BWb#
BWc#, BWd#
CE#, CE2#, CE2
SA0, SA1, SA

Input Registers

256K x 9 x 4 SRAM Array

Address

Control

DI    DO

Control Logic

CLK

Mux

Sel

OE#

Output Buffers

**DQa-DQd**

**Functional Block Diagram 512Kx18**[1]

ZZ
MODE
CKE#
ADV/LD#
R/W#
BWa#, BWb#
CE#, CE2#, CE2
SA0, SA1, SA

Input Registers

512K x 9 x 2 SRAM Array

Address

Control

DI    DO

Control Logic

CLK

Mux

Sel

OE#

Output Buffers

**DQa, DQb**

**Note:**
1. The Functional Block Diagram illustrates simplified device operation. See Truth Table, pin descriptions and timing diagrams for detailed information.
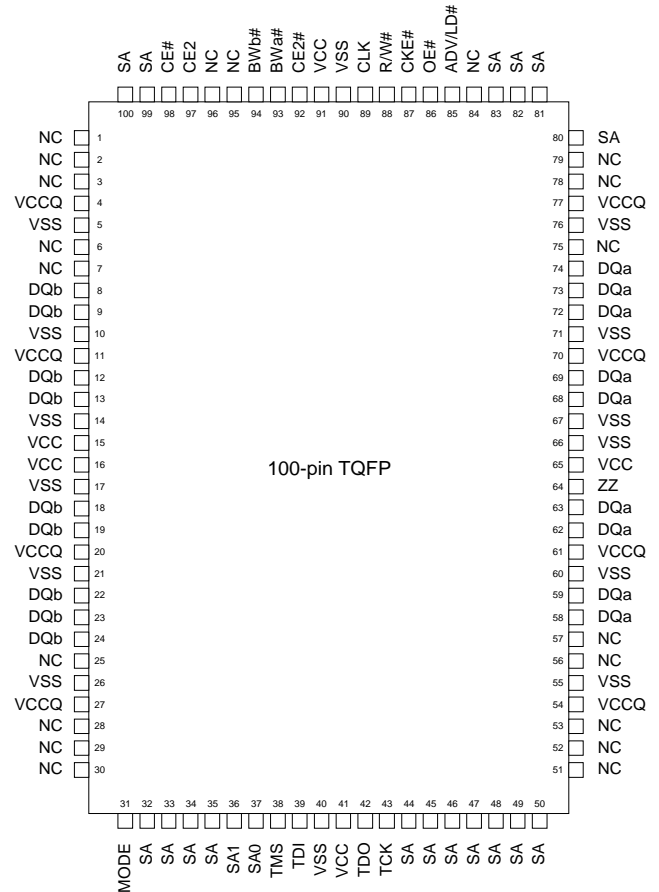
*PRELIMINARY*

**Pin Configurations**

**100-Pin TQFP Packages**

**256Kx36—CY7C1355A/GVT71256ZB36**
**Top View**
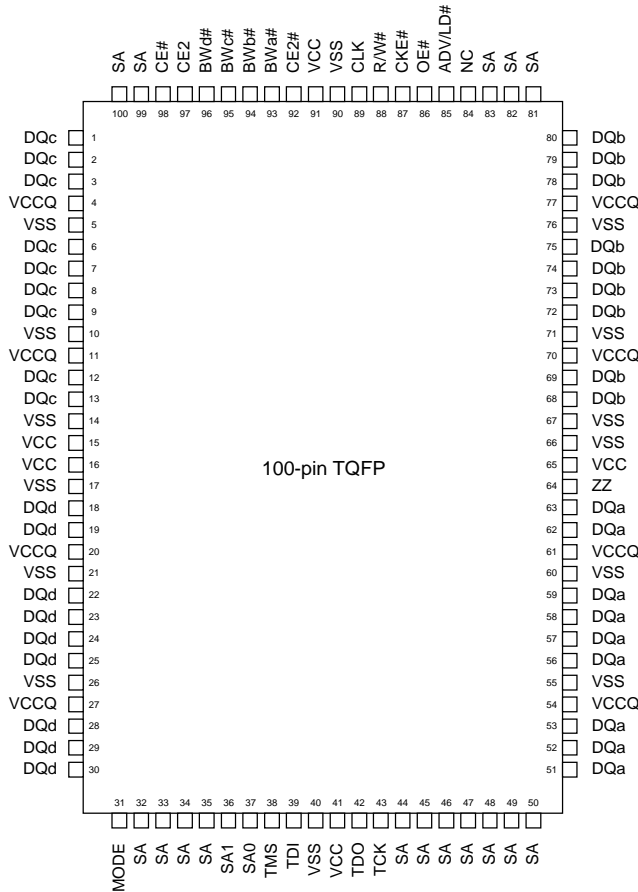


**512Kx18—CY7C1357A/GVT71512ZB18**
**Top View**

*PRELIMINARY*

## Pin Configurations (continued)

**119-Ball Bump BGA**
**256Kx36—CY7C1355A/GVT71256ZB36**
**Top View**

|   | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|
| **A** | $V_{CCQ}$ | SA | SA | NC | SA | SA | $V_{CCQ}$ |
| **B** | NC | $CE_2$ | A | ADV/$\overline{LD}$ | SA | $\overline{CE}_2$ | NC |
| **C** | NC | SA | SA | $V_{CC}$ | SA | SA | NC |
| **D** | DQc | DQc | $V_{SS}$ | NC | $V_{SS}$ | DQb | DQb |
| **E** | DQc | DQc | $V_{SS}$ | $\overline{CE}$ | $V_{SS}$ | DQb | DQb |
| **F** | $V_{CCQ}$ | DQc | $V_{SS}$ | $\overline{OE}$ | $V_{SS}$ | DQb | $V_{CCQ}$ |
| **G** | DQc | DQc | $\overline{BWc}$ | SA | $\overline{BWb}$ | DQb | DQb |
| **H** | DQc | DQc | $V_{SS}$ | R/$\overline{W}$ | $V_{SS}$ | DQb | DQb |
| **J** | $V_{CCQ}$ | $V_{CC}$ | NC | $V_{CC}$ | NC | $V_{CC}$ | $V_{CCQ}$ |
| **K** | DQd | DQd | $V_{SS}$ | CLK | $V_{SS}$ | DQa | DQa |
| **L** | DQd | DQd | $\overline{BWd}$ | NC | $\overline{BWa}$ | DQa | DQa |
| **M** | $V_{CCQ}$ | DQd | $V_{SS}$ | $\overline{CKE}$ | $V_{SS}$ | DQa | $V_{CCQ}$ |
| **N** | DQd | DQd | $V_{SS}$ | SA1 | $V_{SS}$ | DQa | DQa |
| **P** | DQd | DQd | $V_{SS}$ | SA0 | $V_{SS}$ | DQa | DQa |
| **R** | NC | SA | MODE | $V_{CC}$ | $V_{SS}$ | SA | NC |
| **T** | NC | NC | SA | SA | SA | NC | ZZ |
| **U** | $V_{CCQ}$ | TMS | TDI | TCK | TDO | NC | $V_{CCQ}$ |

**512Kx18—CY7C1357A/GVT71512ZB18**
**Top View**

|   | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|
| **A** | $V_{CCQ}$ | SA | SA | NC | SA | SA | $V_{CCQ}$ |
| **B** | NC | $CE_2$ | SA | ADV/$\overline{LD}$ | SA | $\overline{CE}_2$ | NC |
| **C** | NC | SA | SA | $V_{CC}$ | SA | SA | NC |
| **D** | DQb | NC | $V_{SS}$ | NC | $V_{SS}$ | DQa | NC |
| **E** | NC | DQb | $V_{SS}$ | $\overline{CE}$ | $V_{SS}$ | NC | DQa |
| **F** | $V_{CCQ}$ | NC | $V_{SS}$ | $\overline{OE}$ | $V_{SS}$ | DQa | $V_{CCQ}$ |
| **G** | NC | DQb | $\overline{BWb}$ | SA | $V_{SS}$ | NC | DQa |
| **H** | DQb | NC | $V_{SS}$ | R/$\overline{W}$ | $V_{SS}$ | DQa | NC |
| **J** | $V_{CCQ}$ | $V_{CC}$ | NC | $V_{CC}$ | NC | $V_{CC}$ | $V_{CCQ}$ |
| **K** | NC | DQb | $V_{SS}$ | CLK | $V_{SS}$ | NC | DQa |
| **L** | DQb | NC | $V_{SS}$ | NC | $\overline{BWa}$ | DQa | NC |
| **M** | $V_{CCQ}$ | DQb | $V_{SS}$ | $\overline{CKE}$ | $V_{SS}$ | NC | $V_{CCQ}$ |
| **N** | DQb | NC | $V_{SS}$ | SA1 | $V_{SS}$ | DQa | NC |
| **P** | NC | DQb | $V_{SS}$ | SA0 | $V_{SS}$ | NC | DQa |
| **R** | NC | SA | MODE | $V_{CC}$ | NC | SA | NC |
| **T** | NC | SA | SA | NC | SA | SA | ZZ |
| **U** | $V_{CCQ}$ | TMS | TDI | TCK | TDO | NC | $V_{CCQ}$ |

### Pin Descriptions (CY7C1355A/GVT71256ZB36)

| 256Kx36 TQFP Pins | 256Kx36 PBGA Pins | Name | Type | Description |
|---|---|---|---|---|
| 37, 36, 32, 33, 34, 35, 44, 45, 46, 47, 48, 49, 50, 81, 82, 83, 99, 100 | 4P 4N 2A, 3A, 5A, 6A, 3B, 5B, 2C, 3C, 5C, 6C, 4G, 2R, 6R, 3T, 4T, 5T | SA0, SA1, SA | Input-Synchronous | Synchronous Address Inputs: The address register is triggered by a combination of the rising edge of CLK, ADV/$\overline{LD}$ LOW, $\overline{CKE}$ LOW and true chip enables. SA0 and SA1 are the two least significant bits of the address field and set the internal burst counter if burst cycle is initiated. |
| 93, 94, 95, 96 | 5L 5G 3G 3L | $\overline{BWa}$, $\overline{BWb}$, $\overline{BWc}$, $\overline{BWd}$ | Input-Synchronous | Synchronous Byte Write Enables: Each 9-bit byte has its own active LOW byte write enable. On load write cycles (when R/$\overline{W}$ and ADV/$\overline{LD}$ are sampled LOW), the appropriate byte write signal ($\overline{BWx}$) must be valid. The byte write signal must also be valid on each cycle of a burst write. Byte write signals are ignored when R/$\overline{W}$ is sampled HIGH. The appropriate byte(s) of data are written into the device one cycle later. $\overline{BWa}$ controls DQa pins; $\overline{BWb}$ controls DQb pins; $\overline{BWc}$ controls DQc pins; $\overline{BWd}$ controls DQd pins. $\overline{BWx}$ can all be tied LOW if always doing a write to the entire 36-bit word. |
| 87 | 4M | $\overline{CKE}$ | Input-Synchronous | Synchronous Clock Enable Input: When $\overline{CKE}$ is sampled HIGH, all other synchronous inputs, including clock are ignored and outputs remain unchanged. The effect of $\overline{CKE}$ sampled HIGH on the device outputs is as if the LOW-to-HIGH clock transition did not occur. For normal operation, $\overline{CKE}$ must be sampled LOW at rising edge of clock. |
| 88 | 4H | R/$\overline{W}$ | Input-Synchronous | Read Write: R/$\overline{W}$ signal is a synchronous input that identifies whether the current loaded cycle and the subsequent burst cycles initiated by ADV/$\overline{LD}$ is a Read or Write operation. The data bus activity for the current cycle takes place one clock cycle later. |
| 89 | 4K | CLK | Input-Synchronous | Clock: This is the clock input to CY7C1355A/GVT71256ZB36. Except for $\overline{OE}$, ZZ, and MODE, all timing references for the device are made with respect to the rising edge of CLK. |
| 98, 92 | 4E, 6B | $\overline{CE}$, $\overline{CE}_2$ | Input-Synchronous | Synchronous Active LOW Chip Enable: $\overline{CE}$ and $\overline{CE}_2$ are used with CE$_2$ to enable the CY7C1355A/GVT71256ZB36. $\overline{CE}$ or $\overline{CE}_2$ sampled HIGH or CE$_2$ sampled LOW, along with ADV/$\overline{LD}$ LOW at the rising edge of clock, initiates a deselect cycle. The data bus will be High-Z one clock cycle after chip deselect is initiated. |
| 97 | 2B | CE$_2$ | Input-Synchronous | Synchronous Active High Chip enable: CE$_2$ is used with $\overline{CE}$ and $\overline{CE}_2$ to enable the chip. CE$_2$ has inverted polarity but otherwise is identical to $\overline{CE}$ and $\overline{CE}_2$. |
| 86 | 4F | $\overline{OE}$ | Input | Asynchronous Output Enable: $\overline{OE}$ must be LOW to read data. When $\overline{OE}$ is HIGH, the I/O pins are in high-impedance state. $\overline{OE}$ does not need to be actively controlled for read and write cycles. In normal operation, $\overline{OE}$ can be tied LOW. |
| 85 | 4B | ADV/$\overline{LD}$ | Input-Synchronous | Advance/Load: ADV/$\overline{LD}$ is a synchronous input that is used to load the internal registers with new address and control signals when it is sampled LOW at the rising edge of clock with the chip is selected. When ADV/$\overline{LD}$ is sampled HIGH, then the internal burst counter is advanced for any burst that was in progress. The external addresses and R/$\overline{W}$ are ignored when ADV/$\overline{LD}$ is sampled HIGH. |
| 31 | 3R | MODE | Input-Static | Burst Mode: When MODE is HIGH or NC, the interleaved burst sequence is selected. When MODE is LOW, the linear burst sequence is selected. MODE is a static DC input. |
| 64 | 7T | ZZ | Input-Asynchronous | Snooze Enable: This active HIGH input puts the device in low power consumption standby mode. For normal operation, this input has to be either LOW or NC. |

### Pin Descriptions (CY7C1355A/GVT71256ZB36) (continued)

| 256Kx36 TQFP Pins | 256Kx36 PBGA Pins | Name | Type | Description |
|---|---|---|---|---|
| 51, 52, 53, 56–59, 62, 63 68, 69, 72–75, 78, 79, 80 1, 2, 3, 6–9, 12, 13 18, 19, 22–25, 28, 29, 30 | (a) 6P, 7P, 7N, 6N, 6M, 6L, 7L, 6K, 7K, (b) 7H, 6H, 7G, 6G, 6F, 6E, 7E, 7D, 6D, (c) 2D, 1D, 1E, 2E, 2F, 1G, 2G, 1H, 2H, (d) 1K, 2K, 1L, 2L, 2M, 1N, 2N, 1P, 2P | DQa DQb DQc DQd | Input/ Output | Data Inputs/Outputs: Both the data input path and data output path are registered and triggered by the rising edge of CLK. Byte "a" is DQa pins; Byte "b" is DQb pins; Byte "c" is DQc pins; Byte "d" is DQd pins. |
| 38 39 43 | 2U 3U 4U | TMS TDI TCK | Input | IEEE 1149.1 test inputs. LVTTL-level inputs. If Serial Boundary Scan (JTAG) is not used, these pins can be floating (i.e., No Connect) or be connected to $V_{CC}$. |
| 42 | 5U | TDO | Output | IEEE 1149.1 test output. LVTTL-level output. If Serial Boundary Scan (JTAG) is not used, these pins can be floating (i.e., No Connect). |
| 15, 16, 41, 65, 91 | 4C, 2J, 4J, 6J, 4R | $V_{CC}$ | Supply | Power Supply: +3.3V –5% and +5%. |
| 5, 10, 14, 17, 21, 26, 40, 55, 60, 66, 67, 71, 76, 90 | 3D, 5D, 3E, 5E, 3F, 5F, 3H, 5H, 3K, 5K, 3M, 5M, 3N, 5N, 3P, 5P, 5R | $V_{SS}$ | Ground | Ground: GND. |
| 4, 11, 20, 27, 54, 61, 70, 77 | 1A, 7A, 1F, 7F, 1J, 7J, 1M, 7M, 1U, 7U | $V_{CCQ}$ | I/O Supply | Output Buffer Supply: +3.3V –0.165V and +0.165V for 3.3V I/O. +2.5V –0.125V and +0.4V for 2.5V I/O. |
| 84 | 4A, 1B, 7B, 1C, 7C, 4D, 3J, 5J, 4L, 1R, 7R, 1T, 2T, 6T, 6U | NC | - | No Connect: These signals are not internally connected. It can be left floating or be connected to $V_{CC}$ or to GND. |

### Pin Descriptions (CY7C1357A/GVT71512ZB18)

| 512Kx18 TQFP Pins | 512Kx18 PBGA Pins | Name | Type | Description |
|---|---|---|---|---|
| 37, 36, 32, 33, 34, 35, 44, 45, 46, 47, 48, 49, 50, 80, 81, 82, 83, 99, 100 | 4P 4N 2A, 3A, 5A, 6A, 3B, 5B, 6B, 2C, 3C, 5C, 6C, 4G, 2R, 6R, 2T, 3T, 5T, 6T | SA0, SA1, SA | Input-Synchronous | Synchronous Address Inputs: The address register is triggered by a combination of the rising edge of CLK, ADV/$\overline{LD}$ LOW, $\overline{CKE}$ LOW and true chip enables. SA0 and SA1 are the two least significant bits of the address field and set the internal burst counter if burst cycle is initiated. |
| 93, 94, | 5L 3G | $\overline{BWa}$, $\overline{BWb}$ | Input-Synchronous | Synchronous Byte Write Enables: Each 9-bit byte has its own active low byte write enable. On load write cycles (when R/$\overline{W}$ and ADV/$\overline{LD}$ are sampled LOW), the appropriate byte write signal ($\overline{BWx}$) must be valid. The byte write signal must also be valid on each cycle of a burst write. Byte write signals are ignored when R/$\overline{W}$ is sampled HIGH. The appropriate byte(s) of data are written into the device one cycle later. $\overline{BWa}$ controls DQa pins; $\overline{BWb}$ controls DQb pins. $\overline{BWx}$ can all be tied LOW if always doing write to the entire 18-bit word. |

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## Pin Descriptions (CY7C1357A/GVT71512ZB18) (continued)

| 512Kx18 TQFP Pins | 512Kx18 PBGA Pins | Name | Type | Description |
|---|---|---|---|---|
| 87 | 4M | $\overline{\text{CKE}}$ | Input-Synchronous | Synchronous Clock Enable Input: When $\overline{\text{CKE}}$ is sampled HIGH, all other synchronous inputs, including clock are ignored and outputs remain unchanged. The effect of $\overline{\text{CKE}}$ sampled HIGH on the device outputs is as if the LOW-to-HIGH clock transition did not occur. For normal operation, $\overline{\text{CKE}}$ must be sampled LOW at rising edge of clock. |
| 88 | 4H | $\text{R}/\overline{\text{W}}$ | Input-Synchronous | Read Write: $\text{R}/\overline{\text{W}}$ signal is a synchronous input that identifies whether the current loaded cycle and the subsequent burst cycles initiated by $\text{ADV}/\overline{\text{LD}}$ is a Read or Write operation. The data bus activity for the current cycle takes place one clock cycle later. |
| 89 | 4K | CLK | Input-Synchronous | Clock: This is the clock input to CY7C1357A/GVT71512ZB18. Except for $\overline{\text{OE}}$, ZZ and MODE, all timing references for the device are made with respect to the rising edge of CLK. |
| 98, 92 | 4E, 6B | $\overline{\text{CE}}$, $\overline{\text{CE}}_2$ | Input-Synchronous | Synchronous Active Low Chip Enable: $\overline{\text{CE}}$ and $\overline{\text{CE}}_2$ are used with $\text{CE}_2$ to enable the CY7C1357A/GVT71512ZB18. $\overline{\text{CE}}$ or $\overline{\text{CE}}_2$ sampled HIGH or $\text{CE}_2$ sampled LOW, along with $\text{ADV}/\overline{\text{LD}}$ LOW at the rising edge of clock, initiates a deselect cycle. The data bus will be High-Z one clock cycle after chip deselect is initiated. |
| 97 | 2B | $\text{CE}_2$ | Input-Synchronous | Synchronous Active High Chip enable: $\text{CE}_2$ is used with $\overline{\text{CE}}$ and $\overline{\text{CE}}_2$ to enable the chip. $\text{CE}_2$ has inverted polarity but otherwise is identical to $\overline{\text{CE}}$ and $\overline{\text{CE}}_2$. |
| 86 | 4F | $\overline{\text{OE}}$ | Input | Asynchronous Output Enable: $\overline{\text{OE}}$ must be LOW to read data. When $\overline{\text{OE}}$ is HIGH, the I/O pins are in high-impedance state. $\overline{\text{OE}}$ does not need to be actively controlled for read and write cycles. In normal operation, $\overline{\text{OE}}$ can be tied LOW. |
| 85 | 4B | $\text{ADV}/\overline{\text{LD}}$ | Input-Synchronous | Advance/Load: $\text{ADV}/\overline{\text{LD}}$ is a synchronous input that is used to load the internal registers with new address and control signals when it is sampled LOW at the rising edge of clock with the chip is selected. When $\text{ADV}/\overline{\text{LD}}$ is sampled HIGH, then the internal burst counter is advanced for any burst that was in progress. The external addresses and $\text{R}/\overline{\text{W}}$ are ignored when $\text{ADV}/\overline{\text{LD}}$ is sampled HIGH. |
| 31 | 3R | MODE | Input-Static | Burst Mode: When MODE is HIGH or NC, the interleaved burst sequence is selected. When MODE is LOW, the linear burst sequence is selected. MODE is a static DC input. |
| 64 | 7T | ZZ | Input Asynchronous | Snooze Enable: This active HIGH input puts the device in low power consumption standby mode. For normal operation, this input has to be either LOW or NC. |
| 58, 59, 62, 63, 68, 69, 72, 73, 74 8, 9, 12, 13, 18, 19, 22, 23, 24 | (a) 6D, 7E, 6F, 7G, 6H, 7K, 6L, 6N, 7P (b) 1D, 2E, 2G, 1H, 2K, 1L, 2M, 1N, 2P | DQa DQb | Input/Output | Data Inputs/Outputs: Both the data input path and data output path are registered and triggered by the rising edge of CLK. Byte "a" is DQa pins; Byte "b" is DQb pins. |
| 38 39 43 | 2U 3U 4U | TMS TDI TCK | Input | IEEE 1149.1 test inputs. LVTTL-level inputs. If Serial Boundary Scan (JTAG) is not used, these pins can be floating (i.e., No Connect) or be connected to $V_{CC}$. |
| 42 | 5U | TDO | Output | IEEE 1149.1 test output. LVTTL-level output. If Serial Boundary Scan (JTAG) is not used, these pins can be floating (i.e., No Connect). |
| 15, 16, 41, 65, 91 | 4C, 2J, 4J, 6J, 4R | $V_{CC}$ | Supply | Power Supply: +3.3V –5% and +5%. |

## Pin Descriptions (CY7C1357A/GVT71512ZB18) (continued)

| 512Kx18 TQFP Pins | 512Kx18 PBGA Pins | Name | Type | Description |
|---|---|---|---|---|
| 5, 10, 14, 17, 21, 26, 40, 55, 60, 66, 67, 71, 76, 90 | 3D, 5D, 3E, 5E, 3F, 5F, 5G, 3H, 5H, 3K, 5K, 3L, 3M, 5M, 3N, 5N, 3P, 5P | $V_{SS}$ | Ground | Ground: GND. |
| 4, 11, 20, 27, 54, 61, 70, 77 | 1A, 7A, 1F, 7F, 1J, 7J, 1M, 7M, 1U, 7U | $V_{CCQ}$ | I/O Supply | Output Buffer Supply: +3.3V –0.165V and +0.165V for 3.3V I/O. +2.5V –0.125V and +0.4V for 2.5V I/O. |
| 1-3, 6, 7, 25, 28-30, 51-53, 56, 57, 75, 78, 79, 84, 95, 96 | 4A, 1B, 7B, 1C, 7C, 2D, 4D, 7D, 1E, 6E, 2F, 1G, 6G, 2H, 7H, 3J, 5J, 1K, 6K, 2L, 4L, 7L, 6M, 2N, 7N, 1P, 6P, 1R, 7R, 1T, 4T, 6U | NC | - | No Connect: These signals are not internally connected. It can be left floating or be connected to $V_{CC}$ or to GND. |

## Partial Truth Table for Read/Write[2]

| Function | R/$\overline{W}$ | $\overline{BWa}$ | $\overline{BWb}$ | $\overline{BWc}$[4] | $\overline{BWd}$[4] |
|---|---|---|---|---|---|
| Read | H | X | X | X | X |
| No Write | L | H | H | H | H |
| Write Byte a (DQa)[3] | L | L | H | H | H |
| Write Byte b (DQb)[3] | L | H | L | H | H |
| Write Byte c (DQc)[3] | L | H | H | L | H |
| Write Byte d (DQd)[3] | L | H | H | H | L |
| Write all bytes | L | L | L | L | L |

## Interleaved Burst Address Table (MODE = $V_{CC}$ or NC)

| First Address (external) | Second Address (internal) | Third Address (internal) | Fourth Address (internal)[5] |
|---|---|---|---|
| A...A$_{00}$ | A...A$_{01}$ | A...A$_{10}$ | A...A$_{11}$ |
| A...A$_{01}$ | A...A$_{00}$ | A...A$_{11}$ | A...A$_{10}$ |
| A...A$_{10}$ | A...A$_{11}$ | A...A$_{00}$ | A...A$_{01}$ |
| A...A$_{11}$ | A...A$_{10}$ | A...A$_{01}$ | A...A$_{00}$ |

## Linear Burst Address Table (MODE = $V_{SS}$)

| First Address (external) | Second Address (internal) | Third Address (internal) | Fourth Address (internal)[5] |
|---|---|---|---|
| A...A$_{00}$ | A...A$_{01}$ | A...A$_{10}$ | A...A$_{11}$ |
| A...A$_{01}$ | A...A$_{10}$ | A...A$_{11}$ | A...A$_{00}$ |
| A...A$_{10}$ | A...A$_{11}$ | A...A$_{00}$ | A...A$_{01}$ |
| A...A$_{11}$ | A...A$_{00}$ | A...A$_{01}$ | A...A$_{10}$ |

**Notes:**
2. L means logic LOW. H means logic HIGH. X means "Don't Care."
3. Multiple bytes may be selected during the same cycle.
4. BWc and BWd apply to 256Kx36 device only.
5. Upon completion of the Burst sequence, the counter wraps around to its initial state and continues counting.

*PRELIMINARY*

## Functional Timing Diagram[6, 7, 8]

| CYCLE | n+19 | n+20 | n+21 | n+22 | n+23 | n+24 | n+25 | n+26 | n+27 |
|---|---|---|---|---|---|---|---|---|---|
| ADDRESS (SA0, SA1, SA ) | $A_{19}$ | $A_{20}$ | $A_{21}$ | $A_{22}$ | $A_{23}$ | $A_{24}$ | $A_{25}$ | $A_{26}$ | $A_{27}$ |
| CONTROL (R/W#, BWx#, ADV/LD#) | $C_{19}$ | $C_{20}$ | $C_{21}$ | $C_{22}$ | $C_{23}$ | $C_{24}$ | $C_{25}$ | $C_{26}$ | $C_{27}$ |
| DATA DQ[a:d] | $DQ_{18}$ | $DQ_{19}$ | $DQ_{20}$ | $DQ_{21}$ | $DQ_{22}$ | $DQ_{23}$ | $DQ_{24}$ | $DQ_{25}$ | $DQ_{26}$ |
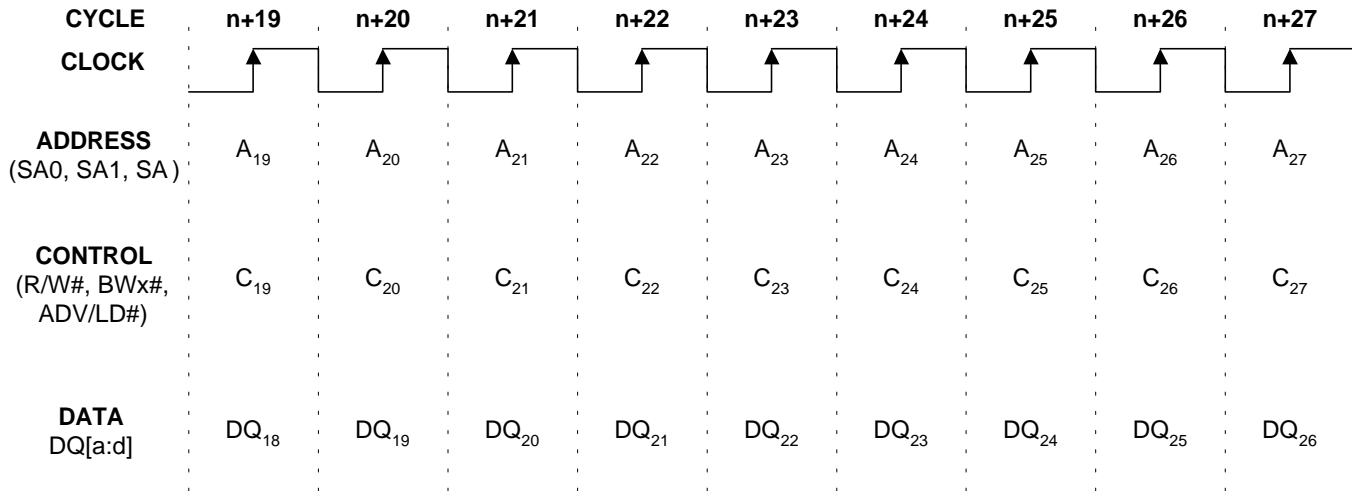
## Truth Table[9, 10, 11, 12, 13, 14, 15, 16, 17]

| Operation | Previous Cycle | Address Used | R/$\overline{W}$ | ADV/$\overline{LD}$ | $\overline{CE}$ | $\overline{CKE}$ | $\overline{BWx}$ | $\overline{OE}$ | DQ (1 cycle later) |
|---|---|---|---|---|---|---|---|---|---|
| Deselect Cycle | X | X | X | L | H | L | X | X | High-Z |
| Continue Deselect/NOP[18] | Deselect | X | X | H | X | L | X | X | High-Z |
| Read Cycle (Begin Burst) | X | External | H | L | L | L | X | X | Q |
| Read Cycle (Continue Burst)[18] | Read | Next | X | H | X | L | X | X | Q |
| Dummy Read (Begin Burst)[19] | X | External | H | L | L | L | X | H | High-Z |
| Dummy Read (Continue Burst)[18, 19] | Read | Next | X | H | X | L | X | H | High-Z |
| Write Cycle (Begin Burst) | X | External | L | L | L | L | L | X | D |
| Write Cycle (Continue Burst)[18] | Write | Next | X | H | X | L | L | X | D |
| Abort Write (Begin Burst)[19] | X | External | L | L | L | L | H | X | High-Z |
| Abort Write (Continue Burst)[18, 19] | Write | Next | X | H | X | L | H | X | High-Z |
| Ignore Clock Edge/NOP[20] | X | X | X | H | X | H | X | X | - |

**Notes:**

6. This assumes that $\overline{CKE}$, $\overline{CE}$, $CE_2$ and $\overline{CE_2}$ are all True.
7. All addresses, control and data-in are only required to meet set-up and hold time with respect to the rising edge of clock. Data out is valid after a clock-to-data delay from the rising edge of clock.
8. DQc and DQd apply to 256Kx36 device only.
9. L means logic LOW. H means logic HIGH. X means "Don't Care." High-Z means High Impedance. $\overline{BWx}$ = L means [$\overline{BWa}*\overline{BWb}*\overline{BWc}*\overline{BWd}$] equals LOW. $\overline{BWx}$ = H means [$\overline{BWa}*\overline{BWb}*\overline{BWc}*\overline{BWd}$] equals HIGH. BWc and BWd apply to 256Kx36 device only.
10. $\overline{CE}$ = H means $\overline{CE}$ and $\overline{CE_2}$ are LOW along with $CE_2$ being HIGH. $\overline{CE}$ = L means $\overline{CE}$ or $CE_2$ is HIGH or $\overline{CE_2}$ is LOW. $\overline{CE}$ = X means $\overline{CE}$, $\overline{CE_2}$, and $CE_2$ are "Don't Care."
11. $\overline{BWa}$ enables WRITE to byte "a" (DQa pins). $\overline{BWb}$ enables WRITE to byte "b" (DQb pins). $\overline{BWc}$ enables WRITE to byte "c" (DQc pins). $\overline{BWd}$ enables WRITE to byte "d" (DQd pins). DQc, DQd, $\overline{BWc}$, and $\overline{BWd}$ apply to 256Kx36 device only.
12. The device is not in Snooze Mode, i.e., the ZZ pin is LOW.
13. During Snooze Mode, the ZZ pin is HIGH and all the address pins and control pins are "Don't Care." The Snooze Mode can only be entered one cycle after the WRITE cycle, otherwise the WRITE cycle may not be completed.
14. All inputs, except $\overline{OE}$, ZZ, and MODE pins, must meet set-up time and hold time specification against the clock (CLK) LOW-to-HIGH transition edge.
15. $\overline{OE}$ may be tied to LOW for all the operation. This device automatically turns off the output driver during WRITE cycle.
16. Device outputs are ensured to be in High-Z during device power-up.
17. This device contains a 2-bit burst counter. The address counter is incremented for all Continue Burst cycles. Address wraps to the initial address every fourth burst cycle.
18. Continue Burst cycles, whether READ or WRITE, use the same control signals. The type of cycle performed, READ or WRITE, depends upon the R/$\overline{W}$ control signal at the BEGIN BURST cycle. A Continue Deselect cycle can only be entered if a Deselect cycle is executed first.
19. Dummy Read and Abort WRITE cycles can be entered to set up subsequent READ or WRITE cycles or to increment the burst counter.
20. When an Ignore Clock Edge cycle enters, the output data (Q) will remain the same if the previous cycle is READ cycle or remain High-Z if the previous cycle is WRITE or Deselect cycle.

## IEEE 1149.1 Serial Boundary Scan (JTAG)

### Overview

This device incorporates a serial boundary scan access port (TAP). This port is designed to operate in a manner consistent with IEEE Standard 1149.1-1990 (commonly referred to as JTAG), but does not implement all of the functions required for IEEE 1149.1 compliance. Certain functions have been modified or eliminated because their implementation places extra delays in the critical speed path of the device. Nevertheless, the device supports the standard TAP controller architecture (the TAP controller is the state machine that controls the TAPs operation) and can be expected to function in a manner that does not conflict with the operation of devices with IEEE Standard 1149.1 compliant TAPs. The TAP operates using LVTTL/LVCMOS logic level signaling.

### Disabling the JTAG Feature

It is possible to use this device without using the JTAG feature. To disable the TAP controller without interfering with normal operation of the device, TCK should be tied LOW ($V_{SS}$) to prevent clocking the device. TDI and TMS are internally pulled up and may be unconnected. They may alternately be pulled up to $V_{CC}$ through a resistor. TDO should be left unconnected. Upon power-up the device will come up in a reset state which will not interfere with the operation of the device.

## Test Access Port (TAP)

### TCK - Test Clock (INPUT)

Clocks all TAP events. All inputs are captured on the rising edge of TCK and all outputs propagate from the falling edge of TCK.

### TMS - Test Mode Select (INPUT)

The TMS input is sampled on the rising edge of TCK. This is the command input for the TAP controller state machine. It is allowable to leave this pin unconnected if the TAP is not used. The pin is pulled up internally, resulting in a logic HIGH level.

### TDI - Test Data In (INPUT)

The TDI input is sampled on the rising edge of TCK. This is the input side of the serial registers placed between TDI and TDO. The register placed between TDI and TDO is determined by the state of the TAP controller state machine and the instruction that is currently loaded in the TAP instruction register (refer to *Figure 1*, TAP Controller State Diagram). It is allowable to leave this pin unconnected if it is not used in an application. The pin is pulled up internally, resulting in a logic HIGH level. TDI is connected to the most significant bit (MSB) of any register. (See *Figure 2*.)

### TDO - Test Data Out (OUTPUT)

The TDO output pin is used to serially clock data-out from the registers. The output that is active depending on the state of the TAP state machine (refer to *Figure 1*, TAP Controller State Diagram). Output changes in response to the falling edge of TCK. This is the output side of the serial registers placed between TDI and TDO. TDO is connected to the least significant bit (LSB) of any register. (See *Figure 2*.)

### Performing a TAP Reset

The TAP circuitry does not have a reset pin ($\overline{TRST}$, which is optional in the IEEE 1149.1 specification). A RESET can be performed for the TAP controller by forcing TMS HIGH ($V_{CC}$) for five rising edges of TCK and pre-loads the instruction register with the IDCODE command. This type of reset does not affect the operation of the system logic. The reset affects test logic only.

At power-up, the TAP is reset internally to ensure that TDO is in a High-Z state.

## Test Access Port (TAP) Registers

### Overview

The various TAP registers are selected (one at a time) via the sequences of ones and zeros input to the TMS pin as the TCK is strobed. Each of the TAPs registers are serial shift registers that capture serial input data on the rising edge of TCK and push serial data out on subsequent falling edge of TCK. When a register is selected, it is connected between the TDI and TDO pins.

### Instruction Register

The instruction register holds the instructions that are executed by the TAP controller when it is moved into the run test/idle or the various data register states. The instructions are three bits long. The register can be loaded when it is placed between the TDI and TDO pins. The parallel outputs of the instruction register are automatically preloaded with the IDCODE instruction upon power-up or whenever the controller is placed in the test-logic reset state. When the TAP controller is in the Capture-IR state, the two least significant bits of the serial instruction register are loaded with a binary "01" pattern to allow for fault isolation of the board-level serial test data path.

### Bypass Register

The bypass register is a single-bit register that can be placed between TDI and TDO. It allows serial test data to be passed through the device TAP to another device in the scan chain with minimum delay. The bypass register is set LOW ($V_{SS}$) when the BYPASS instruction is executed.

### Boundary Scan Register

The Boundary scan register is connected to all the input and bidirectional I/O pins (not counting the TAP pins) on the device. This also includes a number of NC pins that are reserved for future needs. There are a total of 70 bits for x36 device and 51 bits for x18 device. The boundary scan register, under the control of the TAP controller, is loaded with the contents of the device I/O ring when the controller is in Capture-DR state and then is placed between the TDI and TDO pins when the controller is moved to Shift-DR state. The EXTEST, SAMPLE/PRELOAD and SAMPLE-Z instructions can be used to capture the contents of the I/O ring.

The Boundary Scan Order table describes the order in which the bits are connected. The first column defines the bit's position in the boundary scan register. The MSB of the register is connected to TDI, and LSB is connected to TDO. The second column is the signal name and the third column is the bump number. The third column is the TQFP pin number and the fourth column is the BGA bump number.

### Identification (ID) Register

The ID Register is a 32-bit register that is loaded with a device and vendor specific 32-bit code when the controller is put in Capture-DR state with the IDCODE command loaded in the instruction register. The register is then placed between the TDI and TDO pins when the controller is moved into Shift-DR state. Bit 0 in the register is the LSB and the first to reach TDO when shifting begins. The code is loaded from a 32-bit on-chip ROM. It describes various attributes of the device as described in the Identification Register Definitions table.

## TAP Controller Instruction Set

### Overview

There are two classes of instructions defined in the IEEE Standard 1149.1-1990; the standard (public) instructions and device specific (private) instructions. Some public instructions are mandatory for IEEE 1149.1 compliance. Optional public instructions must be implemented in prescribed ways.

Although the TAP controller in this device follows the IEEE 1149.1 conventions, it is not IEEE 1149.1 compliant because some of the mandatory instructions are not fully implemented. The TAP on this device may be used to monitor all input and I/O pads, but can not be used to load address, data, or control signals into the device or to preload the I/O buffers. In other words, the device will not perform IEEE 1149.1 EXTEST, IN-TEST, or the preload portion of the SAMPLE/PRELOAD command.

When the TAP controller is placed in Capture-IR state, the two least significant bits of the instruction register are loaded with 01. When the controller is moved to the Shift-IR state the instruction is serially loaded through the TDI input (while the previous contents are shifted out at TDO). For all instructions, the TAP executes newly loaded instructions only when the controller is moved to Update-IR state. The TAP instruction sets for this device are listed in the following tables.

### EXTEST

EXTEST is an IEEE 1149.1 mandatory public instruction. It is to be executed whenever the instruction register is loaded with all 0s. EXTEST is not implemented in this device.

The TAP controller does recognize an all-0 instruction. When an EXTEST instruction is loaded into the instruction register, the device responds as if a SAMPLE/PRELOAD instruction has been loaded. There is one difference between two instructions. Unlike SAMPLE/PRELOAD instruction, EXTEST places the device outputs in a High-Z state.

### IDCODE

The IDCODE instruction causes a vendor-specific, 32-bit code to be loaded into the ID register when the controller is in Cap-ture-DR mode and places the ID register between the TDI and TDO pins in Shift-DR mode. The IDCODE instruction is the default instruction loaded in the instruction upon power-up and at any time the TAP controller is placed in the test-logic reset state.

### SAMPLE-Z

If the High-Z instruction is loaded in the instruction register, all output pins are forced to a High-Z state and the boundary scan register is connected between TDI and TDO pins when the TAP controller is in a Shift-DR state.

### SAMPLE/PRELOAD

SAMPLE/PRELOAD is an IEEE 1149.1 mandatory instruction. The PRELOAD portion of the command is not implemented in this device, so the device TAP controller is not fully IEEE 1149.1-compliant.

When the SAMPLE/PRELOAD instruction is loaded in the instruction register and the TAP controller is in the Capture-DR state, a snap shot of the data in the device's input and I/O buffers is loaded into the boundary scan register. Because the device system clock(s) are independent from the TAP Clock (TCK), it is possible for the TAP to attempt to capture the input and I/O ring contents while the buffers are in transition (i.e., in a metastable state). Although allowing the TAP to sample metastable inputs will not harm the device, repeatable results can not be expected. To guarantee that the boundary scan register will capture the correct value of a signal, the device input signals must be stabilized long enough to meet the TAP controller's capture set up plus hold time ($t_{CS}$ plus $t_{CH}$). The device clock input(s) need not be paused for any other TAP operation except capturing the input and I/O ring contents into the boundary scan register.

Moving the controller to Shift-DR state then places the boundary scan register between the TDI and TDO pins. Because the PRELOAD portion of the command is not implemented in this device, moving the controller to the Update-DR state with the SAMPLE/PRELOAD instruction loaded in the instruction register has the same effect as the Pause-DR command.

### BYPASS

When the BYPASS instruction is loaded in the instruction register and the TAP controller is in the Shift-DR state, the bypass register is placed between TDI and TDO. This allows the board level scan path to be shortened to facilitate testing of other devices in the scan path.

### Reserved

Do not use these instructions. They are reserved for future use.
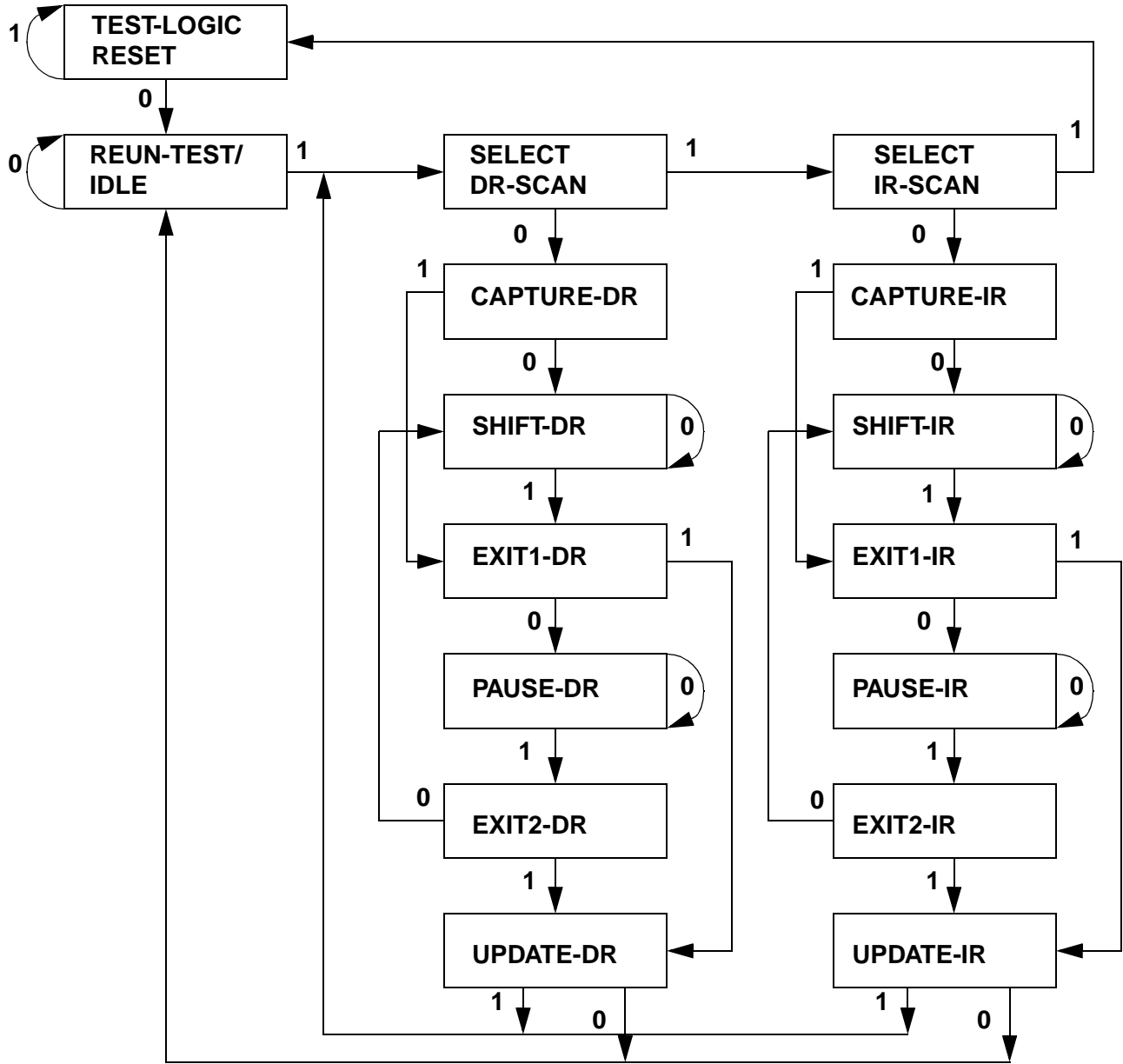
**Figure 1. TAP Controller State Diagram**[21]

**Note:**
21.  The 0/1 next to each state represents the value at TMS at the rising edge of TCK.
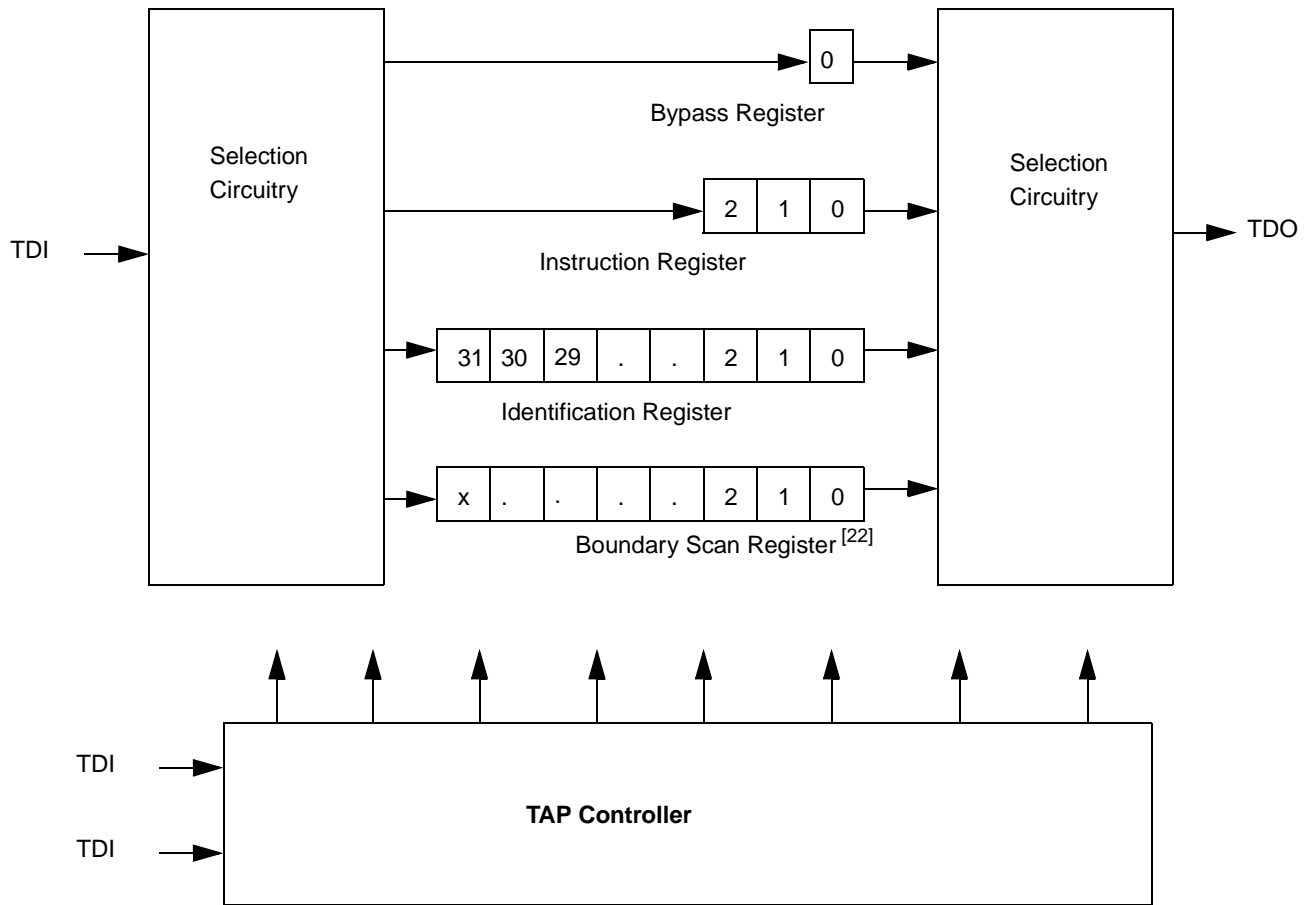
**Figure 2. TAP Controller Block Diagram**

## TAP Electrical Characteristics Over the Operating Range

| Parameter | Description | Test Conditions | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{IH}$ | Input High (Logic 1) Voltage[23, 24] | | 2.0 | $V_{CC}$ + 0.3 | V |
| $V_{Il}$ | Input Low (Logic 0) Voltage[23, 24] | | −0.3 | 0.8 | V |
| $IL_I$ | Input Leakage Current | $0V \leq V_{IN} \leq V_{CC}$ | −5.0 | 5.0 | µA |
| $IL_I$ | TMS and TDI Input Leakage Current | $0V \leq V_{IN} \leq V_{CC}$ | −30 | 30 | µA |
| $IL_O$ | Output Leakage Current | Output disabled, $0V \leq V_{IN} \leq V_{CCQ}$ | −5.0 | 5.0 | µA |
| $V_{OLC}$ | LVCMOS Output Low Voltage[23, 25] | $I_{OLC}$ = 100 µA | | 0.2 | V |
| $V_{OHC}$ | LVCMOS Output High Voltage[23, 25] | $I_{OHC}$ = 100 µA | $V_{CC}$ − 0.2 | | V |
| $V_{OLT}$ | LVTTL Output Low Voltage[23] | $I_{OLT}$ = 8.0 mA | | 0.4 | V |
| $V_{OHT}$ | LVTTL Output High Voltage[23] | $I_{OHT}$ = 8.0 mA | 2.4 | | V |

**Notes:**
22. X = 69 for the x36 configuration;
    X = 50 for the x18 configuration.
23. All Voltage referenced to $V_{SS}$ (GND).
24. Overshoot: $V_{IH}(AC) \leq V_{CC}+1.5V$ for $t \leq t_{KHKH}/2$, Undershoot: $V_{IL}(AC) \leq −0.5V$ for $t \leq t_{KHKH}/2$, Power-up: $V_{IH} \leq 3.6V$ and $V_{CC} \leq 3.135V$ and $V_{CCQ} \leq 1.4V$ for $t \leq 200$ ms. During normal operation, $V_{CCQ}$ must not exceed $V_{CC}$. Control input signals (such as R/$\overline{W}$, ADV/$\overline{LD}$, etc.) may not have pulse widths less than $t_{KHKL}$ (min.).
25. This parameter is sampled.

*PRELIMINARY*

**TAP AC Switching Characteristics** Over the Operating Range[26, 27]

| Parameter | Description | Min. | Max | Unit |
|---|---|---|---|---|
| **Clock** | | | | |
| $t_{THTH}$ | Clock Cycle Time | 20 | | ns |
| $f_{TF}$ | Clock Frequency | | 50 | MHz |
| $t_{THTL}$ | Clock HIGH Time | 8 | | ns |
| $t_{TLTH}$ | Clock LOW Time | 8 | | ns |
| **Output Times** | | | | |
| $t_{TLQX}$ | TCK LOW to TDO Unknown | 0 | | ns |
| $t_{TLQV}$ | TCK LOW to TDO Valid | | 10 | ns |
| $t_{DVTH}$ | TDI Valid to TCK HIGH | 5 | | ns |
| $t_{THDX}$ | TCK HIGH to TDI Invalid | 5 | | ns |
| **Set-up Times** | | | | |
| $t_{MVTH}$ | TMS Set-up | 5 | | ns |
| $t_{CS}$ | Capture Set-up | 5 | | ns |
| **Hold Times** | | | | |
| $t_{THMX}$ | TMS Hold | 5 | | ns |
| $t_{CH}$ | Capture Hold | 5 | | ns |

**Notes:**
26.  $t_{CS}$ and $t_{CH}$ refer to the set-up and hold time requirements of latching data from the boundary scan register.
27.  Test conditions are specified using the load in TAP AC test conditions.

**TAP Timing and Test Conditions**



(a)

(b)
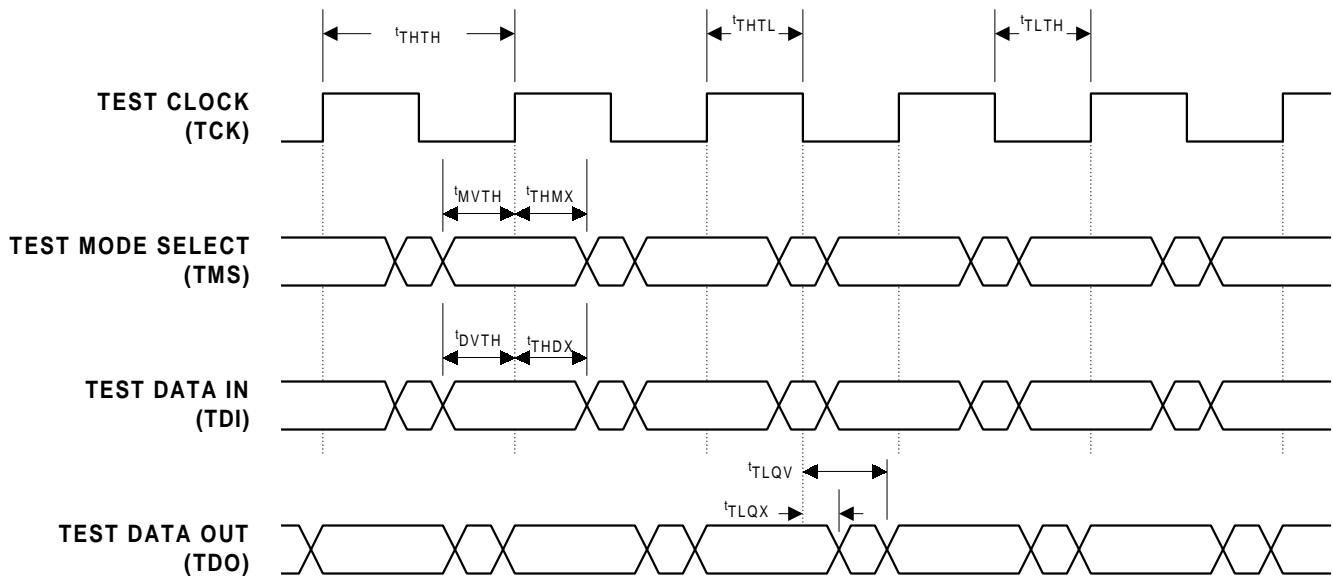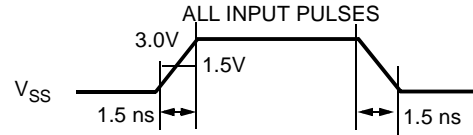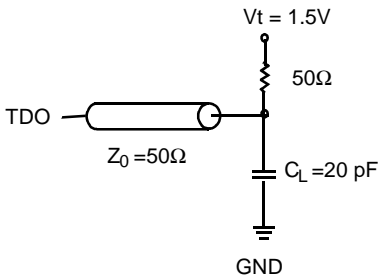
## Identification Register Definitions

| Instruction Field | 256K x 36 | 512K x 18 | Description |
|---|---|---|---|
| REVISION NUMBER (31:28) | XXXX | XXXX | Reserved for revision number. |
| DEVICE DEPTH (27:23) | 00110 | 00111 | Defines depth of 256K or 512K words. |
| DEVICE WIDTH (22:18) | 00100 | 00011 | Defines width of x36 or x18 bits. |
| RESERVED (17:12) | XXXXXX | XXXXXX | Reserved for future use. |
| CYPRESS JEDEC ID CODE (11:1) | 00011100100 | 00011100100 | Allows unique identification of DEVICE vendor. |
| ID Register Presence Indicator (0) | 1 | 1 | Indicates the presence of an ID register. |

## Scan Register Sizes

| Register Name | Bit Size (x36) | Bit Size (x18) |
|---|---|---|
| Instruction | 3 | 3 |
| Bypass | 1 | 1 |
| ID | 32 | 32 |
| Boundary Scan | 70 | 51 |

## Instruction Codes

| Instruction | Code | Description |
|---|---|---|
| EXTEST | 000 | Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all device outputs to High-Z state. This instruction is not IEEE 1149.1-compliant. |
| IDCODE | 001 | Preloads ID register with vendor ID code and places it between TDI and TDO. This instruction does not affect device operations. |
| SAMPLE-Z | 010 | Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all device outputs to High-Z state. |
| RESERVED | 011 | Do not use these instructions; they are reserved for future use. |
| SAMPLE/PRELOAD | 100 | Captures I/O ring contents. Places the boundary scan register between TDI and TDO. This instruction does not affect device operations. This instruction does not implement IEEE 1149.1 PRELOAD function and is therefore not 1149.1-compliant. |
| RESERVED | 101 | Do not use these instructions; they are reserved for future use. |
| RESERVED | 110 | Do not use these instructions; they are reserved for future use. |
| BYPASS | 111 | Places the bypass register between TDI and TDO. This instruction does not affect device operations. |

## Boundary Scan Order (256K x 36)

| Bit# | Signal Name | TQFP | Bump ID |
|------|-------------|------|---------|
| 1 | SA | 44 | 2R |
| 2 | SA | 45 | 3T |
| 3 | SA | 46 | 4T |
| 4 | SA | 47 | 5T |
| 5 | SA | 48 | 6R |
| 6 | SA | 49 | 3B |
| 7 | SA | 50 | 5B |
| 8 | DQa | 51 | 6P |
| 9 | DQa | 52 | 7N |
| 10 | DQa | 53 | 6M |
| 11 | DQa | 56 | 7L |
| 12 | DQa | 57 | 6K |
| 13 | DQa | 58 | 7P |
| 14 | DQa | 59 | 6N |
| 15 | DQa | 62 | 6L |
| 16 | DQa | 63 | 7K |
| 17 | ZZ | 64 | 7T |
| 18 | DQb | 68 | 6H |
| 19 | DQb | 69 | 7G |
| 20 | DQb | 72 | 6F |
| 21 | DQb | 73 | 7E |
| 22 | DQb | 74 | 6D |
| 23 | DQb | 75 | 7H |
| 24 | DQb | 78 | 6G |
| 25 | DQb | 79 | 6E |
| 26 | DQb | 80 | 7D |
| 27 | SA | 81 | 6A |
| 28 | SA | 82 | 5A |
| 29 | SA | 83 | 4G |
| 30 | NC | 84 | 4A |
| 31 | ADV/$\overline{\text{LD}}$ | 85 | 4B |
| 32 | $\overline{\text{OE}}$ | 86 | 4F |
| 33 | $\overline{\text{CKE}}$ | 87 | 4M |
| 34 | R/$\overline{\text{W}}$ | 88 | 4H |
| 35 | CLK | 89 | 4K |

## Boundary Scan Order (256K x 36) (continued)

| Bit# | Signal Name | TQFP | Bump ID |
|------|-------------|------|---------|
| 36 | $\overline{\text{CE}}_2$ | 92 | 6B |
| 37 | $\overline{\text{BWa}}$ | 93 | 5L |
| 38 | $\overline{\text{BWb}}$ | 94 | 5G |
| 39 | $\overline{\text{BWc}}$ | 95 | 3G |
| 40 | $\overline{\text{BWd}}$ | 96 | 3L |
| 41 | CE$_2$ | 97 | 2B |
| 42 | $\overline{\text{CE}}$ | 98 | 4E |
| 43 | SA | 99 | 3A |
| 44 | SA | 100 | 2A |
| 45 | DQc | 1 | 2D |
| 46 | DQc | 2 | 1E |
| 47 | DQc | 3 | 2F |
| 48 | DQc | 6 | 1G |
| 49 | DQc | 7 | 2H |
| 50 | DQc | 8 | 1D |
| 51 | DQc | 9 | 2E |
| 52 | DQc | 12 | 2G |
| 53 | DQc | 13 | 1H |
| 54 | NC | 14 | 5R |
| 55 | DQd | 18 | 2K |
| 56 | DQd | 19 | 1L |
| 57 | DQd | 22 | 2M |
| 58 | DQd | 23 | 1N |
| 59 | DQd | 24 | 2P |
| 60 | DQd | 25 | 1K |
| 61 | DQd | 28 | 2L |
| 62 | DQd | 29 | 2N |
| 63 | DQd | 30 | 1P |
| 64 | MODE | 31 | 3R |
| 65 | SA | 32 | 2C |
| 66 | SA | 33 | 3C |
| 67 | SA | 34 | 5C |
| 68 | SA | 35 | 6C |
| 69 | SA1 | 36 | 4N |
| 70 | SA0 | 37 | 4P |

## Boundary Scan Order (512K x 18)

| Bit# | Signal Name | TQFP | Bump ID |
|---|---|---|---|
| 1 | SA | 44 | 2R |
| 2 | SA | 45 | 2T |
| 3 | SA | 46 | 3T |
| 4 | SA | 47 | 5T |
| 5 | SA | 48 | 6R |
| 6 | SA | 49 | 3B |
| 7 | SA | 50 | 5B |
| 8 | DQa | 58 | 7P |
| 9 | DQa | 59 | 6N |
| 10 | DQa | 62 | 6L |
| 11 | DQa | 63 | 7K |
| 12 | ZZ | 64 | 7T |
| 13 | DQa | 68 | 6H |
| 14 | DQa | 69 | 7G |
| 15 | DQa | 72 | 6F |
| 16 | DQa | 73 | 7E |
| 17 | DQa | 74 | 6D |
| 18 | SA | 80 | 6T |
| 19 | SA | 81 | 6A |
| 20 | SA | 82 | 5A |
| 21 | SA | 83 | 4G |
| 22 | NC | 84 | 4A |
| 23 | ADV/$\overline{LD}$ | 85 | 4B |
| 24 | $\overline{OE}$ | 86 | 4F |
| 25 | $\overline{CKE}$ | 87 | 4M |
| 26 | R/$\overline{W}$ | 88 | 4H |

## Boundary Scan Order (512K x 18) (continued)

| Bit# | Signal Name | TQFP | Bump ID |
|---|---|---|---|
| 27 | CLK | 89 | 4K |
| 28 | $\overline{CE2}$ | 92 | 6B |
| 29 | $\overline{BWa}$ | 93 | 5L |
| 30 | $\overline{BWb}$ | 94 | 3G |
| 31 | CE2 | 97 | 2B |
| 32 | $\overline{CE}$ | 98 | 4E |
| 33 | SA | 99 | 3A |
| 34 | SA | 100 | 2A |
| 35 | DQb | 8 | 1D |
| 36 | DQb | 9 | 2E |
| 37 | DQb | 12 | 2G |
| 38 | DQb | 13 | 1H |
| 39 | NC | 14 | 5R |
| 40 | DQb | 18 | 2K |
| 41 | DQb | 19 | 1L |
| 42 | DQb | 22 | 2M |
| 43 | DQb | 23 | 1N |
| 44 | DQb | 24 | 2P |
| 45 | MODE | 31 | 3R |
| 46 | SA | 32 | 2C |
| 47 | SA | 33 | 3C |
| 48 | SA | 34 | 5C |
| 49 | SA | 35 | 6C |
| 50 | SA1 | 36 | 4N |
| 51 | SA0 | 37 | 4P |

## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Voltage on $V_{CC}$ Supply Relative to $V_{SS}$ ......... –0.5V to +4.6V

$V_{IN}$ ........................................................–0.5V to $V_{CC}$+0.5V

Storage Temperature (plastic) ......................–55°C to +125°

Junction Temperature ...................................+125°

Power Dissipation ........................................2.0W

Short Circuit Output Current ...................................... 50 mA

## Operating Range

| Range | Ambient Temperature[11] | $V_{CC}/V_{CCQ}$ |
|---|---|---|
| Com'l | 0°C to +70°C | 3.3V ± 5% |
| Ind'l | -40°C to +85°C | |

## Electrical Characteristics Over the Operating Range

| Parameter | Description | Test Conditions | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{IHD}$ | Input High (Logic 1) Voltage[23, 29] | Data Inputs (DQxx) | 2.0 | $V_{CC}$+0.3 | V |
| $V_{IH}$ | | All Other Inputs | 2.0 | 4.6 | V |
| $V_{Il}$ | Input Low (Logic 0) Voltage[23, 29] | | –0.5 | 0.8 | V |
| $IL_I$ | Input Leakage Current | $0V \leq V_{IN} \leq V_{CC}$ | - | 5 | µA |
| $IL_I$ | MODE and ZZ Input Leakage Current[30] | $0V \leq V_{IN} \leq V_{CC}$ | - | 30 | µA |
| $IL_O$ | Output Leakage Current | Output(s) disabled, $0V \leq V_{OUT} \leq V_{CC}$ | - | 5 | µA |
| $V_{OH}$ | Output High Voltage[23] | $I_{OH}$ = –5.0 mA for 3.3V I/O | 2.4 | | V |
| | | $I_{OH}$ = –1.0 mA for 2.5V I/O | 2.0 | | V |
| $V_{OL}$ | Output Low Voltage[23] | $I_{OL}$ = 8.0 mA | | 0.4 | V |
| $V_{CC}$ | Supply Voltage[23] | | 3.135 | 3.465 | V |
| $V_{CCQ}$ | I/O Supply Voltage[23] | 3.3V I/O | 3.135 | 3.465 | V |
| | | 2.5V I/O | 2.4 | 2.9 | V |

| Parameter | Description | Conditions | Typ. | 133 MHz/ -6.5 | 117 MHz/ -7 | 100 MHz/ -7.5 | 100 MHz/ -8 | Unit |
|---|---|---|---|---|---|---|---|---|
| $I_{CC}$ | Power Supply Current: Operating[31, 32, 33, 34] | Device selected; all inputs $\leq V_{IL}$ or $\geq V_{IH}$; cycle time $\geq t_{KC}$ min.; $V_{CC}$ =Max.; outputs open, ADV/$\overline{LD}$ = X, f = $f_{MAX}^2$ | 150 | 410 | 385 | 350 | 350 | mA |
| $I_{SB2}$ | CMOS Standby[32, 33, 34] | Device deselected; $V_{CC}$ = Max.; all inputs $\leq V_{SS}$ + 0.2 or $\geq V_{CC}$ – 0.2; all inputs static; CLK frequency = 0 | 5 | 30 | 30 | 30 | 30 | mA |
| $I_{SB3}$ | TTL Standby[32, 33, 34] | Device deselected; all inputs $\leq V_{IL}$ or $\geq V_{IH}$; all inputs static; $V_{CC}$ = MAX; CLK frequency = 0 | 15 | 50 | 50 | 50 | 50 | mA |
| $I_{SB4}$ | Clock Running[32, 33, 34] | Device deselected; all inputs $\leq V_{IL}$ or $\geq V_{IH}$; $V_{CC}$ = MAX; CLK cycle time $\geq t_{KC}$ Min. | 40 | 190 | 180 | 170 | 170 | mA |

## Capacitance[25]

| Parameter | Description | Test Conditions | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $C_I$ | Input Capacitance | $T_A$ = 25°C, f = 1 MHz, $V_{CC}$ = 3.3V | 4 | 4 | pF |
| $C_O$ | Input/Output Capacitance DQ | | 7 | 6.5 | pF |

**Notes:**
28. $T_A$ is the case temperature.
29. Overshoot: $V_{IH} \leq$ +6.0V for t $\leq t_{KC}$ /2
    Undershoot:$V_{IL} \leq$ -2.0V for t $\leq t_{KC}$ /2.
30. MODE pin has an internal pull-up and ZZ pin has an internal pull-down. These two pins exhibit an input leakage current of ±50 µA.
31. $I_{CC}$ is given with no output current. $I_{CC}$ increases with greater output loading and faster cycle times.
32. "Device Deselected" means the device is in Power-Down mode as defined in the truth table. "Device Selected" means the device is active.
33. Typical values are measured at 3.3V, 25°C, and 20 ns cycle time.
34. At f = $f_{MAX}$, inputs are cycling at the maximum frequency of read cycles of 1/$t_{CYC}$; f = 0 means no input lines are changing.
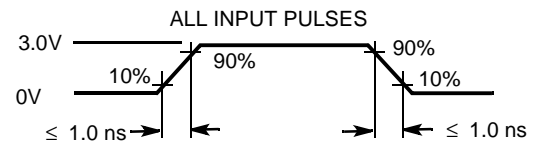
**Thermal Resistance**

| Description | Test Conditions | Symbol | TQFP Typ. | Units |
|---|---|---|---|---|
| Thermal Resistance (Junction to Ambient) | Still Air, soldered on a 4.25 x 1.125 inch, 4-layer PCB | $\Theta_{JA}$ | 25 | °C/W |
| Thermal Resistance (Junction to Case) | | $\Theta_{JC}$ | 9 | °C/W |

**AC Test Loads and Waveforms for 3.3V I/O**
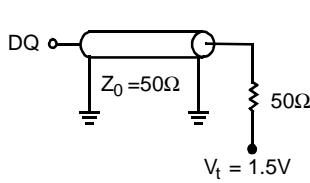


(a)
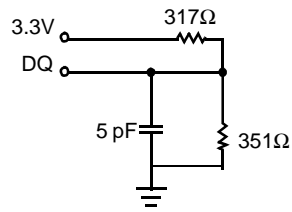
(b)

(c)

**AC Test Loads and Waveforms for 2.5V I/O**



(a)

(c)
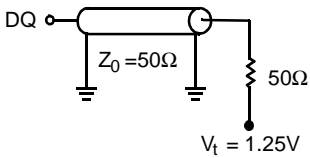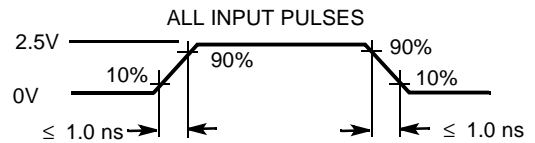
## Switching Characteristics Over the Operating Range[35]

| Parameter | Description | -6.5 133-MHz Min. | -6.5 133-MHz Max. | -7 117 MHz Min. | -7 117 MHz Max. | -7.5 100 MHz Min. | -7.5 100 MHz Max. | -8 100 MHz Min. | -8 100 MHz Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| **Clock** | | | | | | | | | | |
| $t_{KC}$ | Clock Cycle Time | 7.5 | | 8.5 | | 10 | | 10 | | ns |
| $t_{KH}$ | Clock HIGH Time | 2.5 | | 3.0 | | 3.5 | | 3.5 | | ns |
| $t_{KL}$ | Clock LOW Time | 2.5 | | 3.0 | | 3.5 | | 3.5 | | ns |
| **Output Times** | | | | | | | | | | |
| $t_{KQ}$ | Clock to Output Valid | | 6.5 | | 7.0 | | 7.5 | | 8.0 | ns |
| $t_{KQX}$ | Clock to Output Invalid | 2.0 | | 2.0 | | 2.0 | | 2.0 | | ns |
| $t_{KQLZ}$ | Clock to Output in Low-Z[25, 36, 37] | 3.0 | | 3.0 | | 3.0 | | 3.0 | | ns |
| $t_{KQHZ}$ | Clock to Output in High-Z[25, 36, 37] | 2 | 3.5 | 2 | 3.5 | 2 | 3.5 | 2 | 3.5 | ns |
| $t_{OEQ}$ | OE to Output Valid | | 3.5 | | 3.5 | | 4.0 | | 4.0 | ns |
| $t_{OELZ}$ | OE to Output in Low-Z[25, 36, 37] | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{OEHZ}$ | OE to Output in High-Z[25, 36, 37] | | 3.5 | | 3.5 | | 3.5 | | 3.5 | ns |
| **Set-up Times** | | | | | | | | | | |
| $t_S$ | Address and Controls[38] | 1.5 | | 1.5 | | 1.8 | | 2.0 | | ns |
| $t_{SD}$ | Data In[38] | 1.5 | | 1.5 | | 1.8 | | 2.0 | | ns |
| **Hold Times** | | | | | | | | | | |
| $t_H$ | Address and Controls[38] | 0.5 | | 0.5 | | 0.5 | | 0.5 | | ns |
| $t_{HD}$ | Data In[38] | 0.5 | | 0.5 | | 0.5 | | 0.5 | | ns |

**Notes:**
35. Test conditions as specified with the output loading as shown in part (a) of AC Test Loads unless otherwise noted.
36. Output loading is specified with $C_L$=5 pF as in part (a) of AC Test Loads.
37. At any given temperature and voltage condition, $t_{KQHZ}$ is less than $t_{KQLZ}$ and $t_{OEHZ}$ is less than $t_{OELZ}$.
38. This is a synchronous device. All synchronous inputs must meet specified setup and hold time, except for "don't care" as defined in the truth table.
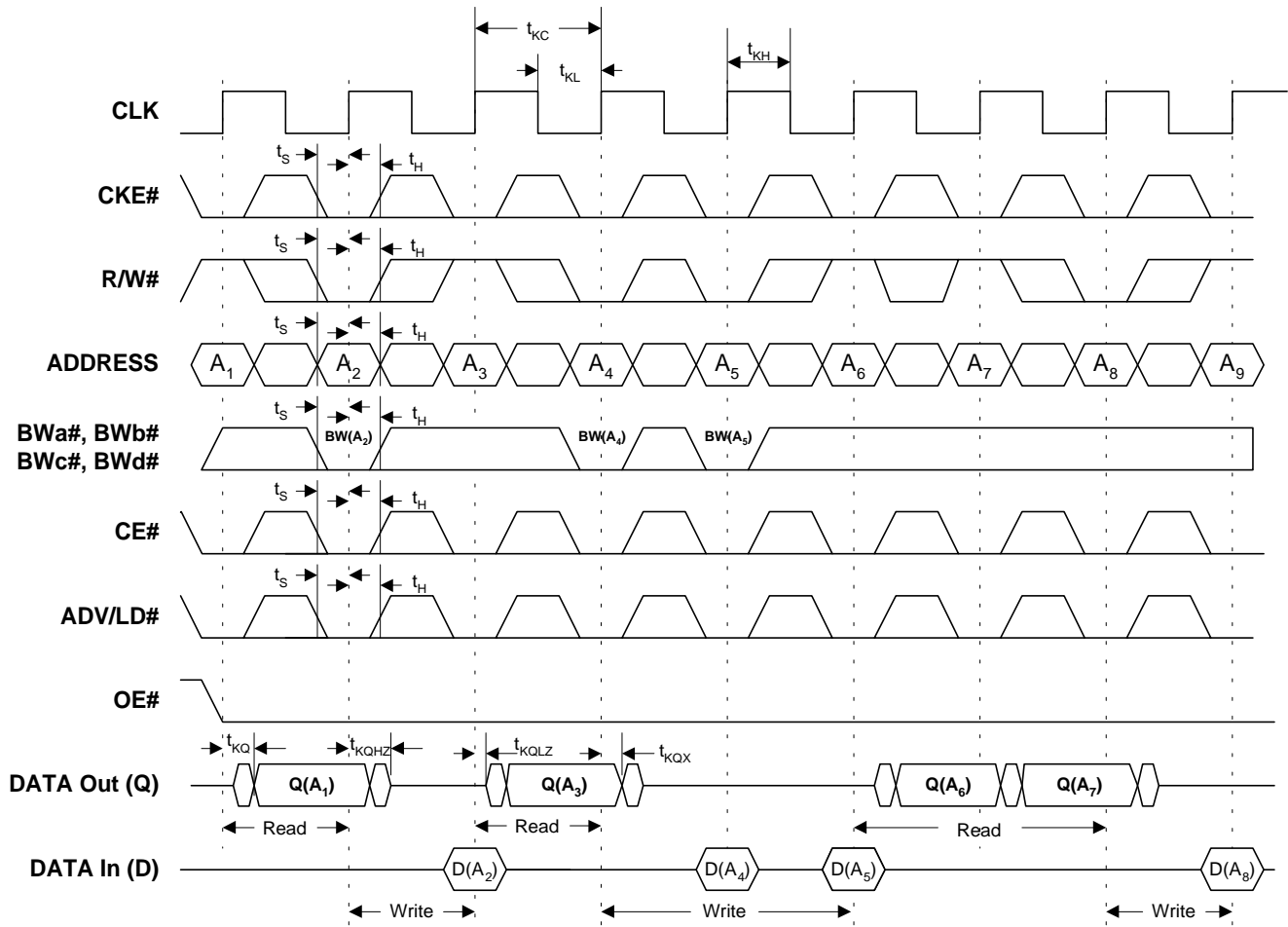
## Switching Waveforms

**Read Timing**[39, 40, 41, 42, 43]
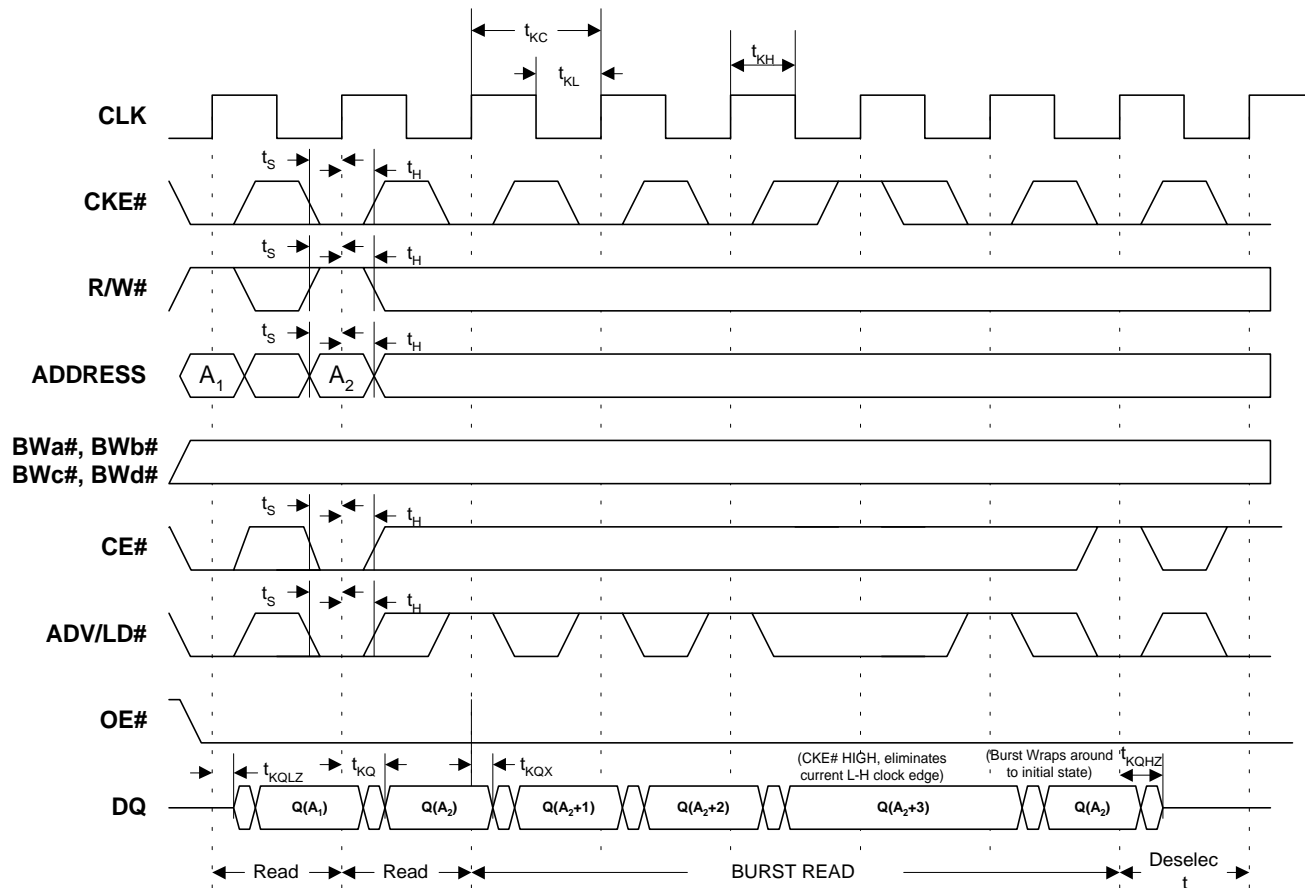


**Notes:**

39. $Q(A_1)$ represents the first output from the external address $A_1$. $Q(A_2)$ represents the first output from the external address $A_2$; $Q(A_2+1)$ represents the next output data in the burst sequence of the base address $A_2$, etc. where address bits SA0 and SA1 are advancing for the four word burst in the sequence defined by the state of the MODE input.
40. $\overline{CE}_2$ timing transitions are identical to the $\overline{CE}$ signal. For example, when $\overline{CE}$ is LOW on this waveform, $\overline{CE}_2$ is LOW. CE_2 timing transitions are identical but inverted to the $\overline{CE}$ signal. For example, when $\overline{CE}$ is LOW on this waveform, CE_2 is HIGH.
41. Burst ends when new address and control are loaded into the SRAM by sampling ADV/$\overline{LD}$ LOW.
42. R/$\overline{W}$ is "Don't Care" when the SRAM is bursting (ADV/$\overline{LD}$ sampled HIGH). The nature of the burst access (Read or Write) is fixed by the state of the R/$\overline{W}$ signal when new address and control are loaded into the SRAM.
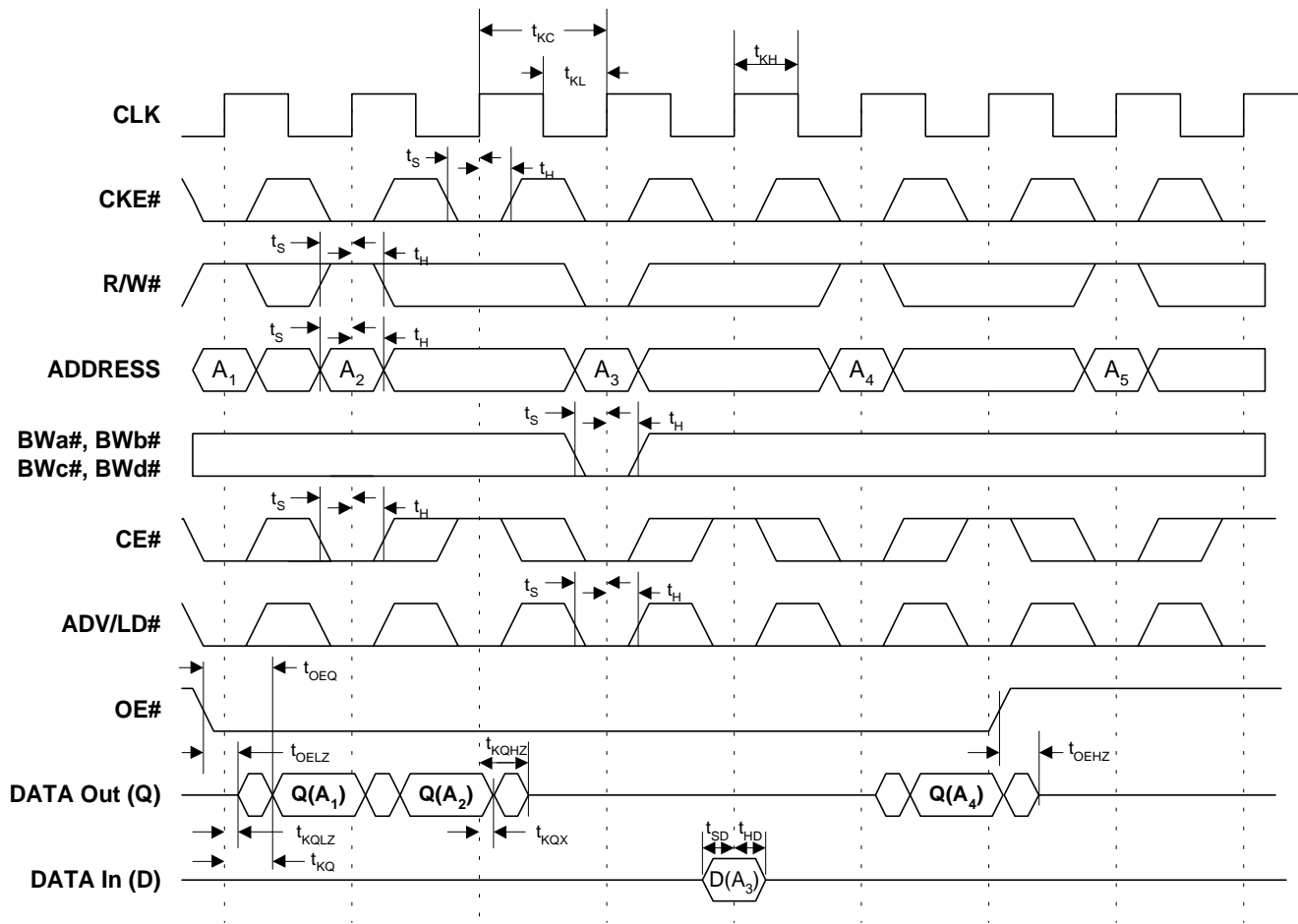43. $\overline{BW}c$ and $\overline{BW}d$ apply to 256Kx36 device only.

## Switching Waveforms (continued)

**Write Timing**[40, 41, 42, 43, 44, 45]
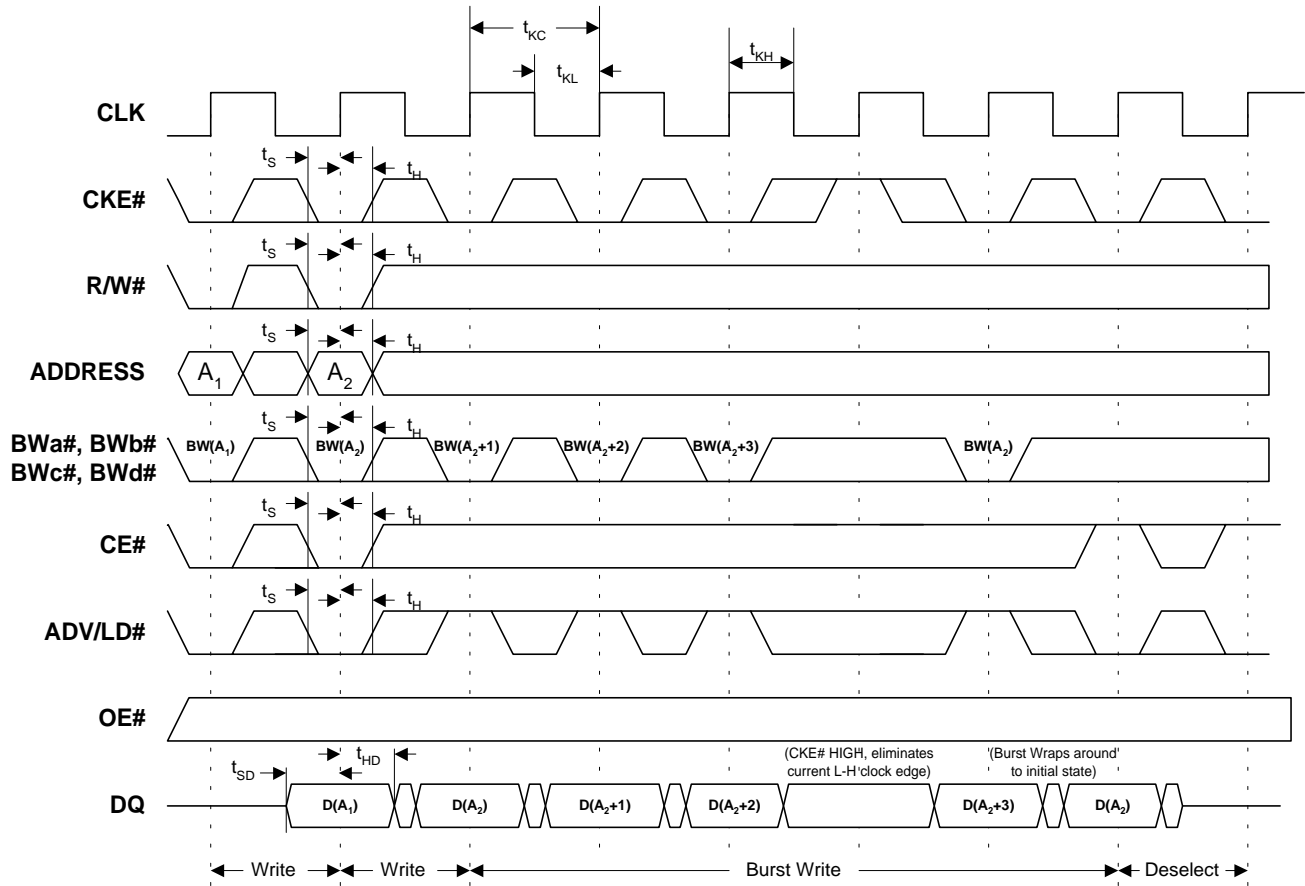


**Notes:**

44. $D(A_1)$ represents the first input to the external address A1. $D(A_2)$ represents the first input to the external address $A_2$; $D(A_2+1)$ represents the next input data in the burst sequence of the base address $A_2$, etc. where address bits SA0 and SA1 are advancing for the four word burst in the sequence defined by the state of the MODE input.

45. Individual Byte Write signals ($\overline{BWx}$) must be valid on all write and burst-write cycles. A write cycle is initiated when R/$\overline{W}$ signal is sampled LOW when ADV/$\overline{LD}$ is sampled LOW. The byte write information comes in one cycle before the actual data is presented to the SRAM.

*PRELIMINARY*

## Switching Waveforms (continued)

**Read/Write Timing**[40, 43, 45, 46]



**Note:**
46. $Q(A_1)$ represents the first output from the external address $A_1$. $D(A_2)$ represents the input data to the SRAM corresponding to address $A_2$.

## Switching Waveforms (continued)

$\overline{\text{CKE}}$ **Timing**[40, 43, 45, 46, 47]



**Note:**
47. $\overline{\text{CKE}}$ when sampled HIGH on the rising edge of clock will block that L-H transition of the clock from propagating into the SRAM. The part will behave as if the L-H clock transition did not occur. All internal register in the SRAM will retain their previous state.

*PRELIMINARY*

## Switching Waveforms (continued)

$\overline{CE}$ Timing[40, 43, 45, 48, 49]



**Notes:**
48. $Q(A_1)$ represents the first output from the external address $A_1$. $D(A_3)$ represents the input data to the SRAM corresponding to address $A_3$, etc.
49. When either one of the Chip enables ($\overline{CE}$, $CE_2$ or $\overline{CE}_2$) is sampled inactive at the rising clock edge, a chip deselect cycle is initiated. The data-bus High-Z one cycle after the initiation of the deselect cycle. This allows for any pending data transfers (reads or writes) to be completed.

**Ordering Information**

| Speed (MHz) | Ordering Code | Package Name | Package Type | Operating Range |
|---|---|---|---|---|
| 133 | CY7C1355A-133AC/ GVT71256ZB36-6.5 | A101 | 100-Lead 14 x 20 x 1.4 mm Thin Quad Flat Pack | Commercial |
| | CY7C1355A-133BGC/ GVT71256ZB36B-6.5 | BG119 | 119-Lead BGA (14 x 22 x 2.4 mm) | Commercial |
| 117 | CY7C1355A-117AC/ GVT71256ZB36-7 | A101 | 100-Lead 14 x 20 x 1.4 mm Thin Quad Flat Pack | Commercial |
| | CY7C1355A-117AI/ GVT71256ZB36-7I | A101 | 100-Lead 14 x 20 x 1.4 mm Thin Quad Flat Pack | Industrial |
| | CY7C1355A-117BGC/ GVT71256ZB36B-7 | BG119 | 119-Lead BGA (14 x 22 x 2.4 mm) | Commercial |
| | CY7C1355A-117BGI/ GVT71256ZB36B-7I | BG119 | 119-Lead BGA (14 x 22 x 2.4 mm) | Industrial |
| 100 | CY7C1355A-100AC/ GVT71256ZB36-7.5 | A101 | 100-Lead 14 x 20 x 1.4 mm Thin Quad Flat Pack | Commercial |
| | CY7C1355A-100AI/ GVT71256ZB36-7.5I | A101 | 100-Lead 14 x 20 x 1.4 mm Thin Quad Flat Pack | Industrial |
| | CY7C1355A-100BGC/ GVT71256ZB36B-7.5 | BG119 | 119-Lead BGA (14 x 22 x 2.4 mm) | Commercial |
| | CY7C1355A-100BGI/ GVT71256ZB36B-7.5I | BG119 | 119-Lead BGA (14 x 22 x 2.4 mm) | Industrial |
| | CY7C1355A1-100AC | A101 | 100-Lead 14 x 20 x 1.4 mm Thin Quad Flat Pack | Commercial |
| | CY7C1355A1-100AI | A101 | 100-Lead 14 x 20 x 1.4 mm Thin Quad Flat Pack | Industrial |
| | CY7C1355A1-100BGC | BG119 | 119-Lead BGA (14 x 22 x 2.4 mm) | Commercial |
| | CY7C1355A1-100BGI | BG119 | 119-Lead BGA (14 x 22 x 2.4 mm) | Industrial |

## Ordering Information

| Speed (MHz) | Ordering Code | Package Name | Package Type | Operating Range |
|---|---|---|---|---|
| 133 | CY7C1357A-133AC/ GVT71512ZB36-6.5 | A101 | 100-Lead 14 x 20 x 1.4 mm Thin Quad Flat Pack | Commercial |
| | CY7C1357A-133BGC/ GVT71512ZB36B-6.5 | BG119 | 119-Lead BGA (14 x 22 x 2.4 mm) | Commercial |
| 117 | CY7C1357A-117AC/ GVT71512ZB36-7 | A101 | 100-Lead 14 x 20 x 1.4 mm Thin Quad Flat Pack | Commercial |
| | CY7C1357A-117AI/ GVT71512ZB36-7I | A101 | 100-Lead 14 x 20 x 1.4 mm Thin Quad Flat Pack | Industrial |
| | CY7C1357A-117BGC/ GVT71512ZB36B-7 | BG119 | 119-Lead BGA (14 x 22 x 2.4 mm) | Commercial |
| | CY7C1357A-117BGI/ GVT71512ZB36B-7I | BG119 | 119-Lead BGA (14 x 22 x 2.4 mm) | Industrial |
| 100 | CY7C1357A-100AC/ GVT71512ZB36-7.5 | A101 | 100-Lead 14 x 20 x 1.4 mm Thin Quad Flat Pack | Commercial |
| | CY7C1357A-100AI/ GVT71512ZB36-7.5I | A101 | 100-Lead 14 x 20 x 1.4 mm Thin Quad Flat Pack | Industrial |
| | CY7C1357A-100BGC/ GVT71512ZB36B-7.5 | BG119 | 119-Lead BGA (14 x 22 x 2.4 mm) | Commercial |
| | CY7C1357A-100BGI/ GVT71512ZB36B-7.5I | BG119 | 119-Lead BGA (14 x 22 x 2.4 mm) | Industrial |
| | CY7C1357A1-100AC | A101 | 100-Lead 14 x 20 x 1.4 mm Thin Quad Flat Pack | Commercial |
| | CY7C1357A1-100AI | A101 | 100-Lead 14 x 20 x 1.4 mm Thin Quad Flat Pack | Industrial |
| | CY7C1357A1-100BGC | BG119 | 119-Lead BGA (14 x 22 x 2.4 mm) | Commercial |
| | CY7C1357A1-100BGI | BG119 | 119-Lead BGA (14 x 22 x 2.4 mm) | Industrial |

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## Package Diagrams

**100-Pin Thin Plastic Quad Flatpack (14 x 20 x 1.4 mm) A101**
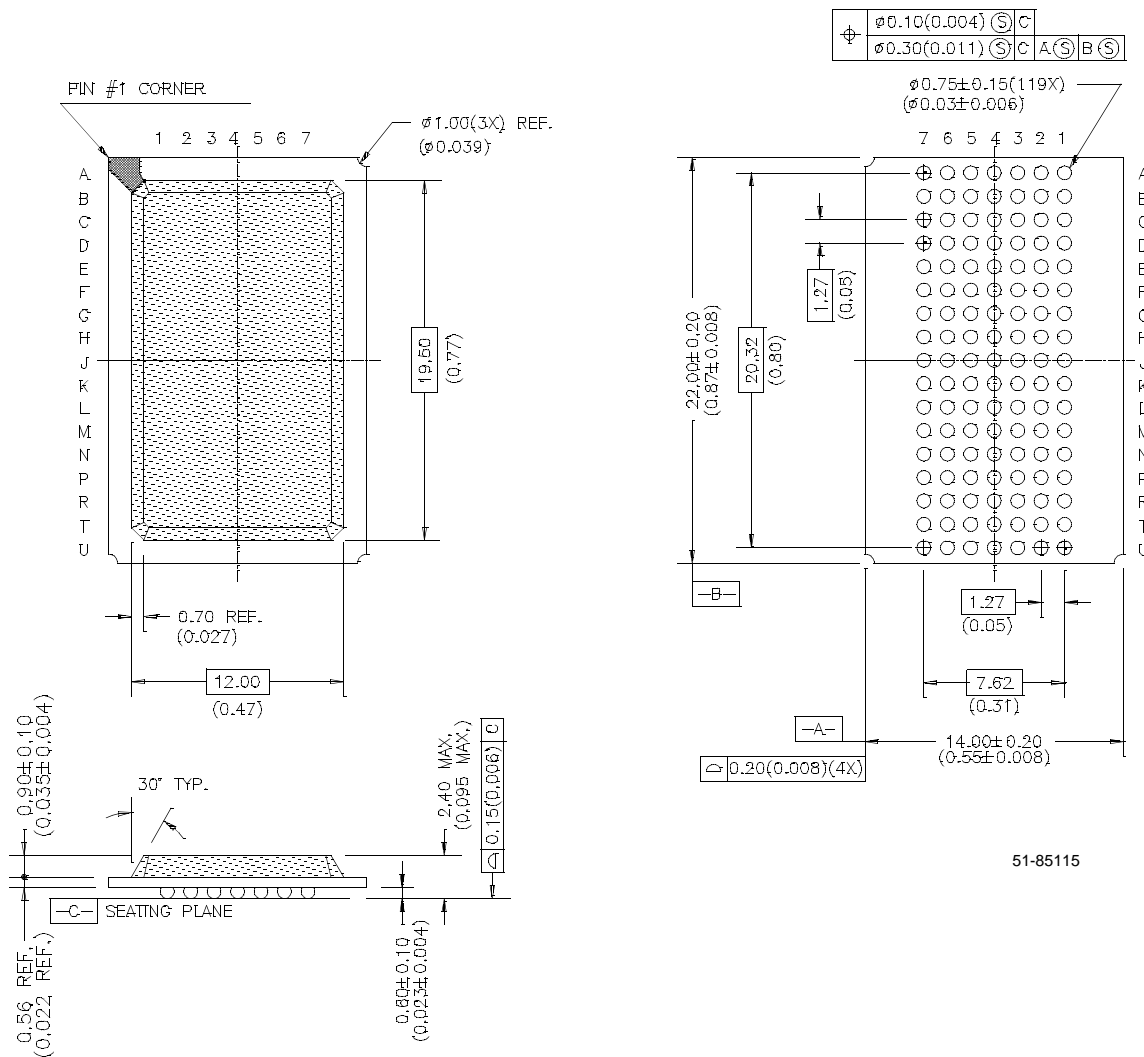
DIMENSIONS ARE IN MILLIMETERS.
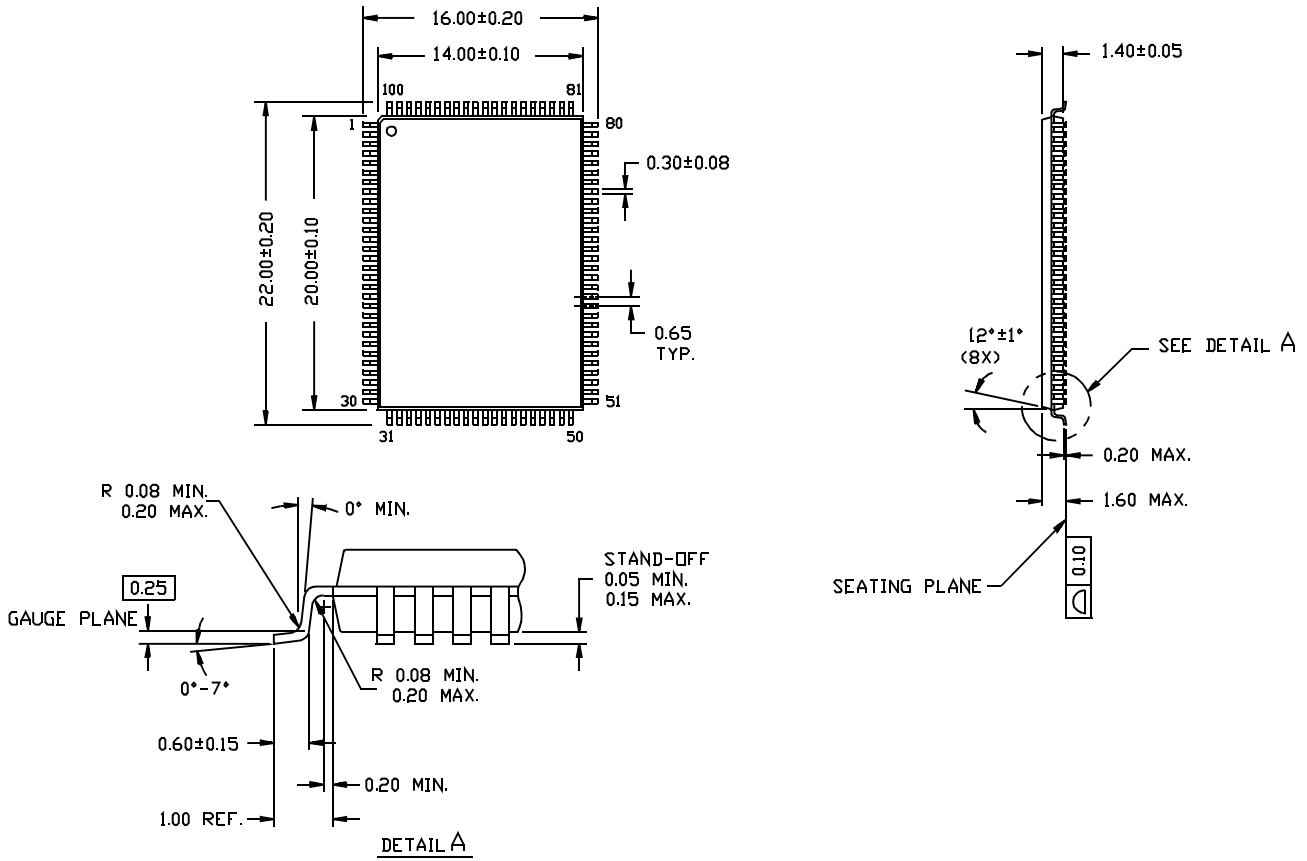


51-85050-A

## Package Diagrams (continued)

**119-Lead BGA (14 x 22 x 2.4 mm) BG119**



DIMENSION IN MILLIMETERS (INCHES)

51-85115