



**512K x 8 MoBL Static RAM**

**Features**

- **Low voltage range:**  
— 2.7V–3.6V
- **Ultra low active power**
- **Low standby power**
- **TTL-compatible inputs and outputs**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**

**Functional Description**

The CY62148V is a high-performance CMOS static RAM organized as 524,288 words by 8 bits. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL™) in portable applications such as cellular telephones. The device also has an automatic power-down feature that significantly reduces power consumption by 99% when addresses are not toggling.

The device can be put into standby mode when deselected ( $\overline{CE}$  HIGH).

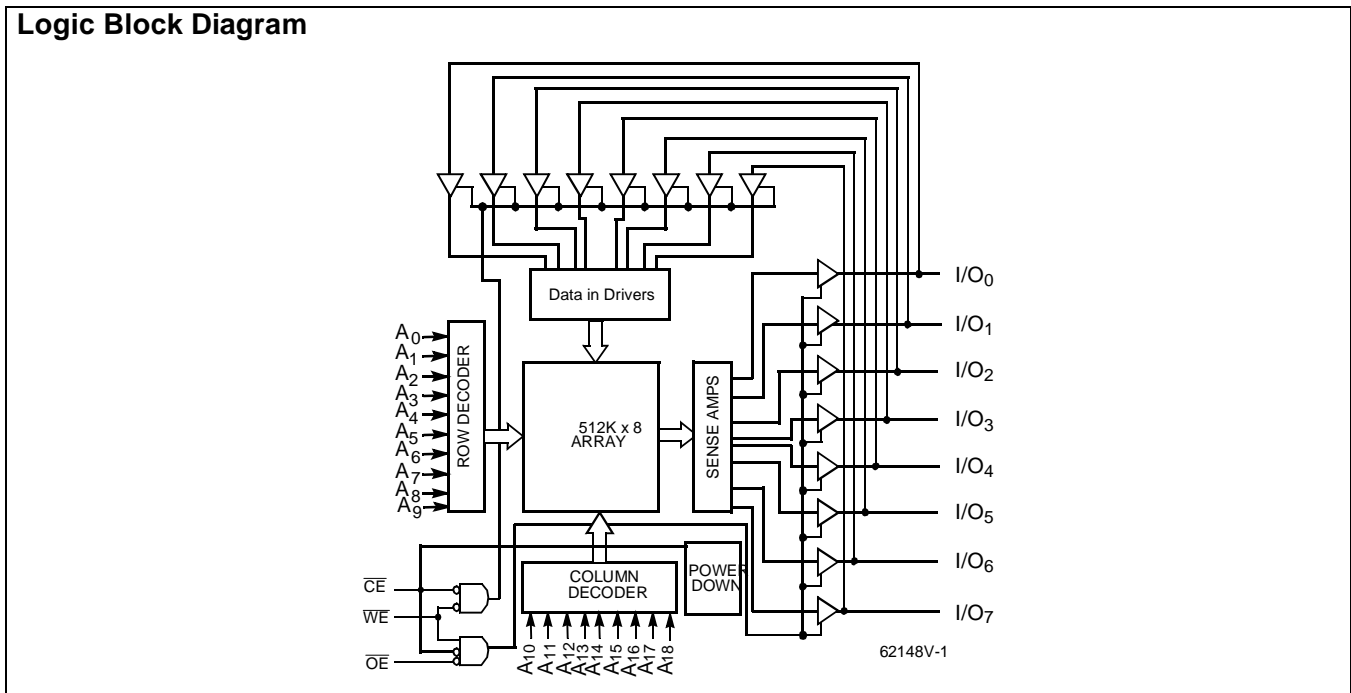
Writing to the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Write Enable ( $\overline{WE}$ ) inputs LOW. Data on the eight I/O pins ( $I/O_0$  through  $I/O_7$ ) is then written into the location specified on the address pins ( $A_0$  through  $A_{18}$ ).

Reading from the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Output Enable ( $\overline{OE}$ ) LOW while forcing Write Enable ( $\overline{WE}$ ) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

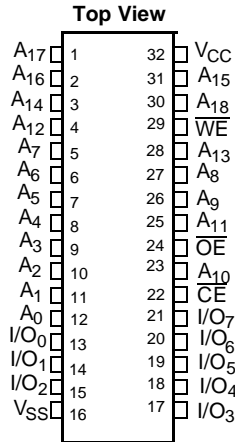
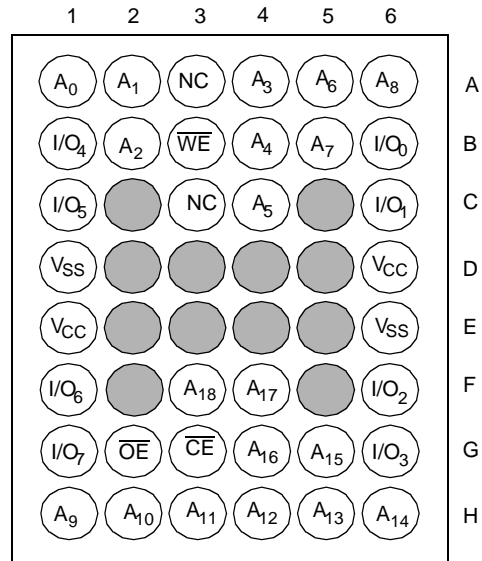
The eight input/output pins ( $I/O_0$  through  $I/O_7$ ) are placed in a high-impedance state when the device is deselected ( $\overline{CE}$  HIGH), the outputs are disabled ( $\overline{OE}$  HIGH), or during a write operation ( $\overline{CE}$  LOW and  $\overline{WE}$  LOW).

The CY62148V is available in a 36-ball FBGA, 32 pin TSOPII, and a 32-pin SOIC package.

**Logic Block Diagram**



## Pin Configurations

**TSOPII/SOIC**

**FBGA  
Top View**


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## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C

Ambient Temperature with

Power Applied ..... 55°C to +125°C

Supply Voltage to Ground Potential ..... -0.5V to +4.6V

DC Voltage Applied to Outputs  
in High Z State<sup>[1]</sup> ..... -0.5V to V<sub>CC</sub> + 0.5V

DC Input Voltage<sup>[1]</sup> ..... -0.5V to V<sub>CC</sub> + 0.5V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V  
(per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

## Operating Range

Range	Ambient Temperature	V <sub>CC</sub>
Industrial	-40°C to +85°C	2.7V to 3.6V

## Product Portfolio

Product	V <sub>CC</sub> Range			Speed	Power Dissipation (Industrial)			
					Operating (I <sub>CC</sub> )		Standby (I <sub>SB2</sub> )	
	Min.	Typ. <sup>[2]</sup>	Max.		Typ. <sup>[2]</sup>	Maximum	Typ. <sup>[2]</sup>	Maximum
CY62148V	2.7V	3.0V	3.6V	70 ns	7	15 mA	2 μA	20 μA

### Notes:

1. V<sub>IL(min.)</sub> = -2.0V for pulse durations less than 20 ns.

2. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC(typ.)</sub>, T<sub>A</sub> = 25°C.

**Electrical Characteristics** Over the Operating Range

Parameter	Description	Test Conditions		CY62148V			Unit
				Min.	Typ. <sup>[2]</sup>	Max.	
V <sub>OH</sub>	Output HIGH Voltage	I <sub>OH</sub> = -1.0 mA	V <sub>CC</sub> = 2.7V	2.4			V
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> = 2.1 mA	V <sub>CC</sub> = 2.7V			0.4	V
V <sub>IH</sub>	Input HIGH Voltage		V <sub>CC</sub> = 3.6V	2.2		V <sub>CC</sub> + 0.5V	V
V <sub>IL</sub>	Input LOW Voltage		V <sub>CC</sub> = 2.7V	-0.5		0.8	V
I <sub>IX</sub>	Input Load Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>		-1	±1	+1	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output Disabled		-1	±1	+1	μA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	I <sub>OUT</sub> = 0 mA, (f = f <sub>MAX</sub> = 1/t <sub>RC</sub> ) CMOS Levels	V <sub>CC</sub> = 3.6V		7	15	mA
		I <sub>OUT</sub> = 0 mA, f = 1 MHz CMOS Levels			1	2	mA
I <sub>SB1</sub>	Automatic CE Power-Down Current—CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.3V$ , V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V or V <sub>IN</sub> ≤ 0.3V, f = f <sub>MAX</sub>				100	μA
I <sub>SB2</sub>	Automatic CE Power-Down Current—CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.3V$ V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V or V <sub>IN</sub> ≤ 0.3V, f = 0	L		1	50	μA
			V <sub>CC</sub> = 3.6V LL		2	20	μA

**Capacitance<sup>[3]</sup>**

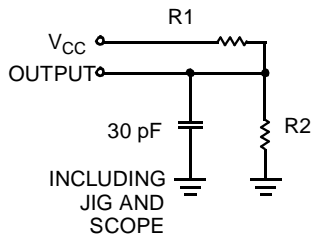
Parameter	Description	Test Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = 3.0V	6	pF
C <sub>OUT</sub>	Output Capacitance		8	pF

**Thermal Resistance**

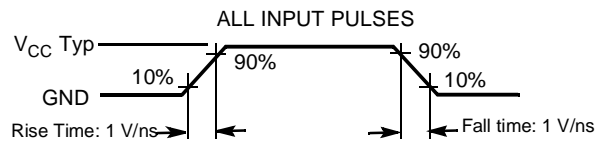
Description	Test Conditions	Symbol	Others	BGA	Units
Thermal Resistance <sup>[3]</sup> (Junction to Ambient)	Still Air, soldered on a 4.25 x 1.125 inch, 4-layer printed circuit board	Θ <sub>JA</sub>	TBD	TBD	°C/W
Thermal Resistance <sup>[3]</sup> (Junction to Case)		Θ <sub>JC</sub>	TBD	TBD	°C/W

**Note:**

3. Tested initially and after any design or process changes that may affect these parameters.

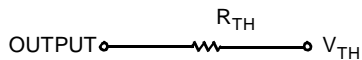
**AC Test Loads and Waveforms**


62148V-3



62148V-4

Equivalent to: THEVENIN EQUIVALENT



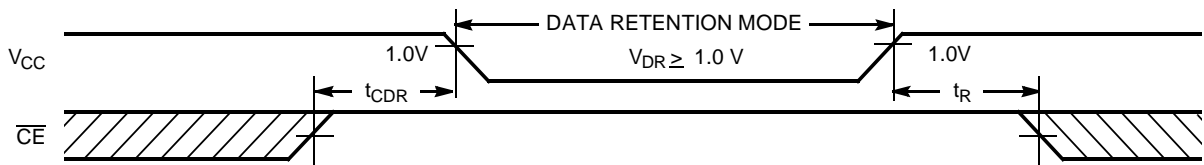
Parameters	3.0V	Unit
R1	1105	Ohms
R2	1550	Ohms
R <sub>TH</sub>	645	Ohms
V <sub>TH</sub>	1.75V	Volts

**Data Retention Characteristics (Over the Operating Range)**

Parameter	Description	Conditions		Min.	Typ. <sup>[2]</sup>	Max.	Unit
V <sub>DR</sub>	V <sub>CC</sub> for Data Retention			1.0		3.6	V
I <sub>CCDR</sub>	Data Retention Current	V <sub>CC</sub> = 1.0V CE ≥ V <sub>CC</sub> - 0.3V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V or V <sub>IN</sub> ≤ 0.3V No input may exceed V <sub>CC</sub> +0.3V	L/ LL		0.2	5.5	μA
t <sub>CDR</sub> <sup>[3]</sup>	Chip Deselect to Data Retention Time			0			ns
t <sub>R</sub> <sup>[4]</sup>	Operation Recovery Time			t <sub>RC</sub>			ns

**Note:**

4. Full Device AC operation requires linear V<sub>CC</sub> ramp from V<sub>DR</sub> to V<sub>CC(min.)</sub> ≥ 10 μs or stable at V<sub>CC(min.)</sub> ≥ 10 μs.

**Data Retention Waveform**


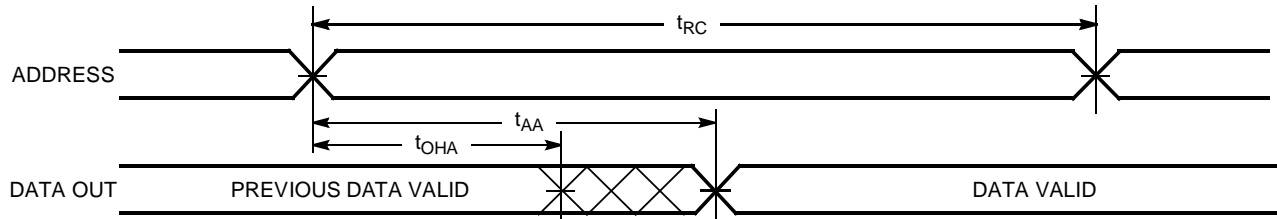
62148V-5

**Switching Characteristics** Over the Operating Range<sup>[5]</sup>

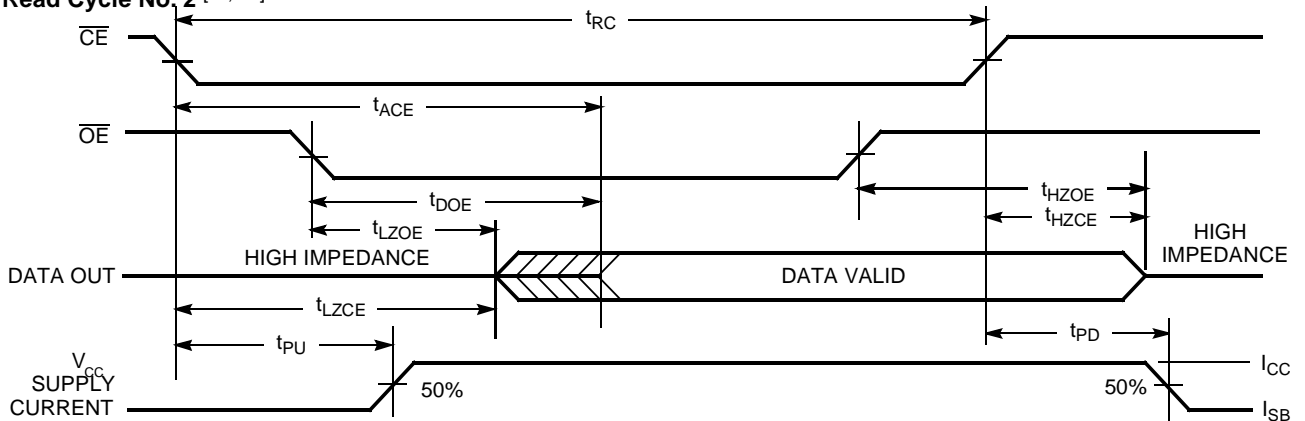
Parameter	Description	(2.7V–3.6V Operation)		Unit
		Min.	Max.	
<b>READ CYCLE</b>				
$t_{RC}$	Read Cycle Time	70		ns
$t_{AA}$	Address to Data Valid		70	ns
$t_{OHA}$	Data Hold from Address Change	10		ns
$t_{ACE}$	$\overline{CE}$ LOW to Data Valid		70	ns
$t_{DOE}$	$\overline{OE}$ LOW to Data Valid		35	ns
$t_{LZOE}$	$\overline{OE}$ LOW to Low Z <sup>[6]</sup>	5		ns
$t_{HZOE}$	$\overline{OE}$ HIGH to High Z <sup>[7]</sup>		25	ns
$t_{LZCE}$	$\overline{CE}$ LOW to Low Z <sup>[6]</sup>	10		ns
$t_{HZCE}$	$\overline{CE}$ HIGH to High Z <sup>[6, 7]</sup>		25	ns
$t_{PU}$	$\overline{CE}$ LOW to Power-Up	0		ns
$t_{PD}$	$\overline{CE}$ HIGH to Power-Down		70	ns
<b>WRITE CYCLE<sup>[8, 9]</sup></b>				
$t_{WC}$	Write Cycle Time	70		ns
$t_{SCE}$	$\overline{CE}$ LOW to Write End	60		ns
$t_{AW}$	Address Set-Up to Write End	60		ns
$t_{HA}$	Address Hold from Write End	0		ns
$t_{SA}$	Address Set-Up to Write Start	0		ns
$t_{PWE}$	$\overline{WE}$ Pulse Width	50		ns
$t_{SD}$	Data Set-Up to Write End	30		ns
$t_{HD}$	Data Hold from Write End	0		ns
$t_{HZWE}$	$\overline{WE}$ LOW to High Z <sup>[6, 7]</sup>		25	ns
$t_{LZWE}$	$\overline{WE}$ HIGH to Low Z <sup>[6]</sup>	10		ns

**Notes:**

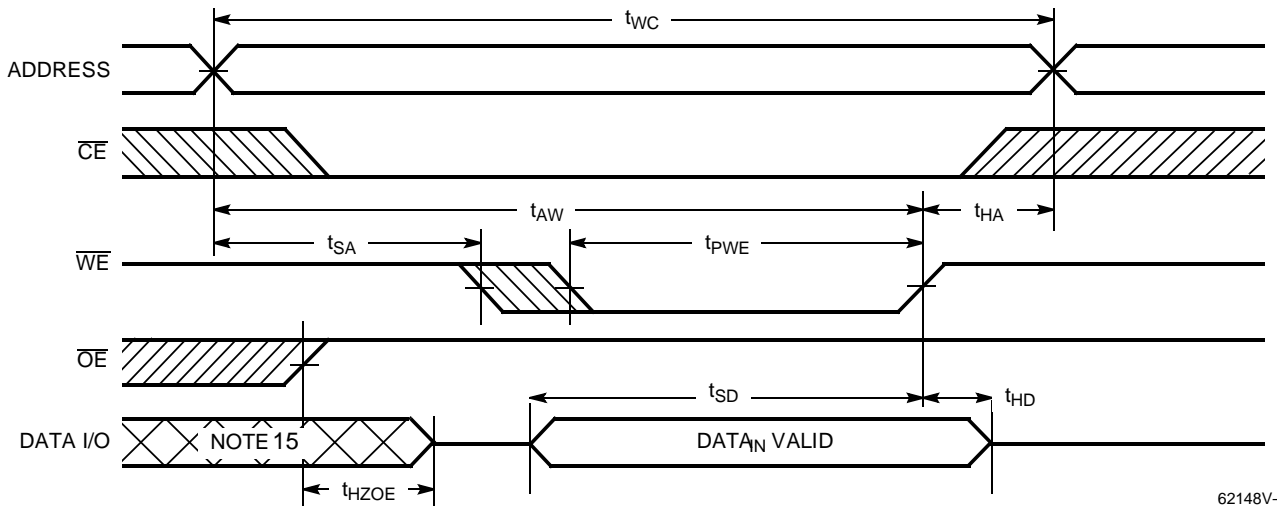
- Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to  $V_{CC(typ)}$ , and output loading of the specified  $I_{OL}/I_{OH}$  and 30 pF load capacitance.
- At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any given device.
- $t_{HZOE}$ ,  $t_{HZCE}$ , and  $t_{HZWE}$  are specified with  $C_L = 5$  pF as in part (b) of AC Test Loads. Transition is measured  $\pm 200$  mV from steady-state voltage.
- The internal write time of the memory is defined by the overlap of  $\overline{CE}$  LOW and  $\overline{WE}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
- The minimum write cycle time for Write Cycle #3 ( $\overline{WE}$  controlled,  $\overline{OE}$  LOW) is the sum of  $t_{HZWE}$  and  $t_{SD}$ .

**Switching Waveforms**
**Read Cycle No. 1**<sup>[10, 11]</sup>


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**Read Cycle No. 2**<sup>[11, 12]</sup>


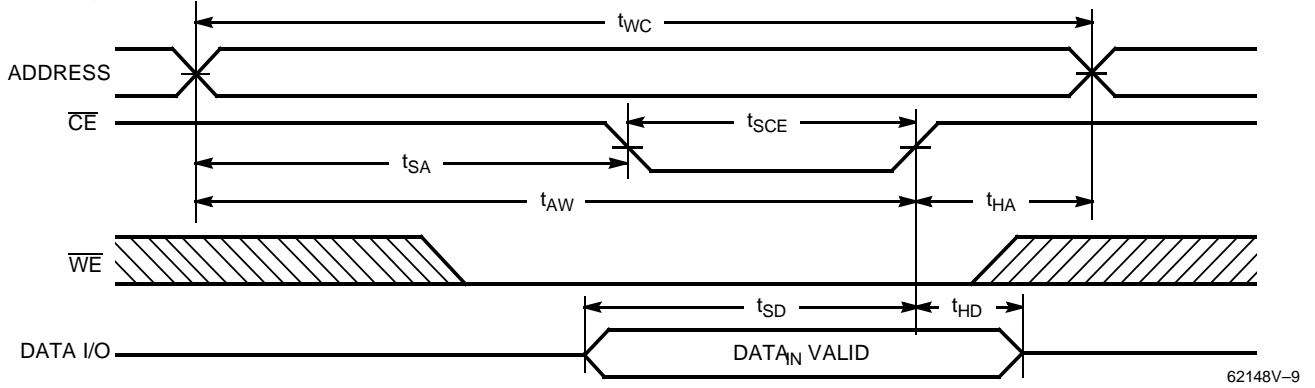
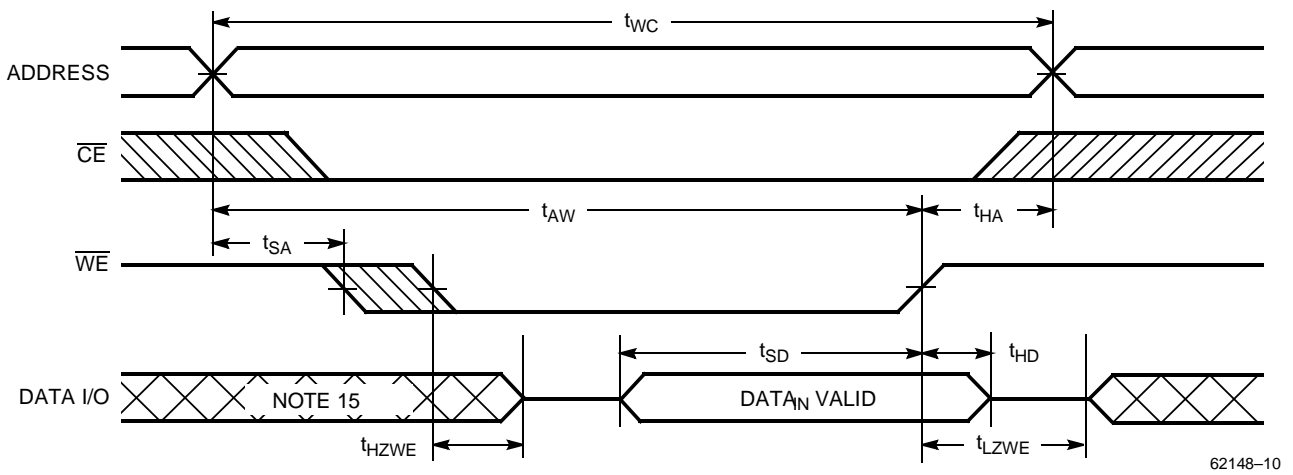
62148V-7

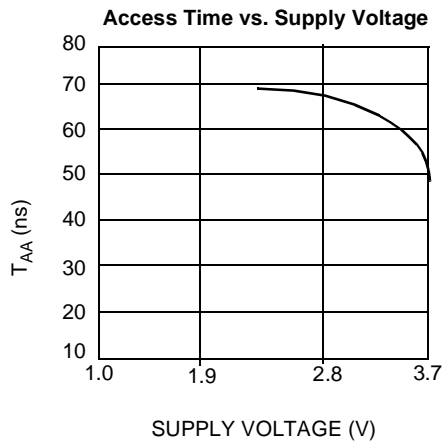
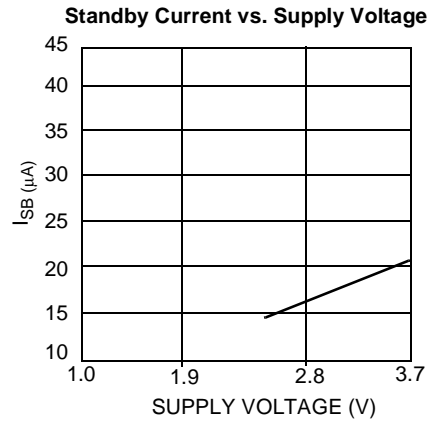
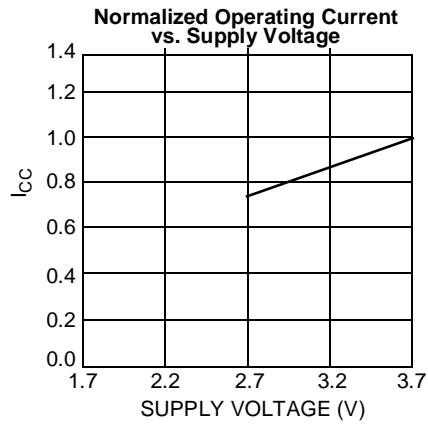
**Write Cycle No. 1 (WE Controlled)**<sup>[8, 13, 14]</sup>


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**Notes:**

10. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE} = V_{IL}$ .
11.  $\overline{WE}$  is HIGH for read cycle.
12. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.
13. Data I/O is high impedance if  $\overline{OE} = V_{IH}$ .
14. If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  HIGH, the output remains in a high-impedance state.
15. During this period, the I/Os are in output state and input signals should not be applied.

**Switching Waveforms (continued)**
**Write Cycle No. 2 ( $\overline{CE}$  Controlled)** [8, 13, 14]

**Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW)** [9, 14]


**Typical DC and AC Characteristics**

**Truth Table**

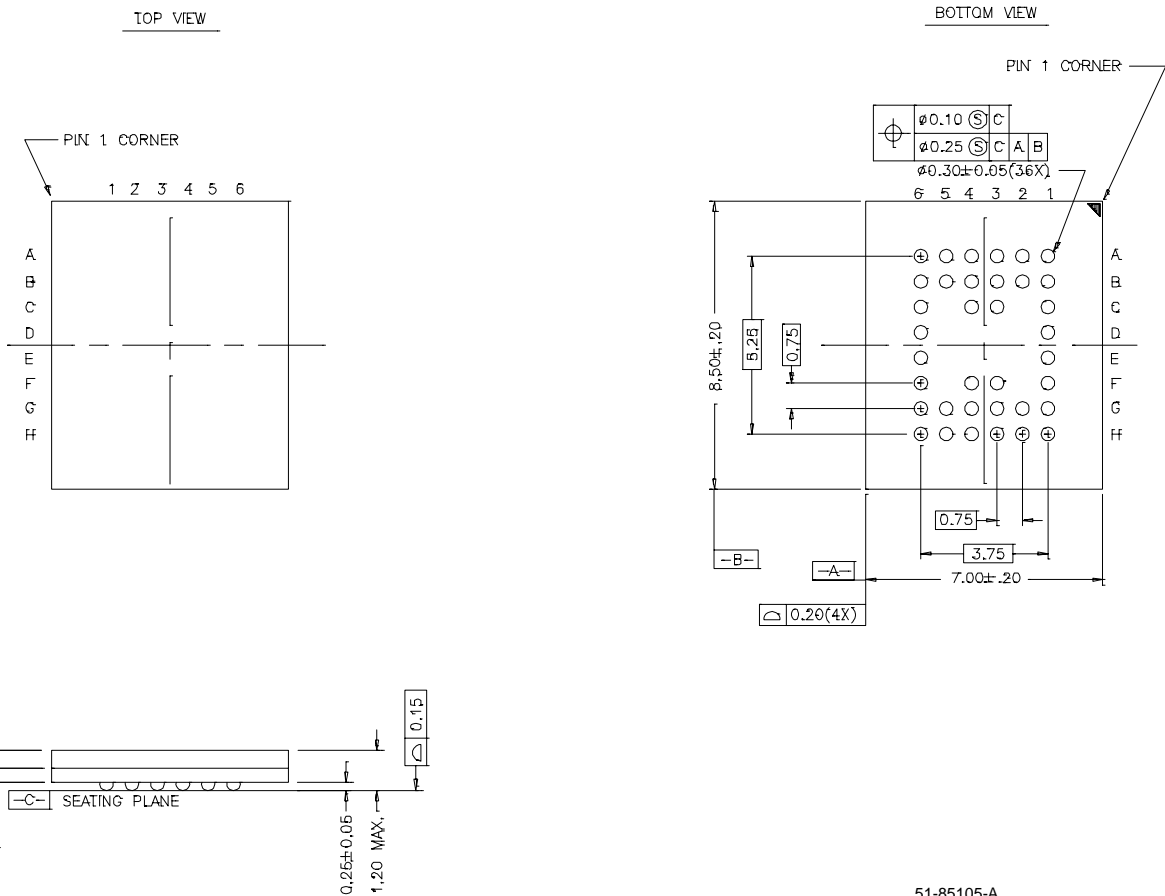
$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Inputs/Outputs	Mode	Power
H	X	X	High Z	Deselect/Power-Down	Standby ( $I_{SB}$ )
L	H	L	Data Out	Read	Active ( $I_{CC}$ )
L	L	X	Data In	Write	Active ( $I_{CC}$ )
L	H	H	High Z	Output Disabled	Active ( $I_{CC}$ )



**Ordering Information**

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
70	CY62148VLL-70BAI	BA37	36-Ball Fine Pitch BGA	Industrial
	CY62148VLL-70ZI	ZS32	32-Lead TSOPII	
	CY62148VLL-70SI	S34	32-Lead 450 mil. molded SOIC	

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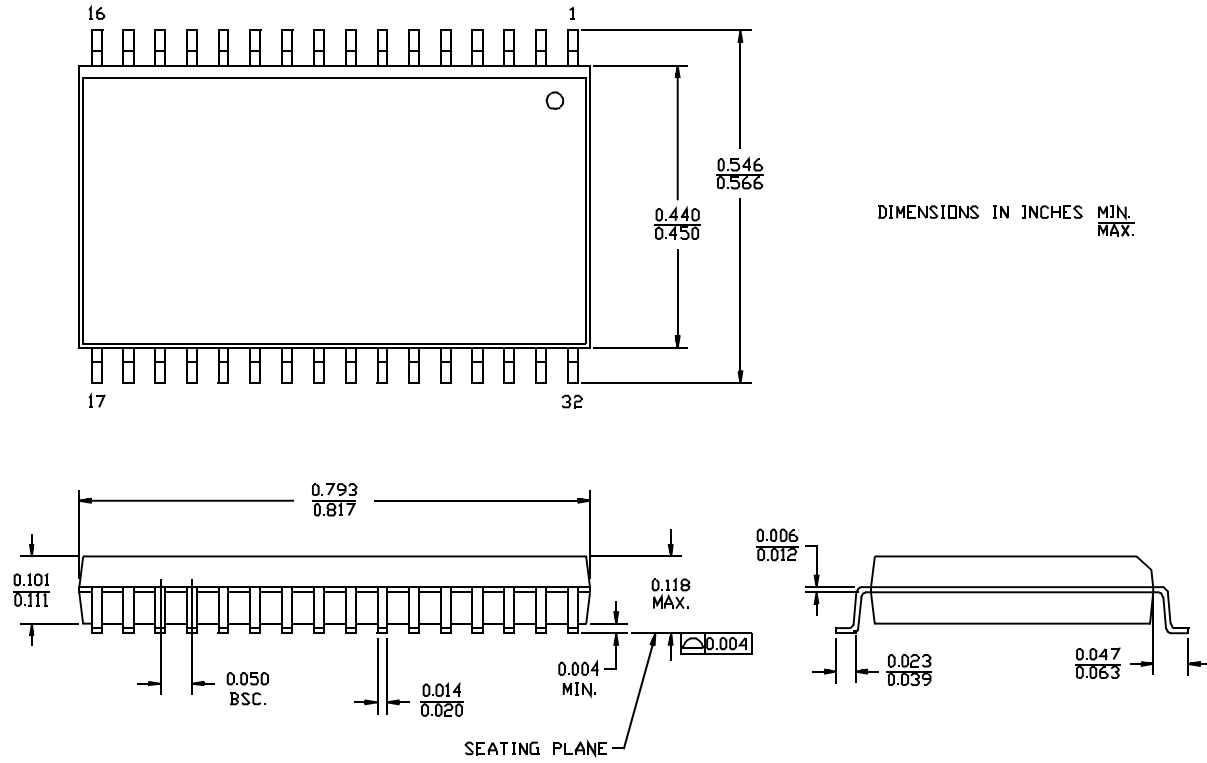
**Package Diagrams**
**36-Ball (7.00 mm x 8.5 mm x 1.5 mm) Thin BGA BA37**


51-85105-A

\* THE BALL DIAMETER, BALL PITCH, STAND-OFF & PACKAGE THICKNESS ARE DIFFERENT FROM JEDEC SPEC M0192 (LOW PROFILE BGA FAMILY)

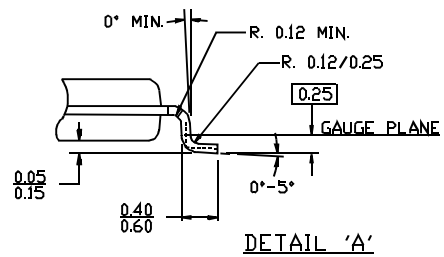
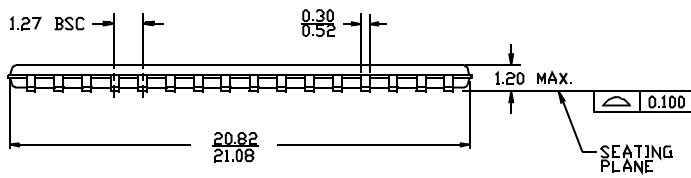
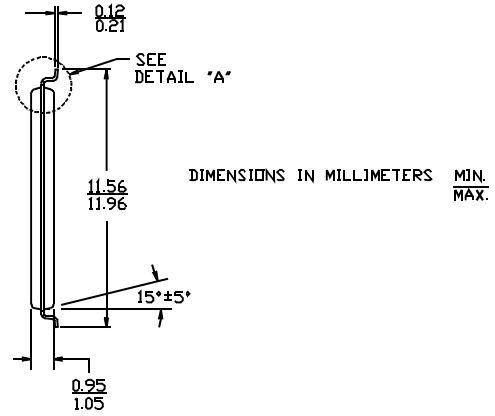
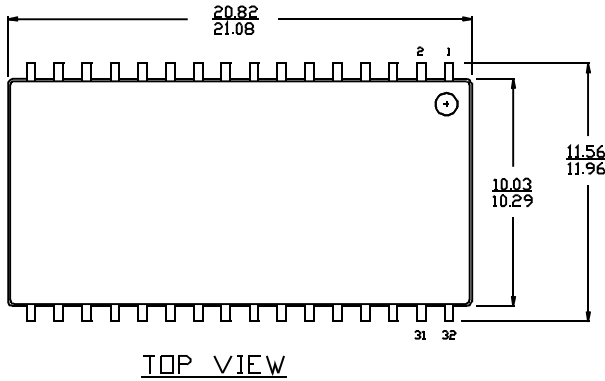
Package Diagrams (continued)

32-Lead (450 MIL) Molded SOIC S34



Package Diagrams (continued)

32-Lead TSOP II ZS32



51-85095