

# 1 Mb (64K x 16) Static RAM

## Features

- Very high speed: 45 ns
- Wide voltage range: 2.2V to 3.6V
- Pin compatible with CY62127BV
- Ultra-low active power
  - Typical active current: 0.85 mA @ f = 1 MHz
  - Typical active current: 5 mA @ f = f<sub>MAX</sub>
- Ultra-low standby power
- Easy memory expansion with  $\overline{CE}$  and  $\overline{OE}$  features
- Automatic power-down when deselected
- Packages offered in a 48-ball FBGA and a 44-lead TSOP Type II
- Also available in Lead-Free 48-ball FBGA, and 44-lead TSOP Type II packages

## Functional Description<sup>[1]</sup>

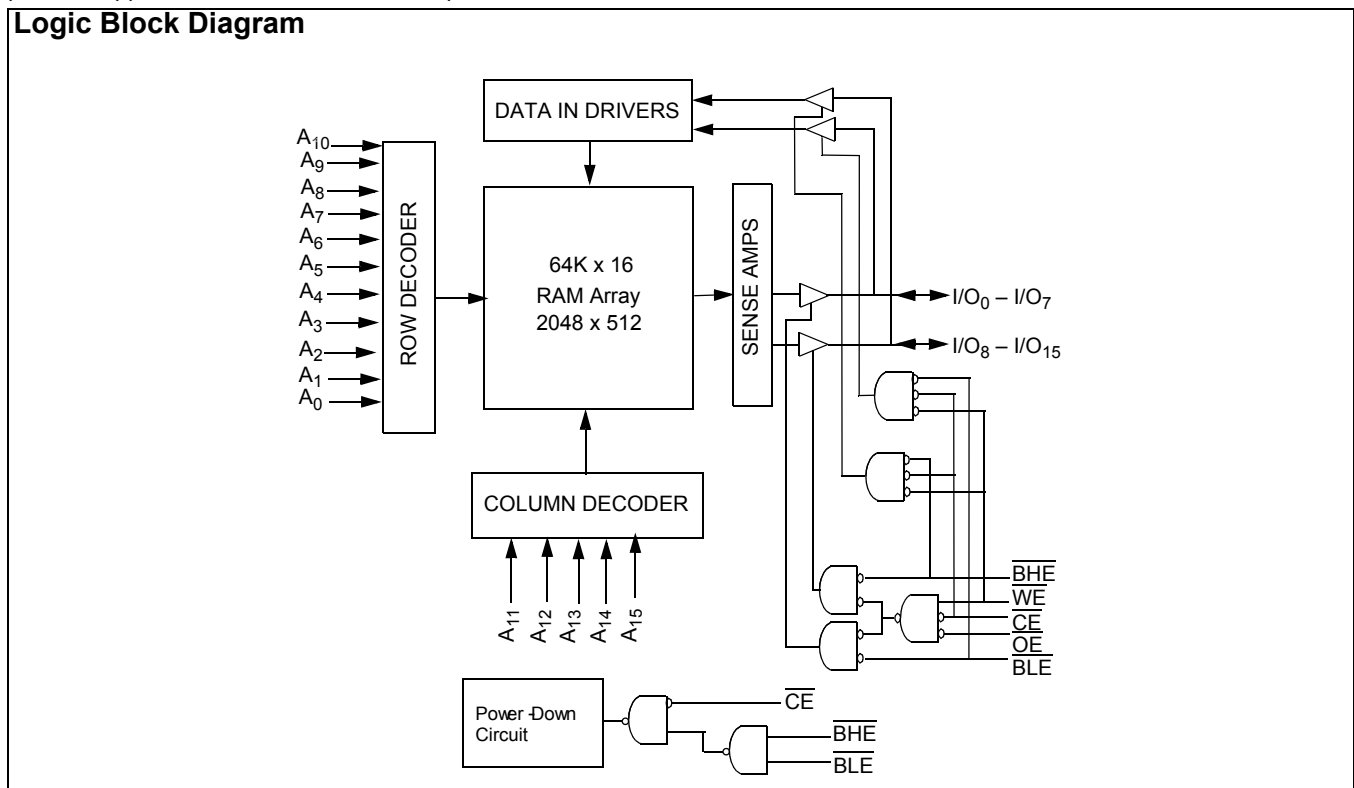
The CY62127DV30 is a high-performance CMOS static RAM organized as 64K words by 16 bits. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL<sup>®</sup>) in portable applications such as cellular telephones. The device

also has an automatic power-down feature that significantly reduces power consumption by 90% when addresses are not toggling. The device can be put into standby mode reducing power consumption by more than 99% when deselected ( $\overline{CE}$  HIGH or both  $\overline{BHE}$  and  $\overline{BLE}$  are HIGH). The input/output pins ( $I/O_0$  through  $I/O_{15}$ ) are placed in a high-impedance state when: deselected ( $\overline{CE}$  HIGH), outputs are disabled ( $\overline{OE}$  HIGH), both Byte High Enable and Byte Low Enable are disabled ( $\overline{BHE}$ ,  $\overline{BLE}$  HIGH) or during a write operation ( $\overline{CE}$  LOW and  $\overline{WE}$  LOW).

Writing to the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Write Enable ( $\overline{WE}$ ) inputs LOW. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from I/O pins ( $I/O_0$  through  $I/O_7$ ), is written into the location specified on the address pins ( $A_0$  through  $A_{15}$ ). If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from I/O pins ( $I/O_8$  through  $I/O_{15}$ ) is written into the location specified on the address pins ( $A_0$  through  $A_{15}$ ).

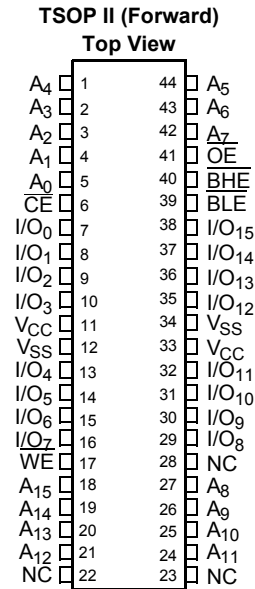
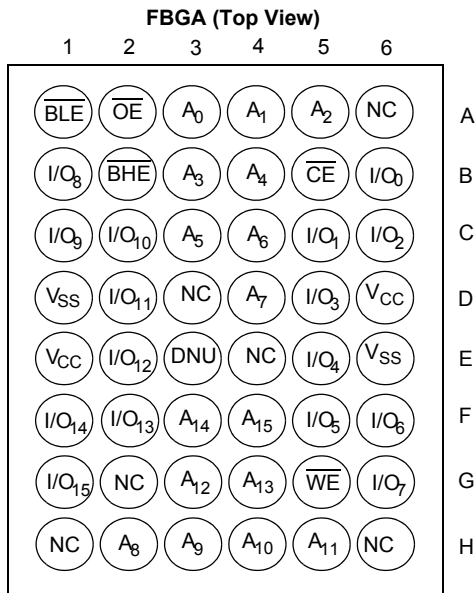
Reading from the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Output Enable ( $\overline{OE}$ ) LOW while forcing the Write Enable ( $\overline{WE}$ ) HIGH. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from the memory location specified by the address pins will appear on  $I/O_0$  to  $I/O_7$ . If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from memory will appear on  $I/O_8$  to  $I/O_{15}$ . See the truth table at the back of this data sheet for a complete description of read and write modes.

## Logic Block Diagram



### Note:

1. For best-practice recommendations, please refer to the Cypress application note "System Design Guidelines" on <http://www.cypress.com>.

**Pin Configuration<sup>[2, 3]</sup>**

**Product Portfolio**

Product	V <sub>CC</sub> Range (V)			Speed (ns)	Power Dissipation					
					Operating, I <sub>CC</sub> (mA)				Standby, I <sub>SB2</sub> (μA)	
	f = 1 MHz		f = f <sub>MAX</sub>							
	Min.	Typ.	Max.		Typ. <sup>[4]</sup>	Max.	Typ. <sup>[4]</sup>	Max.	Typ. <sup>[4]</sup>	Max.
CY62127DV30L	2.2	3.0	3.6	45	0.85	1.5	6.5	13	1.5	5
CY62127DV30LL				45	0.85	1.5	6.5	13	1.5	4
CY62127DV30L	2.2	3.0	3.6	55	0.85	1.5	5	10	1.5	5
CY62127DV30LL				55	0.85	1.5	5	10	1.5	4
CY62127DV30L	2.2	3.0	3.6	70	0.85	1.5	5	10	1.5	5
CY62127DV30LL				70	0.85	1.5	5	10	1.5	4

**Notes:**

- NC pins are not connected to the die.
- E3 (DNU) can be left as NC or V<sub>SS</sub> to ensure proper operation. (Expansion Pins on FBGA Package: E4 - 2M, D3 - 4M, H1 - 8M, G2 - 16M, H6 - 32M).
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC(typ)</sub>, T<sub>A</sub> = 25°C.

### Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C

Ambient Temperature with Power Applied..... -55°C to +125°C

Supply Voltage to Ground Potential ..... -0.3V to 3.9V

DC Voltage Applied to Outputs in High-Z State<sup>[5]</sup> ..... -0.3V to  $V_{CC} + 0.3V$

DC Input Voltage<sup>[5]</sup> ..... -0.3V to  $V_{CC} + 0.3V$

Output Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage..... > 2001V (per MIL-STD-883, Method 3015)

Latch-up Current..... > 200 mA

### Operating Range

Range	Ambient Temperature (T <sub>A</sub> )	V <sub>CC</sub> <sup>[6]</sup>
Industrial	-40°C to +85°C	2.2V to 3.6V

### DC Electrical Characteristics (Over the Operating Range)

Parameter	Description	Test Conditions	CY62127DV30-45			CY62127DV30-55			CY62127DV30-70			Unit	
			Min.	Typ. <sup>[4]</sup>	Max.	Min.	Typ. <sup>[4]</sup>	Max.	Min.	Typ. <sup>[4]</sup>	Max.		
V <sub>OH</sub>	Output HIGH Voltage	2.2 ≤ V <sub>CC</sub> ≤ 2.7	I <sub>OH</sub> = -0.1 mA	2.0			2.0			2.0			V
		2.7 ≤ V <sub>CC</sub> ≤ 3.6	I <sub>OH</sub> = -1.0 mA	2.4			2.4			2.4			
V <sub>OL</sub>	Output LOW Voltage	2.2 ≤ V <sub>CC</sub> ≤ 2.7	I <sub>OL</sub> = 0.1 mA			0.4			0.4			0.4	V
		2.7 ≤ V <sub>CC</sub> ≤ 3.6	I <sub>OL</sub> = 2.1 mA			0.4			0.4			0.4	
V <sub>IH</sub>	Input HIGH Voltage	2.2 ≤ V <sub>CC</sub> ≤ 2.7		1.8		V <sub>CC</sub> + 0.3	1.8		V <sub>CC</sub> + 0.3	1.8		V <sub>CC</sub> + 0.3	V
		2.7 ≤ V <sub>CC</sub> ≤ 3.6		2.2		V <sub>CC</sub> + 0.3	2.2		V <sub>CC</sub> + 0.3	2.2		V <sub>CC</sub> + 0.3	
V <sub>IL</sub>	Input LOW Voltage	2.2 ≤ V <sub>CC</sub> ≤ 2.7		-0.3		0.6	-0.3		0.6	-0.3		0.6	V
		2.7 ≤ V <sub>CC</sub> ≤ 3.6		-0.3		0.8	-0.3		0.8	-0.3		0.8	
I <sub>IX</sub>	Input Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>		-1		+1	-1		+1	-1		+1	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output Disabled		-1		+1	-1		+1	-1		+1	μA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	f = f <sub>MAX</sub> = 1/t <sub>RC</sub>	V <sub>CC</sub> = 3.6V, I <sub>OUT</sub> = 0 mA, CMOS level		6.5	13		5	10		5	10	mA
		f = 1 MHz			0.85	1.5		0.85	1.5		0.85	1.5	
I <sub>SB1</sub>	Automatic CE Power-down Current—CMOS Inputs	CE ≥ V <sub>CC</sub> - 0.2V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V, V <sub>IN</sub> ≤ 0.2V, f = f <sub>MAX</sub> (Address and Data Only), f = 0 (OE, WE, BHE and BLE)	L		1.5	5		1.5	5		1.5	5	μA
			LL		1.5	4		1.5	4		1.5	4	
I <sub>SB2</sub>	Automatic CE Power-down Current—CMOS Inputs	CE ≥ V <sub>CC</sub> - 0.2V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V or V <sub>IN</sub> ≤ 0.2V, f = 0, V <sub>CC</sub> = 3.6V	L		1.5	5		1.5	5		1.5	5	μA
			LL		1.5	4		1.5	4		1.5	4	

#### Notes:

5. V<sub>IL(min.)</sub> = -2.0V for pulse durations less than 20 ns., V<sub>IH(max.)</sub> = V<sub>CC</sub>+0.75V for pulse durations less than 20 ns.

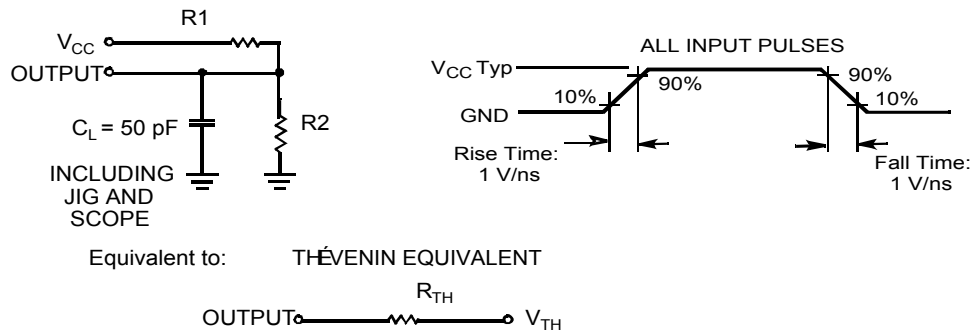
6. Full device Operation Requires linear Ramp of V<sub>CC</sub> from 0V to V<sub>CC(min)</sub> & V<sub>CC</sub> must be stable at V<sub>CC(min)</sub> for 500 μs.

**Capacitance<sup>[7]</sup>**

Parameter	Description	Test Conditions	Max.	Unit
$C_{IN}$	Input Capacitance	$T_A = 25^\circ\text{C}$ , $f = 1\text{ MHz}$ $V_{CC} = V_{CC(\text{typ})}$	8	pF
$C_{OUT}$	Output Capacitance		8	pF

**Thermal Resistance**

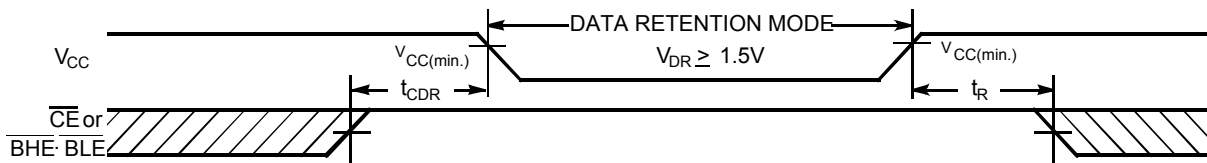
Parameter	Description	Test Conditions	FBGA	TSOP II	Unit
$\theta_{JA}$	Thermal Resistance (Junction to Ambient) <sup>[7]</sup>	Still Air, soldered on a 3 x 4.5 inch, two-layer printed circuit board	55	76	$^\circ\text{C/W}$
$\theta_{JC}$	Thermal Resistance (Junction to Case) <sup>[7]</sup>		12	11	$^\circ\text{C/W}$

**AC Test Loads and Waveforms<sup>[8]</sup>**


Parameters	2.5V (2.2–2.7V)	3.0V (2.7–3.6V)	Unit
R1	16600	1103	$\Omega$
R2	15400	1554	$\Omega$
$R_{TH}$	8000	645	$\Omega$
$V_{TH}$	1.2	1.75	V

**Data Retention Characteristics**

Parameter	Description	Conditions	Min.	Typ <sup>[4]</sup>	Max.	Unit
$V_{DR}$	$V_{CC}$ for Data Retention		1.5			V
$I_{CCDR}$	Data Retention Current	$V_{CC} = 1.5\text{V}$ , $\overline{CE} \geq V_{CC} - 0.2\text{V}$ , $V_{IN} \geq V_{CC} - 0.2\text{V}$ or $V_{IN} \leq 0.2\text{V}$	L		4	$\mu\text{A}$
			LL		3	
$t_{CDR}^{[7]}$	Chip Deselect to Data Retention Time		0			ns
$t_R^{[9]}$	Operation Recovery Time		200			$\mu\text{s}$

**Data Retention Waveform<sup>[10]</sup>**

**Notes:**

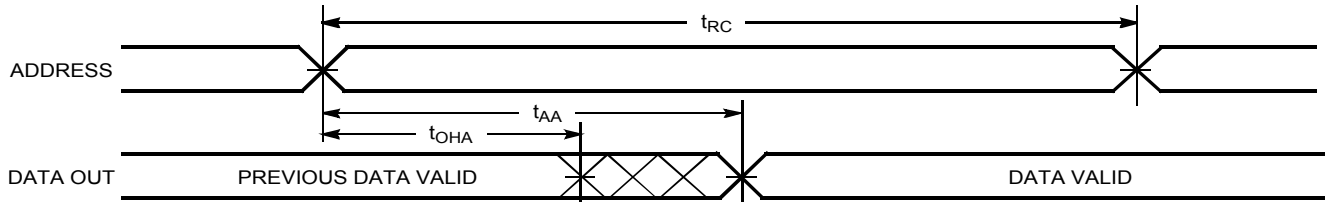
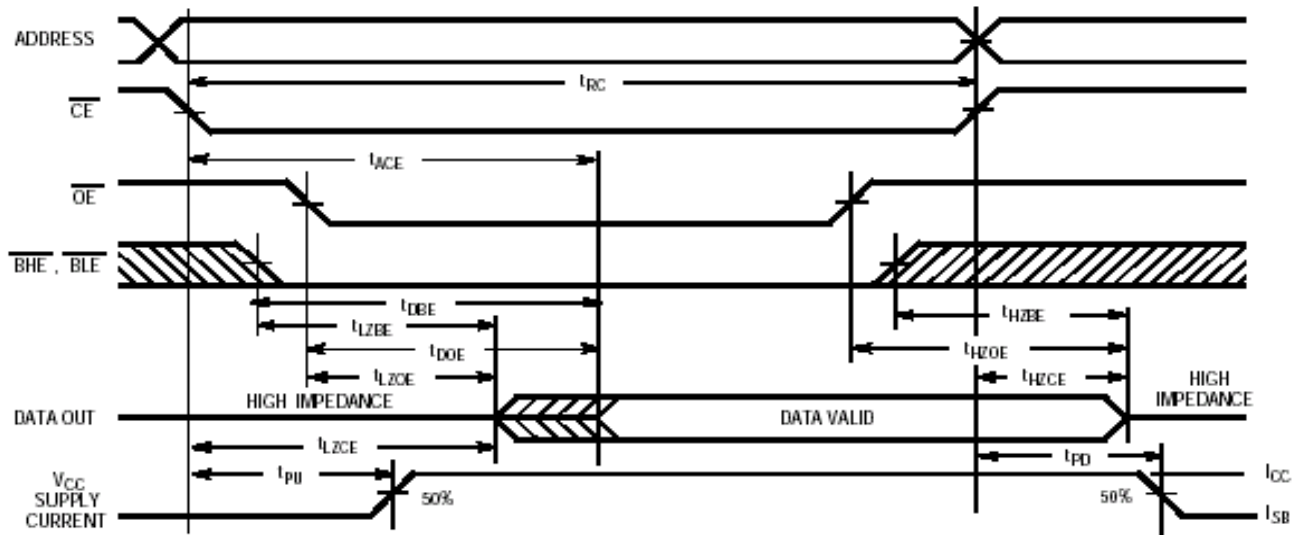
7. Tested initially and after any design or process changes that may affect these parameters.
8. Test condition for the 45-ns part is a load capacitance of 30 pF.
9. Full device operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC(\text{min.})} > 200\ \mu\text{s}$ .
10.  $\overline{BHE}:\overline{BLE}$  is the AND of both  $\overline{BHE}$  and  $\overline{BLE}$ . Chip can be deselected by either disabling the Chip Enable signals or by disabling both.

**Switching Characteristics** (Over the Operating Range)<sup>[11]</sup>

Parameter	Description	CY62127DV30-45 <sup>[8]</sup>		CY62127DV30-55		CY62127DV30-70		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
<b>Read Cycle</b>								
$t_{RC}$	Read Cycle Time	45		55		70		ns
$t_{AA}$	Address to Data Valid		45		55		70	ns
$t_{OHA}$	Data Hold from Address Change	10		10		10		ns
$t_{ACE}$	$\overline{CE}$ LOW to Data Valid		45		55		70	ns
$t_{DOE}$	$\overline{OE}$ LOW to Data Valid		25		25		35	ns
$t_{LZOE}$	$\overline{OE}$ LOW to Low Z <sup>[12]</sup>	5		5		5		ns
$t_{HZOE}$	$\overline{OE}$ HIGH to High Z <sup>[12,14]</sup>		15		20		25	ns
$t_{LZCE}$	$\overline{CE}$ LOW to Low Z <sup>[12]</sup>	10		10		10		ns
$t_{HZCE}$	$\overline{CE}$ HIGH to High Z <sup>[12,14]</sup>		20		20		25	ns
$t_{PU}$	$\overline{CE}$ LOW to Power-up	0		0		0		ns
$t_{PD}$	$\overline{CE}$ HIGH to Power-down		45		55		70	ns
$t_{DBE}$	$\overline{BLE}/\overline{BHE}$ LOW to Data Valid		45		55		70	ns
$t_{LZBE}$ <sup>[13]</sup>	$\overline{BLE}/\overline{BHE}$ LOW to Low Z <sup>[12]</sup>	5		5		5		ns
$t_{HZBE}$	$\overline{BLE}/\overline{BHE}$ HIGH to High-Z <sup>[12,14]</sup>		15		20		25	ns
<b>Write Cycle<sup>[15]</sup></b>								
$t_{WC}$	Write Cycle Time	45		55		70		ns
$t_{SCE}$	$\overline{CE}$ LOW to Write End	40		40		60		ns
$t_{AW}$	Address Set-up to Write End	40		40		60		ns
$t_{HA}$	Address Hold from Write End	0		0		0		ns
$t_{SA}$	Address Set-up to Write Start	0		0		0		ns
$t_{PWE}$	$\overline{WE}$ Pulse Width	35		40		50		ns
$t_{BW}$	$\overline{BLE}/\overline{BHE}$ LOW to Write End	40		40		60		ns
$t_{SD}$	Data Set-up to Write End	25		25		30		ns
$t_{HD}$	Data Hold from Write End	0		0		0		ns
$t_{HZWE}$	$\overline{WE}$ LOW to High Z <sup>[12,14]</sup>		15		20		25	ns
$t_{LZWE}$	$\overline{WE}$ HIGH to Low Z <sup>[12]</sup>	10		10		5		ns

**Notes:**

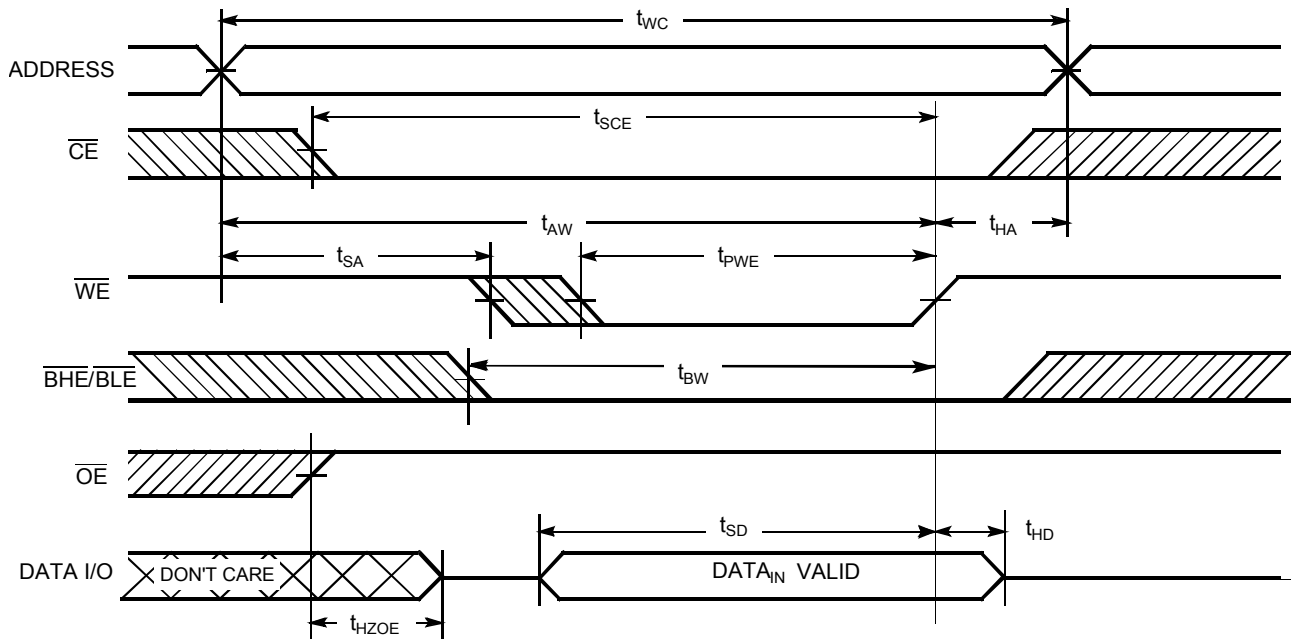
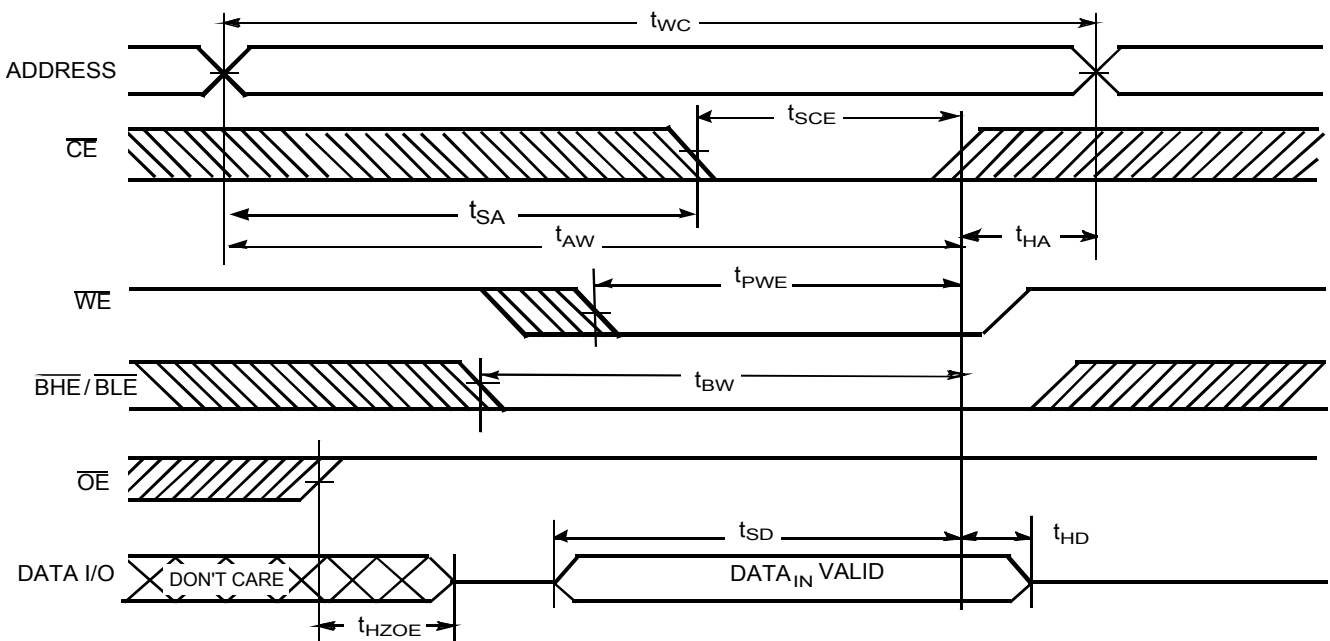
11. Test conditions assume signal transition time of 1V/ns or less, timing reference levels of  $V_{CC(typ.)}/2$ , input pulse levels of 0 to  $V_{CC(typ.)}$ , and output loading of the specified  $I_{OL}$ .
12. At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZBE}$  is less than  $t_{LZBE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any given device.
13. If both byte enables are toggled together, this value is 10 ns.
14.  $t_{HZOE}$ ,  $t_{HZCE}$ ,  $t_{HZBE}$ , and  $t_{HZWE}$  transitions are measured when the outputs enter a high-impedance state.
15. The internal Write time of the memory is defined by the overlap of  $\overline{WE}$ ,  $\overline{CE} = V_{IL}$ ,  $\overline{BHE}$  and/or  $\overline{BLE} = V_{IL}$ . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the write.

**Switching Waveforms**
**Read Cycle No. 1 (Address Transition Controlled)<sup>[16,17]</sup>**

**Read Cycle No. 2 (OE Controlled)<sup>[16,17, 18]</sup>**

**Notes:**

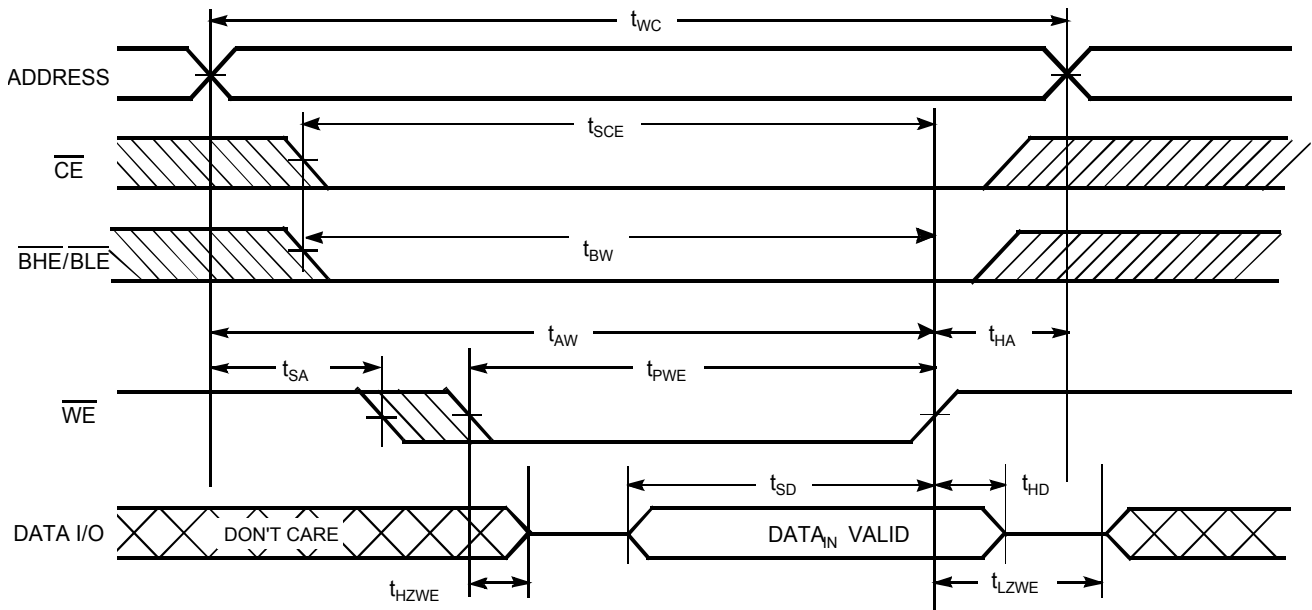
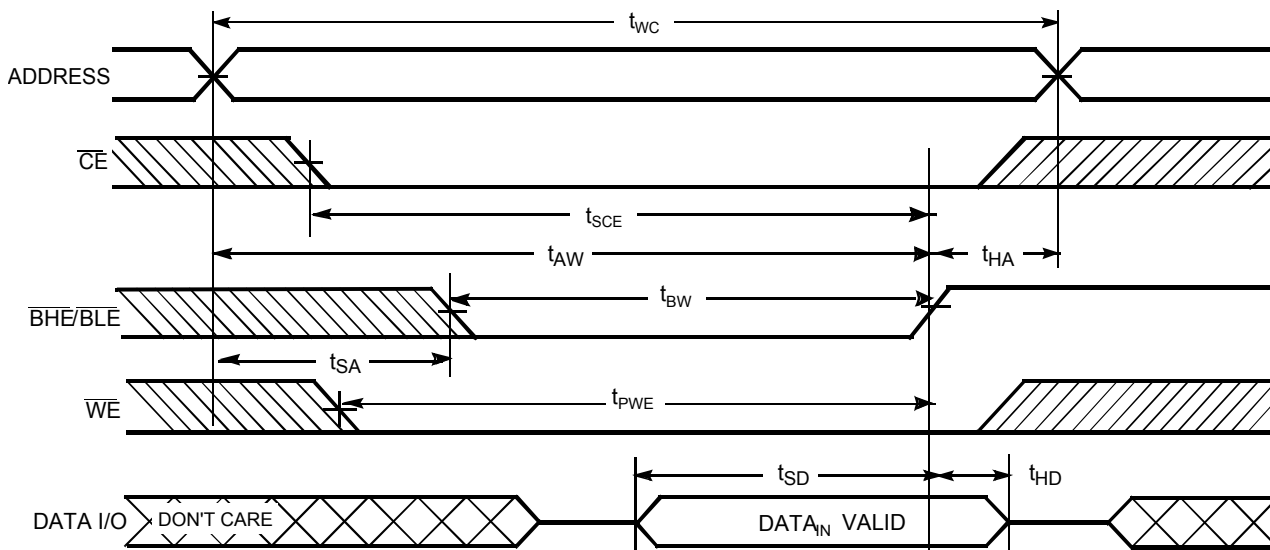
16. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE} = V_{IL}$ ,  $\overline{BHE}$ ,  $\overline{BLE} = V_{IL}$ .

17.  $\overline{WE}$  is HIGH for Read cycle.

18. Address valid prior to or coincident with  $\overline{CE}$ ,  $\overline{BHE}$ ,  $\overline{BLE}$  transition LOW.

**Switching Waveforms (continued)**
**Write Cycle No. 1 ( $\overline{WE}$  Controlled)<sup>[14, 15, 19, 20, 21]</sup>**

**Write Cycle No. 2 ( $\overline{CE}$  Controlled)<sup>[14, 15, 19, 20, 21]</sup>**

**Notes:**

19. Data I/O is high-impedance if  $\overline{OE} = V_{IH}$ .
20. If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  HIGH, the output remains in a high-impedance state.
21. During the DON'T CARE period in the DATA I/O waveform, the I/Os are in output state and input signals should not be applied.

**Switching Waveforms (continued)**
**Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW)<sup>[20, 21]</sup>**

**Write Cycle No. 4 ( $\overline{BHE}/\overline{BLE}$ -controlled,  $\overline{OE}$  LOW)<sup>[20, 21]</sup>**




**Truth Table**

CE	WE	OE	BHE	BLE	I/O <sub>0</sub> -I/O <sub>7</sub>	I/O <sub>8</sub> -I/O <sub>15</sub>	Mode	Power
H	X	X	X	X	High Z	High Z	Deselect/Power-down	Standby (I <sub>SB</sub> )
X	X	X	H	H	High Z	High Z	Deselect/Power-down	Standby (I <sub>SB</sub> )
L	H	L	L	L	Data Out	Data Out	Read All bits	Active (I <sub>CC</sub> )
L	H	L	H	L	Data Out	High Z	Read Lower Byte Only	Active (I <sub>CC</sub> )
L	H	L	L	H	High Z	Data Out	Read Upper Byte Only	Active (I <sub>CC</sub> )
L	H	H	L	L	High Z	High Z	Output Disabled	Active (I <sub>CC</sub> )
L	H	H	H	L	High Z	High Z	Output Disabled	Active (I <sub>CC</sub> )
L	H	H	L	H	High Z	High Z	Output Disabled	Active (I <sub>CC</sub> )
L	L	X	L	L	Data In	Data In	Write	Active (I <sub>CC</sub> )
L	L	X	H	L	Data In	High Z	Write Lower Byte Only	Active (I <sub>CC</sub> )
L	L	X	L	H	High Z	Data In	Write Upper Byte Only	Active (I <sub>CC</sub> )

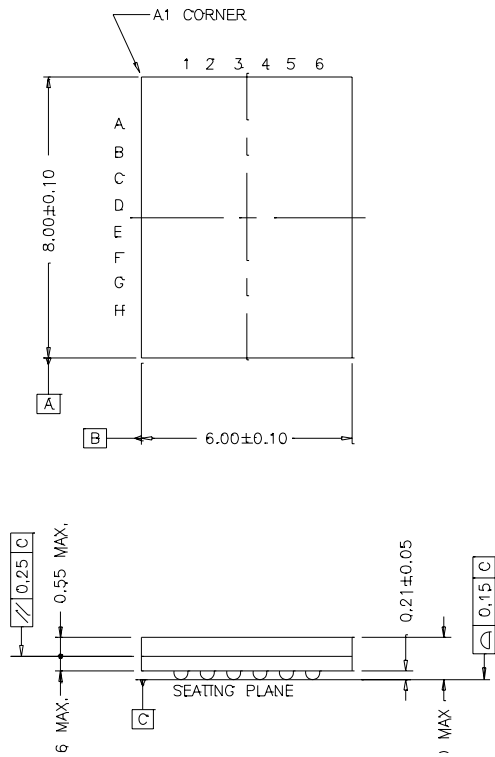
**Ordering Information**

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
45	CY62127DV30LL-45BVI	BV48A	48-ball Fine Pitch BGA (6 mm x 8 mm x 1 mm)	Industrial
	CY62127DV30LL-45BVXI	BV48A	48-ball Fine Pitch BGA (6 mm x 8 mm x 1 mm) (Pb-Free)	
	CY62127DV30LL-45ZSI	ZS44	44-lead TSOP Type II	
	CY62127DV30LL-45ZSXI	ZS44	44-lead TSOP Type II (Pb-Free)	
55	CY62127DV30L-55BVI	BV48A	48-ball Fine Pitch BGA (6 mm x 8 mm x 1 mm)	Industrial
	CY62127DV30LL-55BVI	BV48A	48-ball Fine Pitch BGA (6 mm x 8 mm x 1 mm)	
	CY62127DV30LL-55BVXI	BV48A	48-ball Fine Pitch BGA (6 mm x 8 mm x 1 mm) (Pb-Free)	
	CY62127DV30L-55ZSI	ZS44	44-lead TSOP Type II	
	CY62127DV30L-55ZSXI	ZS44	44-lead TSOP Type II (Pb-Free)	
	CY62127DV30LL-55ZSI	ZS44	44-lead TSOP Type II	
70	CY62127DV30L-70BVI	BV48A	48-ball Fine Pitch BGA (6 mm x 8 mm x 1 mm)	Industrial
	CY62127DV30LL-70BVI	BV48A	48-ball Fine Pitch BGA (6 mm x 8 mm x 1 mm)	
	CY62127DV30LL-70BVXI	BV48A	48-ball Fine Pitch BGA (6 mm x 8 mm x 1 mm) (Pb-Free)	
	CY62127DV30L-70ZSI	ZS44	44-lead TSOP Type II	
	CY62127DV30LL-70ZSI	ZS44	44-lead TSOP Type II	

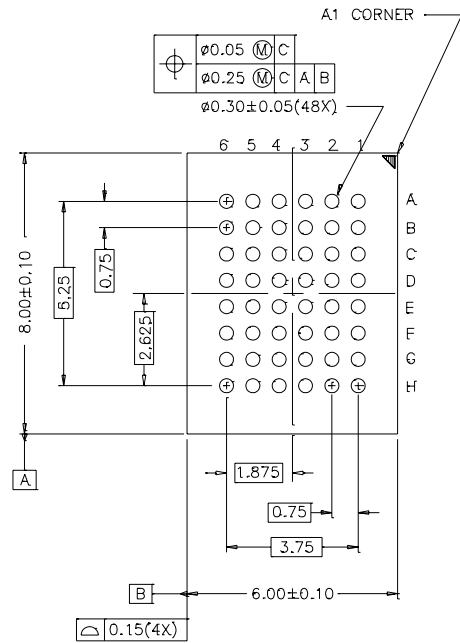
Package Diagrams

48-Lead VFBGA (6 x 8 x 1 mm) BV48A

TOP VIEW



BOTTOM VIEW

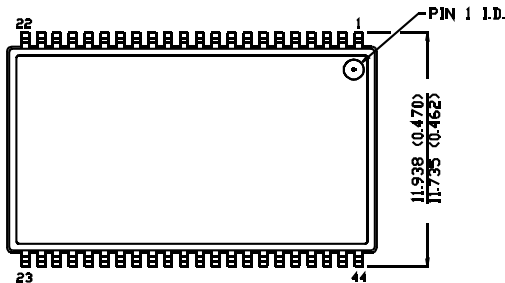


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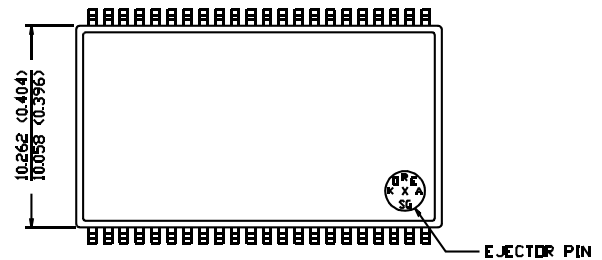
Package Diagrams

44-pin TSOP II ZS44

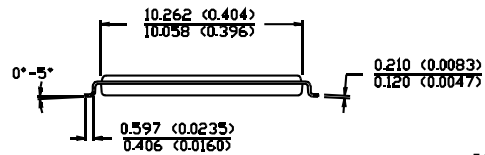
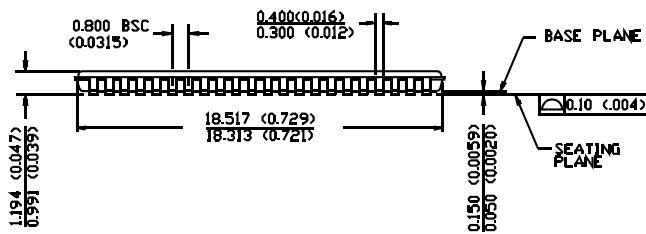
DIMENSION IN MM (INCH)  
MAX  
MIN



TOP VIEW



BOTTOM VIEW



51-85087-A

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**Document History Page**

Document Title: CY62127DV30 MoBL <sup>®</sup> 1 Mb (64K x 16) Static RAM				
Document Number: 38-05229				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	117690	08/27/02	JUI	New Data Sheet
*A	127311	06/13/03	MPR	Changed From Advanced Status to Preliminary Changed Isb2 to 5 $\mu$ A (L), 4 $\mu$ A (LL) Changed Iccdr to 4 $\mu$ A (L), 3 $\mu$ A (LL) Changed Cin from 6 pF to 8 pF
*B	128341	07/22/03	JUI	Changed from Preliminary to Final Add 70-ns speed, updated ordering information
*C	129000	08/29/03	CDY	Changed Icc 1 MHz typ from 0.5 mA to 0.85 mA
*D	316039	See ECN	PCI	Added 45-ns Speed Bin in AC, DC and Ordering Information tables Added Footnote # 8 on page #4 Added Lead-Free Package ordering information on page# 9 Changed 44-lead TSOP-II package name from Z44 to ZS44