PRELIMINARY

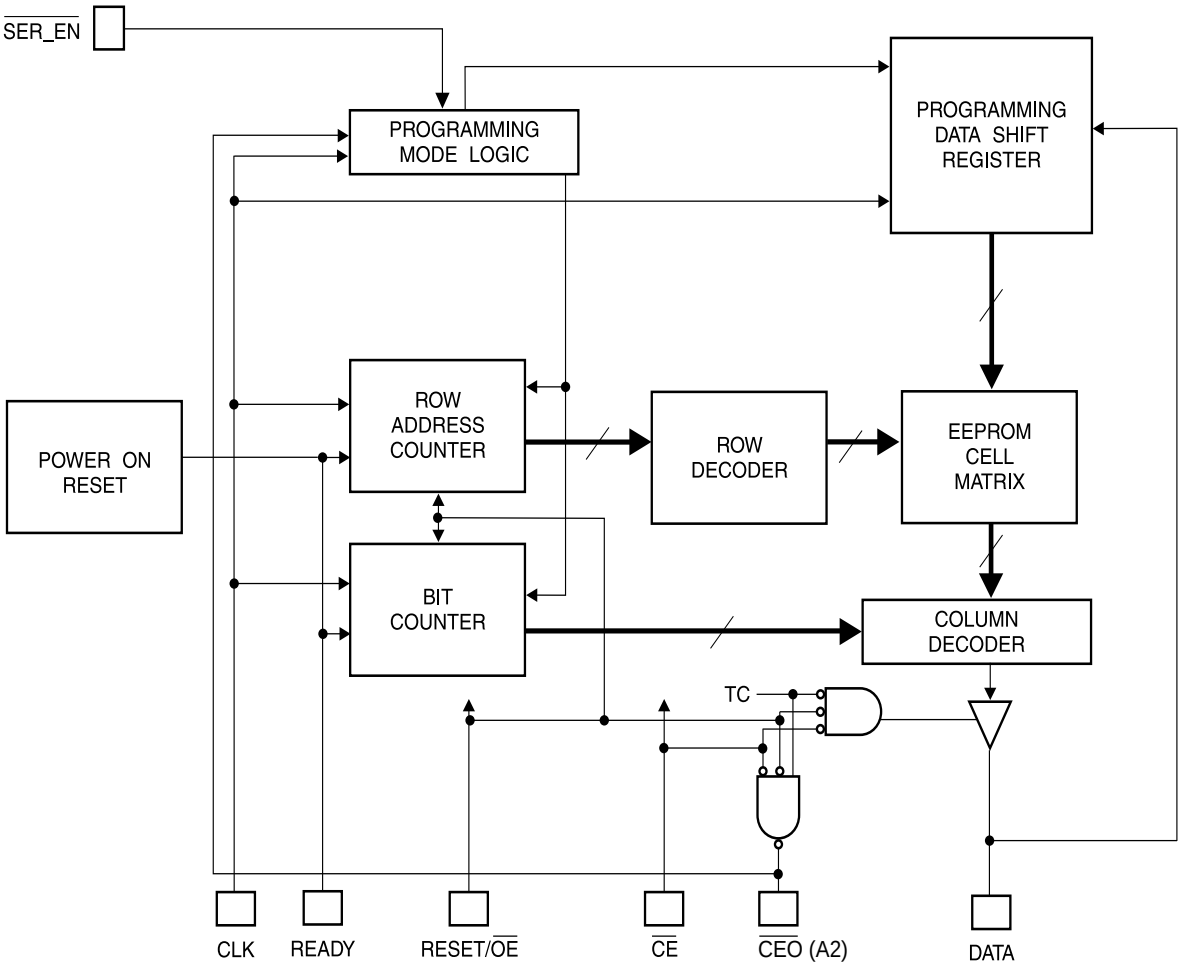
CY3LV512/010

512K / 1 Mbit CPLD Boot EEPROM

Features

- EE Reprogrammable 524,288 x 1- and 1,048,576 x 1-bit Serial Memories Designed to Store Configuration Data for Complex Programmable Logic Devices (CPLDs)
- In-System Programmable via two-wire Bus using Cypress's CYDH2200E Programming Kits
- Simple Interface to SRAM-based CPLDs
- Compatible with Cypress Delta39K™ & Quantum38K™ CPLDs
- Cascadable Read-Back to Support Higher-density CPLDs
- Low-power CMOS EEPROM Process
- Available in PLCC Package (Pin Compatible Across Product Family)
- Operate at 3.3V V_{CC}
- System-friendly READY Pin
- Low-power Standby Mode

Block Diagram



Functional Description

The CY3LV512/010 (high-density CY3LV Series) CPLD boot EEPROMs provide an easy-to-use, cost-effective configuration memory for Complex Programmable Logic Devices. The CY3LV Series is packaged in the popular 20-pin PLCC. These devices support a system-friendly READY pin, which signifies a “good” power level to the CPLD and can be used to ensure reliable system power-up.

The CY3LV Series boot PROMs can be programmed with industry-standard programmers or Cypress’s CYDH2200E CPLD boot PROM programming kit. Please refer to the data sheet “CYDH2200E CPLD Boot PROM Programming Kit” for details.

CPLD Master Serial Mode Summary

The I/O and logic functions of the CPLD and their associated interconnections are established by loading configuration data (bitstream) into the CPLD. This configuration data is loaded either automatically upon power-up, or upon issuing JTAG-command. The configuration data is stored in the internal Flash memory (Self-Boot packages only) or in the external CPLD boot PROM memory. This data is loaded from the appropriate memory depending on the state of the CPLD mode select pin (MSEL).

In Master Serial mode (when MSEL=1), the CPLD automatically loads the configuration program from an external memory i.e., CY3LV CPLD boot PROM. These PROMs have been designed for compatibility with the Master Serial Mode. This document discusses the interface between Cypress’s SRAM based CPLDs (Quantum38K and Delta39K) and CY3LV PROMs.

For more details on the other modes of configuration of these CPLDs please refer to the application note titled “Configuring Delta39K/Quantum38K.”

Controlling the CY3LV CPLD Boot PROMs During Configuration

Most connections between the CPLD device and the CY3LV boot PROM are simple and self-explanatory. *Figure 1* shows the five signal interface required between the Delta39K/Quantum38K CPLD and the CY3LV boot PROM device.

- The DATA output of the boot PROM drives DATA input of the CPLD
- The master CPLD CCLK output drives the CLK input of the boot PROM
- The CPLD CCE pin drives the $\overline{CE}$ input of the boot PROM
- The RESET/$\overline{OE}$ input of the boot PROM is driven by the CPLD RESET pin
- The READY pin of the boot PROM is connected to the RECONFIG pin of the CPLD

The READY pin is available as an open-collector indicator of the device’s RESET status; it is driven LOW while the device is in its POWER-ON RESET cycle and released (three-stated) when the cycle is complete. The rising edge of the READY (hence RECONFIG) signal causes the CPLD to start configuring. The CONFIG_DONE, CCE and RESET output of the CPLD are set LOW, CCLK is activated and CPLD starts receiving configuration data on the DATA pin. After all the configuration data is shifted in, the CPLD device deactivates the CCLK and sets CCE, RESET and CONFIG_DONE HIGH.

A HIGH level on the RESET/$\overline{OE}$ input — during CPLD reset — clears the boot PROM’s internal address pointer and subsequent reconfiguration starts at the beginning.

The $\overline{CEO}$ output of any CY3LV drives the $\overline{CE}$ input of the next CY3LV in a cascade chain of EEPROMs.

$\overline{SER\_EN}$ must be connected to V_{CC}, (except during In-System Programming).

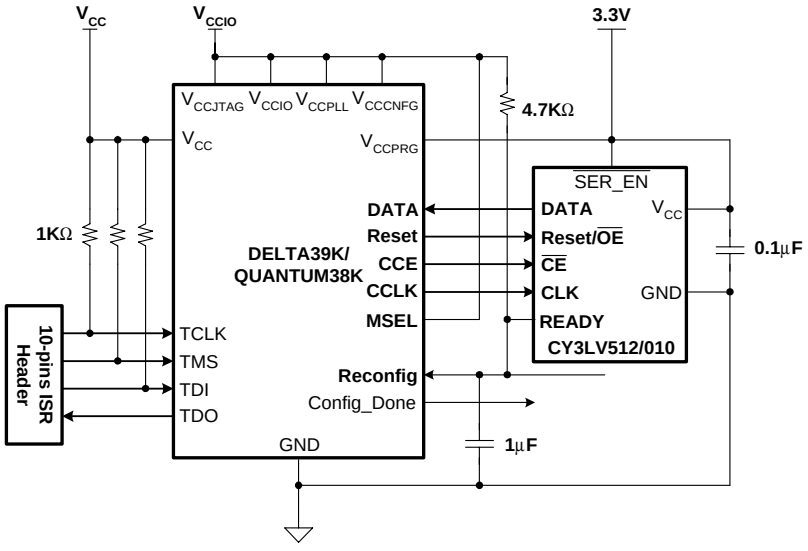


Figure 1. Interface between Delta39K/Quantum38K CPLD and CY3LV boot PROM

Note:

Currently, 3 revisions of Delta39K100 and 2 revisions of Quantum38K100 devices are available marked as CY39100Vxxx, CY39100VxxxA, and CY39100VxxxB, CY38100Vxxx, and CY38100VxxxB. *Figure 1* set-up represents the interface between CY39100VxxxB/CY38100VxxxB and CY3LV device. To get details on interface between other versions and CY3LV please refer to the application note titled "Configuring Delta39K/Quantum38K."

Setup in *Figure 1* also represents the interface between all other devices in Delta39K/Quantum38K families and CY3LV boot PROMs.

Cascading CY3LV CPLD boot PROMs

For future CPLDs requiring larger configuration memories, cascaded CPLD boot PROMs provide additional memory.

As the last bit from the first boot PROM is read, the clock signal to the boot PROM asserts its $\overline{CEO}$ output LOW and disables its DATA line driver. The second boot PROM recognizes the Low level on its $\overline{CE}$ input and enables its DATA output.

After configuration is complete, the address counters of all cascaded boot PROMs are reset if the RESET/$\overline{OE}$ on each boot PROM is driven to its active (HIGH) level.

CY3LV Series RESET Polarity

The CY3LV Series CPLD boot PROMs allow the user to program the reset polarity as either RESET/$\overline{OE}$ or RESET/OE.Cypress's SRAM based CPLDs (Delta39K and Quantum38K) require the RESET pin to be programmed active-High, i.e. as RESET/$\overline{OE}$. CY3LV boot PROMs are shipped from the factory with the reset polarity programmed active-High. This polarity can be verified using industry standard programmers or Cypress's CYDH2200E boot PROM programming kit.

Note: Every time the boot PROM is reprogrammed, care should be taken to select the reset polarity to be "HIGH" programmer software.

Programming Mode

The programming mode is entered by bringing $\overline{SER\_EN}$ LOW. In this mode the chip can be programmed by the two-wire serial bus. The programming is done at V_{CC} (3.3V nominal) supply only. The CY3LV parts are read/write at 3.3V nominal.

Standby Mode

The CY3LV enters a low-power standby mode whenever $\overline{CE}$ is asserted High. In this mode, the boot PROM consumes less than 0.5 mA of current at 3.3V with CMOS level inputs. The output remains in a high-impedance state regardless of the state of the $\overline{OE}$ input.

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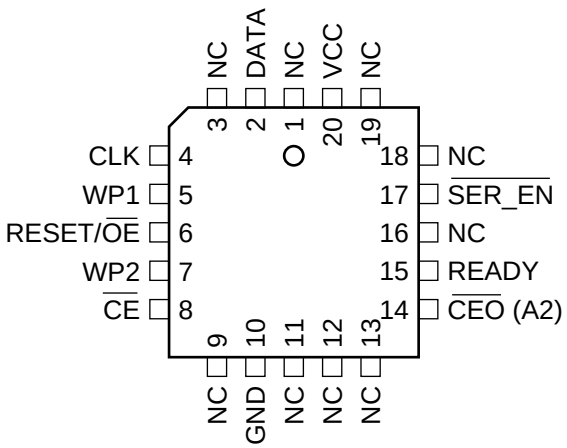
Table 1. Pin Configurations

20-pin PLCC	Name	I/O	Description
2	DATA	I/O	**Three-state DATA output for configuration.** Open-collector bidirectional pin for programming.
4	CLK	I	**Clock input.** Used to increment the internal address and bit counter for reading and programming.
5	WP1	I	**WRITE PROTECT (1).** Used to protect portions of memory during programming. Disabled by default due to internal pull-down resistor. This input pin is not used during CPLD loading operations.
6	RESET / $\overline{OE}$	I	**RESET/Output Enable input (when $\overline{SER\_EN}$ is HIGH).** A LOW level on both the $\overline{CE}$ and RESET/$\overline{OE}$ inputs enables the data output driver. A HIGH level on RESET/$\overline{OE}$ resets both the address and bit counters. The logic polarity of this input is programmable as either RESET/$\overline{OE}$ or RESET/$\overline{OE}$. Delta39K/Quantum38K CPLDs require this pin to be programmed as RESET/$\overline{OE}$ hence this document describes the pin as RESET/$\overline{OE}$.
7	WP2	I	**WRITE PROTECT (2).** Used to protect portions of memory during programming. Disabled by default due to internal pull-down resistor. This input pin is not used during CPLD loading operations.
8	CE	I	**Chip Enable input.** Used for device selection. A LOW level on both $\overline{CE}$ and $\overline{OE}$ enables the data output driver. A HIGH level on $\overline{CE}$ disables both the address and bit counters and forces the device into a low-power standby mode. Note that this pin will not enable/disable the device in the two-wire Serial Programming Mode (i.e., when $\overline{SER\_EN}$ is LOW).
10	GND		**Ground pin.** A 0.1 µF decoupling capacitor between V_{CC} and GND is recommended
14	CEO	O	**Chip Enable Output.** This signal is asserted LOW on the clock cycle following the last bit read from the memory. It will stay LOW as long as $\overline{CE}$ and $\overline{OE}$ are both LOW. It will then follow $\overline{CE}$ until $\overline{OE}$ goes HIGH. Thereafter, $\overline{CEO}$ will stay HIGH until the entire EEPROM is read again.
	A2	I	**Device selection input, A2.** This is used to enable (or select) the device during programming (i.e., when $\overline{SER\_EN}$ is LOW).
15	READY	O	**Open collector reset state indicator.** Driven LOW during power-up reset, released when power-up is complete. (Recommend a 4.7 kΩ pull-up on this pin if used).
17	$\overline{SER\_EN}$	I	Serial enable must be held High during CPLD loading operations. Bringing $\overline{SER\_EN}$ LOW enables the two-wire Serial Programming Mode.
20	VCC		+3.3V power supply pin.

Pin Configurations



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Operating Temperature ..... –55°C to +125°C

Storage Temperature ..... –65°C to +150°C

Voltage on Any Pin with Respect to Ground ..... –0.1V to V_{CC} + 0.5V

Supply Voltage (V_{CC}) ..... –0.5V to +7.0V

Maximum Soldering Temp. (10 sec. @ 1/16in.) ..... 260°C

ESD (R_{ZAP} = 1.5K, C_{ZAP} = 100 pF) 2000V

Operating Range [1]

Range	Ambient Temperature	Junction Temperature	CY3LV512/010 (V_{CC})
Commercial	0°C to + 70°C	0°C to + 90°C	3.3V ± 0.3V
Industrial	–40°C to + 85°C	–40°C to + 125°C	3.3V ± 0.3V
Military	–55°C to + 125°C	–55°C to + 130°C	3.3V ± 0.3V

3.3V Device Electrical Characteristics Over the Operating Range

Parameter	Description		Min,	Max,	Unit
V_{IH}	High-level input voltage		2.0	V_{CC}	V
V_{IL}	Low-level input voltage		0	0.8	V
V_{OH}	High-level output voltage (I_{OH} = –2.5 mA)	Commercial	2.4		V
V_{OL}	Low-level output voltage (I_{OL} = +3 mA)			0.4	V
V_{OH}	High-level output voltage (I_{OH} = –2 mA)	Industrial	2.4		V
V_{OL}	Low-level output voltage (I_{OL} = +3 mA)			0.4	V
V_{OH}	High-level output voltage (I_{OH} = –2 mA)	Military	2.4		V
V_{OL}	Low-level output voltage (I_{OL} = +2.5 mA)			0.4	V
I_{CCA}	Supply current, active mode			5	mA
I_L	Input or output leakage current (V_{IN} = V_{CC} or GND)		–10	10	µA
I_{CCS}	Supply current, standby mode	Commercial		100	µA
		Industrial/Military		100	µA

Switching Characteristics for CY3LV512/010 (3.3V) Over the Operating Range

Parameter	Description	Commercial		Industrial		Unit
		Min.	Max.	Min.	Max.	
T_{OE}[2]	$\overline{OE}$ to Data Delay		50		55	ns
T_{CE}[2]	$\overline{CE}$ to Data Delay		55		60	ns
T_{CAC}[2]	CLK to Data Delay		55		60	ns
T_{OH}	Data Hold From $\overline{CE}$, $\overline{OE}$, or CLK	0		0		ns
T_{DF}[3]	$\overline{CE}$ or $\overline{OE}$ to Data Float Delay		50		50	ns
T_{LC}	CLK Low Time	25		25		ns
T_{HC}	CLK High Time	25		25		ns
T_{SCE}	$\overline{CE}$ Setup Time to CLK (to guarantee proper counting)	30		35		ns
T_{HCE}	$\overline{CE}$ Hold Time from CLK (to guarantee proper counting)	0		0		ns
T_{HOE}	$\overline{OE}$ High Time (guarantees counter is reset)	25		25		ns
F_{MAX}	MAX Input Clock Frequency	15		10		MHz

Switching Characteristics for CY3LV512/010 (3.3V) when Cascading Over the Operating Range

Parameter	Description	Commercial		Industrial		Unit
		Min.	Max.	Min.	Max.	
t_{CDF}[3]	CLK to Data Float Delay		50		50	ns
t_{OCK}[2]	CLK to $\overline{CEO}$ Delay		50		55	ns
t_{OCE}[2]	$\overline{CE}$ to $\overline{CEO}$ Delay		35		40	ns
t_{OOE}[2]	RESET/$\overline{OE}$ to $\overline{CEO}$ Delay		35		35	ns
F_{MAX}	MAX Input Clock Frequency	12.5		10		MHz

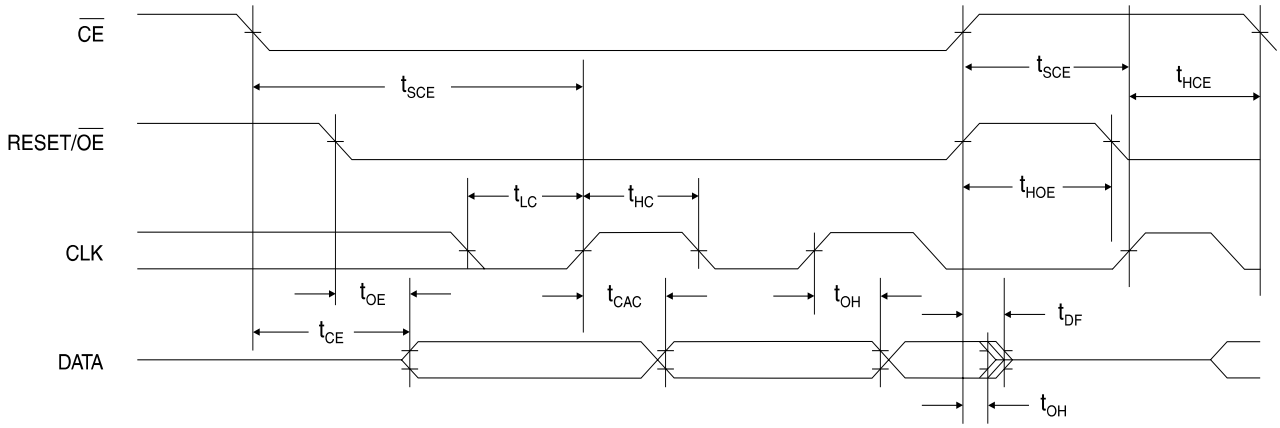
3.3V Ordering Information

Memory Size	Ordering Code	Package Name	Package Type	Operating Range
1M	CY3LV010-10JC	20J	20-Lead Plastic Leaded Chip Carrier	Commercial
	CY3LV010-10JI	20J	20-Lead Plastic Leaded Chip Carrier	Industrial
512K	CY3LV512-10JC	20J	20-Lead Plastic Leaded Chip Carrier	Commercial
	CY3LV512-10JI	20J	20-Lead Plastic Leaded Chip Carrier	Industrial

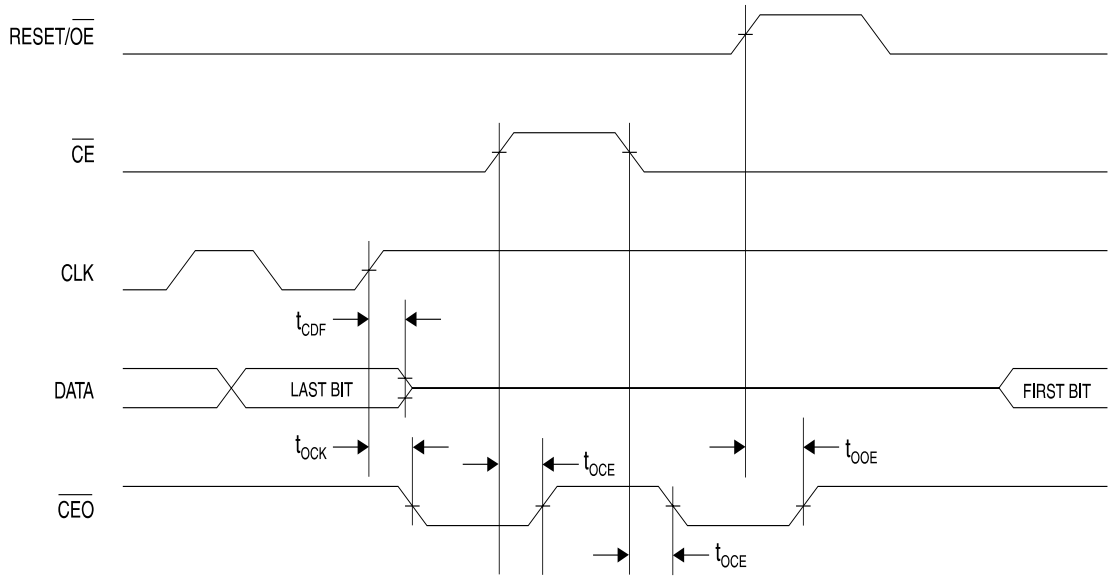
Notes:

1. The Voltage on any input or I/O pin cannot exceed the power pin during power-up.
2. AC test load = 50 pF.
3. Float delays are measured with 5 pF AC loads. Transition is measured ±200 mV from steady state active levels.

AC Characteristics

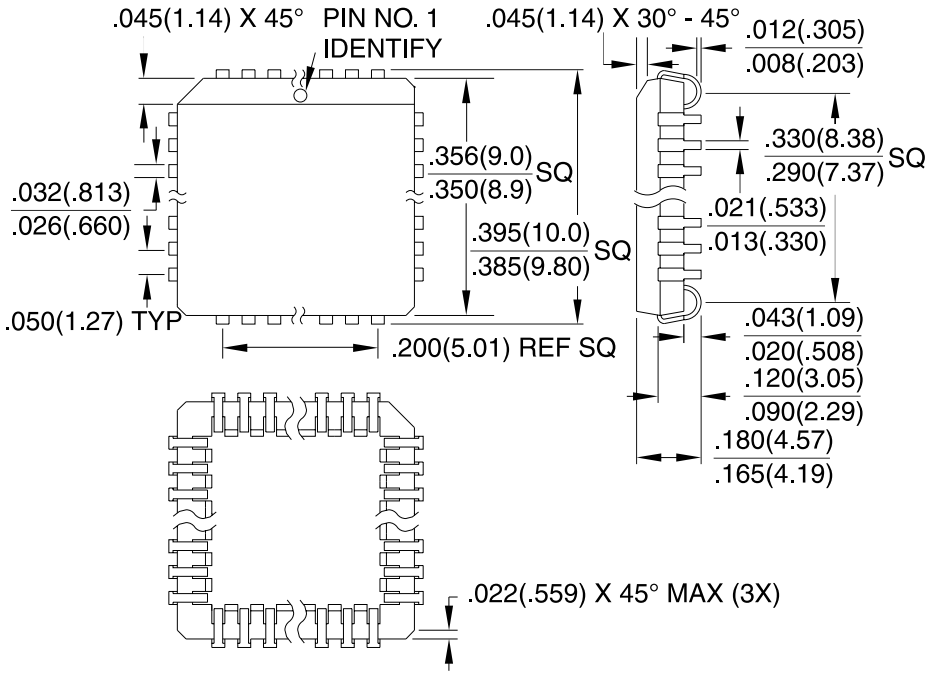


AC Characteristics when Cascading



Package Diagrams: 20J, 20-lead, Plastic J-leaded Chip Carrier (PLCC)

Dimensions in Inches and (Millimeters)



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REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	106080	08/07/01	RN	New Data Sheet
*A	122216	12/28/02	RBI	Power up requirements added to Operating Range Information