



64K x 1 SRAM
SRAM MEMORY ARRAY

AVAILABLE AS MILITARY SPECIFICATIONS

- SMD 5962-86015
- MIL-STD-883

FEATURES

- Speeds: 12, 15, 20, 25, 35, 45, 55, and 70ns
- Battery Backup: 2V data retention
- High-performance, low-power CMOS double-metal process
- Single +5V ($\pm 10\%$) Power Supply
- Easy memory expansion with CE\
- All inputs and outputs are TTL compatible

OPTIONS

• **Timing**

| | |
|-------------|------|
| 12ns access | -12 |
| 15ns access | -15 |
| 20ns access | -20 |
| 25ns access | -25 |
| 35ns access | -35 |
| 45ns access | -45* |
| 55ns access | -55* |
| 70ns access | -70* |

• **Package(s)**

| | | |
|-----------------------|---|---------|
| Ceramic DIP (300 mil) | C | No. 105 |
|-----------------------|---|---------|

• **Operating Temperature Ranges**

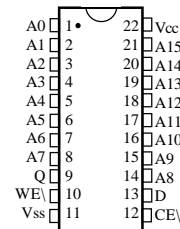
| | |
|-----------------------------|----|
| Industrial (-40°C to +85°C) | IT |
| Military (-55°C to +125°C) | XT |

- 2V data retention/low power L

*Electrical characteristics identical to those provided for the 35ns access devices.

PIN ASSIGNMENT
(Top View)

22-Pin DIP (C)
(300 MIL)



GENERAL DESCRIPTION

The Austin Semiconductor SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Austin Semiconductor SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

For flexibility in high-speed memory applications, Austin Semiconductor offers chip enable (CE\) on all organizations. This enhancement can place the outputs in High-Z for additional flexibility in system design. The X1 configuration features separate data input and output.

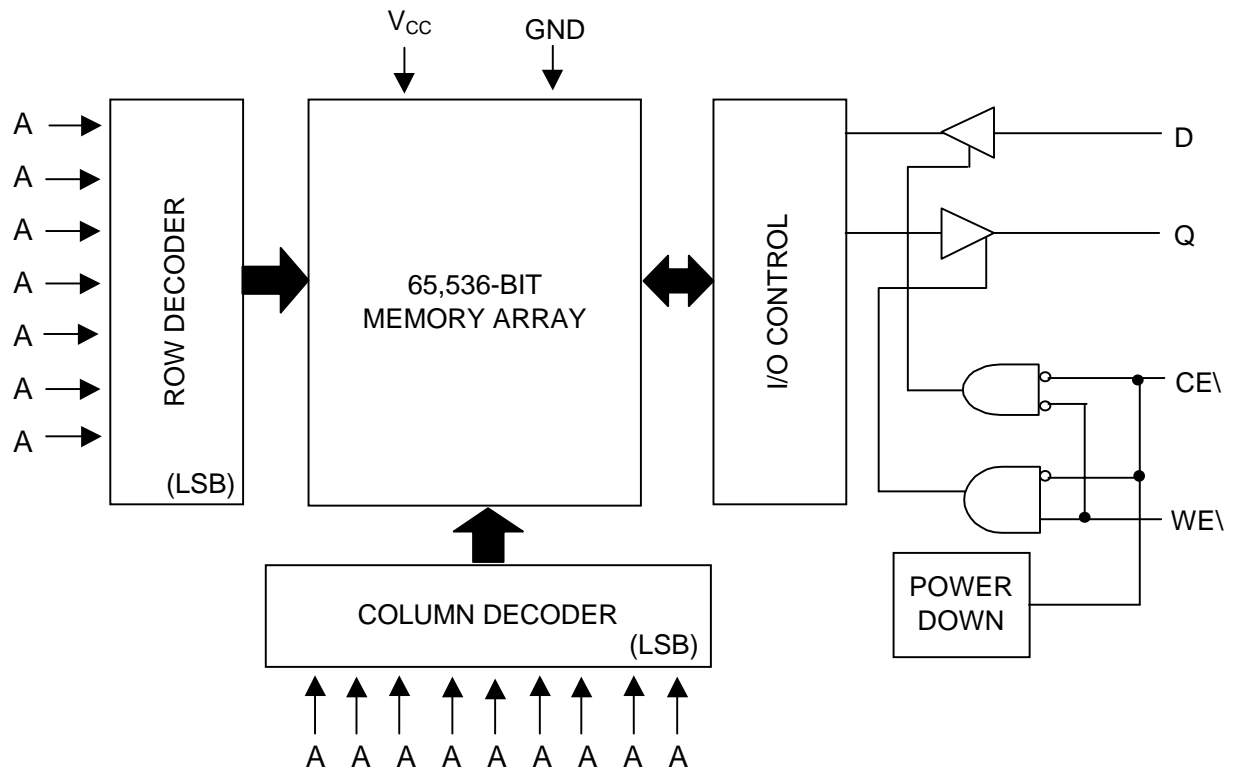
Writing to these devices is accomplished when write enable (WE\) and CE\ inputs are both LOW. Reading is accomplished when WE\ remains HIGH and CE\ goes LOW. The device offers a reduced power standby mode when disabled. This allows system designs to achieve low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

**For more products and information
please visit our web site at
www.austinsemiconductor.com**



FUNCTIONAL BLOCK DIAGRAM



TRUTHTABLE

| MODE | CE\ | WE\ | DQ | POWER |
|---------|-----|-----|--------|---------|
| STANDBY | H | X | HIGH-Z | STANDBY |
| READ | L | H | Q | ACTIVE |
| WRITE | L | L | HIGH-Z | ACTIVE |



ABSOLUTE MAXIMUM RATINGS*

| | |
|---|-----------------|
| Voltage on any Input Relative to V _{SS} | -2.0V to +7.0V |
| Voltage on V _{CC} Supply Relative to V _{SS} | -1.0V to +7.0V |
| Voltage Applied to Q..... | -1.0V to +7.0V |
| Storage Temperature..... | -65°C to +150°C |
| Power Dissipation..... | 1W |
| Max Junction Temperature..... | +175°C |
| Lead Temperature (soldering 10 seconds)..... | +260°C |
| Short Circuit Output Current..... | 50mA |

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(-55°C ≤ T_C ≤ 125°C; V_{CC} = 5V ±10%)

| DESCRIPTION | CONDITIONS | SYM | MIN | MAX | UNITS | NOTES |
|------------------------------|---|-----------------|------|-----------------------|-------|-------|
| Input High (Logic 1) Voltage | | V _{IH} | 2.2 | V _{CC} +1.0V | V | 1 |
| Input Low (Logic 0) Voltage | | V _{IL} | -0.5 | 0.8 | V | 1, 2 |
| Input Leakage Current | 0V ≤ V _{IN} ≤ V _{CC} | I _{LI} | -10 | 10 | μA | |
| Output Leakage Current | Outputs Disabled 0V ≤ V _{OUT} ≤ V _{CC} | I _{LO} | -10 | 10 | μA | |
| Output High Voltage | I _{OH} = -4.0mA | V _{OH} | 2.4 | --- | V | 1 |
| Output Low Voltage | I _{OL} = 8.0mA | V _{OL} | --- | 0.4 | V | 1 |

| PARAMETER | CONDITIONS | SYM | MAX | | | | | UNITS | NOTES |
|---------------------------------|---|-------------------|-----|-----|-----|-----|-----|-------|-------|
| | | | -12 | -15 | -20 | -25 | -35 | | |
| Power Supply Current: Operating | CE \ ≤ V _{IL} ; V _{CC} = MAX Output Open | I _{CC} | 140 | 125 | 110 | 100 | 90 | mA | 3 |
| Power Supply Current: Standby | CE \ ≥ V _{IH} ; V _{CC} = MAX f = 1/t _{RC} (MIN) Hz | I _{SBT1} | 45 | 41 | 36 | 33 | 30 | mA | |
| | CE \ ≥ V _{IH} ; All Other Inputs ≤ V _{IL} or ≥ V _{IH} , V _{CC} = MAX f = 0 Hz | I _{SBT2} | 25 | 25 | 25 | 25 | 25 | mA | |
| | CE \ ≥ (V _{CC} - 0.2); V _{CC} = MAX All Other Inputs ≤ 0.2V or ≥ (V _{CC} - 0.2V), f = 0 Hz | I _{SBC2} | 5 | 5 | 5 | 5 | 5 | mA | |

CAPACITANCE

| DESCRIPTION | CONDITIONS | SYM | MAX | UNITS | NOTES |
|--------------------|---|----------------|-----|-------|-------|
| Input Capacitance | T _A = 25°C, f = 1MHz V _{CC} = 5V | C _I | 6 | pF | 4 |
| Output Capacitance | | C _O | 7 | pF | 4 |



ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) ($-55^{\circ}\text{C} \leq T_c \leq 125^{\circ}\text{C}$; $V_{cc} = 5V \pm 10\%$)

| DESCRIPTION | SYMBOL | -12 | | -15 | | -20 | | -25 | | -35 | | UNITS | NOTES |
|----------------------------------|------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-------|-------|
| | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | | |
| READ CYCLE | | | | | | | | | | | | | |
| READ cycle time | t_{RC} | 12 | | 15 | | 20 | | 25 | | 35 | | ns | |
| Address access time | t_{AA} | | 12 | | 15 | | 20 | | 25 | | 35 | ns | |
| Chip Enable access time | t_{ACE} | | 10 | | 13 | | 15 | | 20 | | 25 | ns | |
| Output hold from address change | t_{OH} | 2 | | 2 | | 2 | | 2 | | 2 | | ns | |
| Chip Enable to output in Low-Z | t_{LZCE} | 2 | | 2 | | 2 | | 2 | | 2 | | ns | 7 |
| Chip disable to output in High-Z | t_{HZCE} | | 7 | | 8 | | 10 | | 12 | | 15 | ns | 6, 7 |
| Chip Enable to power-up time | t_{PU} | 0 | | 0 | | 0 | | 0 | | 0 | | ns | |
| Chip disable to power-down time | t_{PD} | | 12 | | 15 | | 20 | | 25 | | 35 | ns | |
| WRITE CYCLE | | | | | | | | | | | | | |
| WRITE cycle time | t_{WC} | 12 | | 15 | | 20 | | 25 | | 35 | | ns | |
| Chip Enable to end of write | t_{CW} | 10 | | 12 | | 15 | | 20 | | 25 | | ns | |
| Address valid to end of write | t_{AW} | 10 | | 12 | | 15 | | 20 | | 25 | | ns | |
| Address setup time | t_{AS} | 0 | | 0 | | 0 | | 0 | | 0 | | ns | |
| Address hold from end of write | t_{AH} | 0 | | 0 | | 0 | | 0 | | 0 | | ns | |
| WRITE pulse width | t_{WP} | 10 | | 12 | | 15 | | 20 | | 25 | | ns | |
| Data setup time | t_{DS} | 7 | | 8 | | 10 | | 12 | | 15 | | ns | |
| Data hold time | t_{DH} | 0 | | 0 | | 0 | | 0 | | 0 | | ns | |
| Write disable to output in Low-Z | t_{LZWE} | 2 | | 2 | | 2 | | 2 | | 2 | | ns | 7 |
| Write Enable to output in High-Z | t_{HZWE} | 0 | 6 | 0 | 7 | 0 | 8 | 0 | 10 | 0 | 15 | ns | 6, 7 |



ACTEST CONDITIONS

| | |
|-------------------------------------|-------------------------|
| Input pulse levels | V _{ss} to 3.0V |
| Input rise and fall times | 5ns |
| Input timing reference levels | 1.5V |
| Output reference levels | 1.5V |
| Output load | See Figures 1 and 2 |

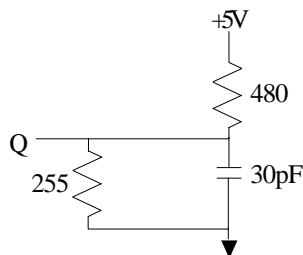


Fig. 1 Output Load Equivalent

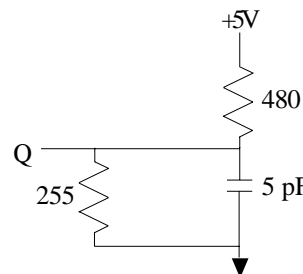


Fig. 2 Output Load Equivalent

NOTES

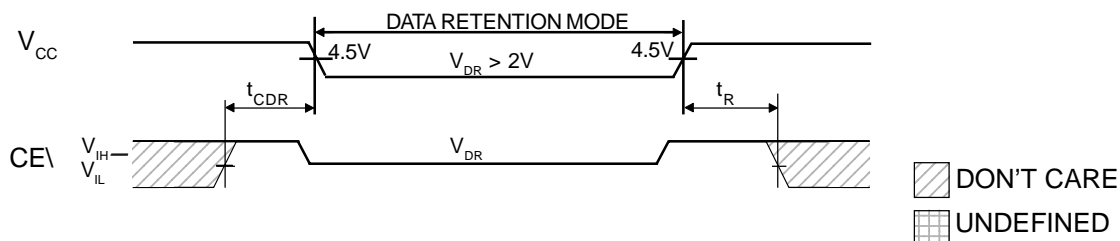
- All voltages referenced to V_{ss} (GND).
- 3V for pulse width < 20ns
- I_{CC} is dependent on output loading and cycle rates. The specified value applies with the outputs unloaded, and $f = \frac{1}{RC (MIN)}$ Hz.
- This parameter is sampled.
- Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
- t_{HZCE} and t_{HZWE} are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV typical from steady state voltage, allowing for actual tester RC time constant.

- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, and t_{HZWE} is less than t_{LZWE}.
- WE\ is HIGH for READ cycle.
- Device is continuously selected. Chip enable is held in its active state.
- Address valid prior to, or coincident with, latest occurring chip enable.
- RC = READ Cycle Time.
- Chip enable (CE\) and write enable (WE\) can initiate and terminate a WRITE cycle.

DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

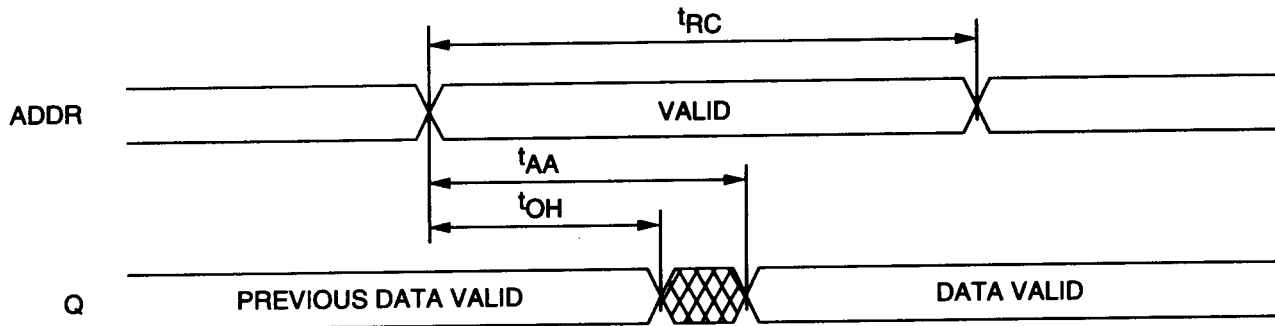
| DESCRIPTION | CONDITIONS | SYM | MIN | MAX | UNITS | NOTES |
|--------------------------------------|---|---|-----------------|-----|-------|-------|
| V _{CC} for Retention Data | | V _{DR} | 2 | --- | V | |
| Data Retention Current | CE\ ≥ (V _{CC} - 0.2V) V _{IN} ≥ (V _{CC} - 0.2V) or ≤ 0.2V | V _{CC} = 2V I _{CCDR} | --- | 300 | μA | |
| | | V _{CC} = 3V I _{CCDR} | --- | 500 | μA | |
| Chip Deselect to Data Retention Time | | t _{CDR} | 0 | --- | ns | 4 |
| Operation Recovery Time | | t _R | t _{RC} | --- | ns | 4, 11 |

LOW V_{CC} DATA RETENTION WAVEFORM

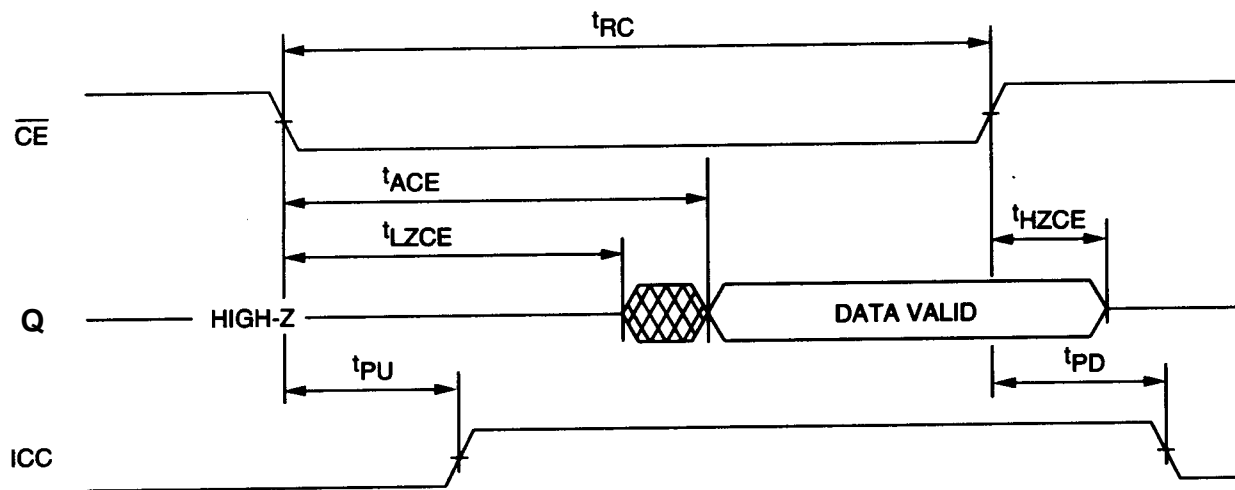




READ CYCLE NO. 1 ^{8,9}



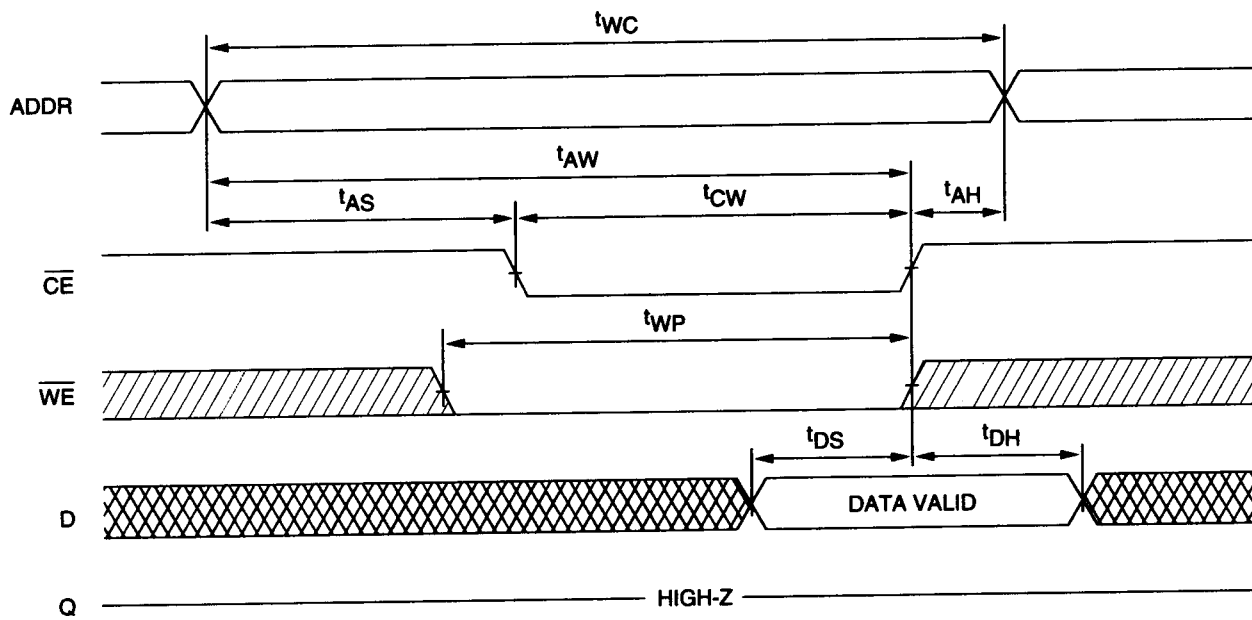
READ CYCLE NO. 2 ^{7,8,10}



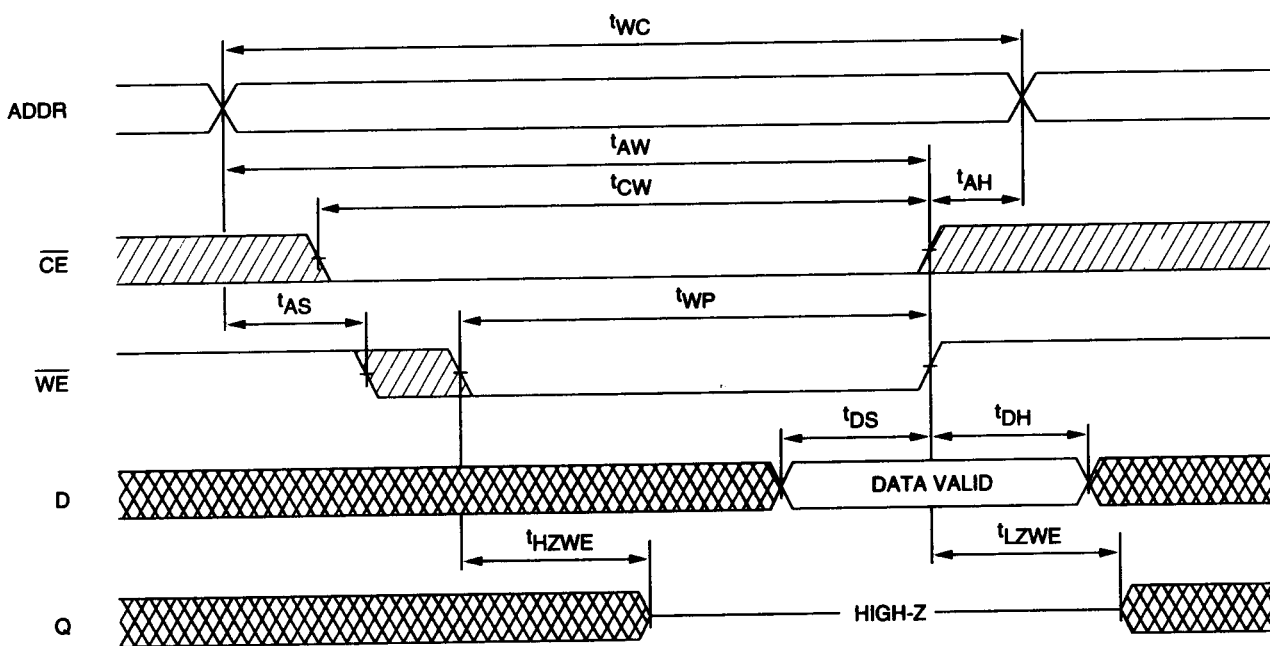
DON'T CARE
 UNDEFINED



WRITE CYCLE NO. 1 ¹²
(Chip Enabled Controlled)



WRITE CYCLE NO. 2 ^{7, 12, 13}
(Write Enabled Controlled)

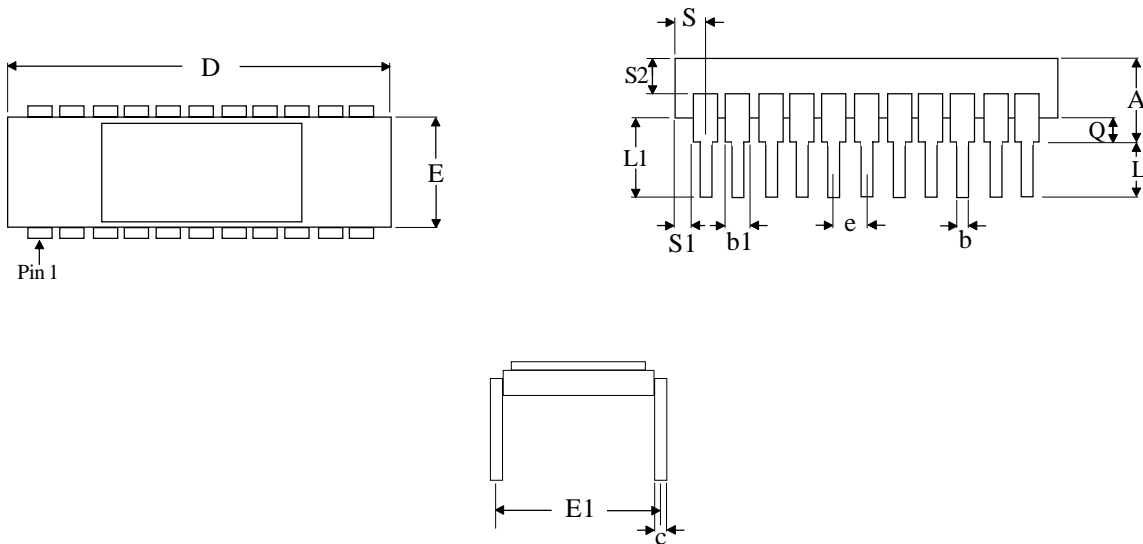


DON'T CARE
 UNDEFINED



MECHANICAL DEFINITIONS*

ASI Case #105 (Package Designator C)
SMD 5962-86015, Case Outline X



| SYMBOL | SMD SPECIFICATIONS | |
|--------|--------------------|-------|
| | MIN | MAX |
| A | --- | 0.200 |
| b | 0.014 | 0.023 |
| b1 | 0.030 | 0.065 |
| c | 0.008 | 0.015 |
| D | --- | 1.260 |
| E | 0.220 | 0.310 |
| E1 | 0.290 | 0.320 |
| e | 0.100 BSC | |
| L | 0.125 | 0.200 |
| L1 | 0.150 | --- |
| Q | 0.015 | 0.060 |
| S | --- | 0.080 |
| S1 | 0.005 | --- |
| S2 | 0.005 | --- |

NOTE: These dimensions are per the SMD. ASI's package dimensional limits may differ, but they will be within the SMD limits.

* All measurements are in inches.



ORDERING INFORMATION

EXAMPLE: MT5C6401C-45L/883C

| Device Number | Package Type | Speed ns | Options** | Process |
|---------------|--------------|----------|-----------|---------|
| MT5C6401 | C | -12 | L | /* |
| MT5C6401 | C | -15 | L | /* |
| MT5C6401 | C | -20 | L | /* |
| MT5C6401 | C | -25 | L | /* |
| MT5C6401 | C | -35 | L | /* |
| MT5C6401 | C | -45 | L | /* |
| MT5C6401 | C | -55 | L | /* |
| MT5C6401 | C | -70 | L | /* |

*AVAILABLE PROCESSES

IT = Industrial Temperature Range

-40°C to +85°C

XT = Extended Temperature Range

-55°C to +125°C

883C = Full Military Processing

-55°C to +125°C

** OPTIONS

L = 2V Data Retention/Low Power



**ASI TO DSCC PART NUMBER
CROSS REFERENCE***

ASI Package Designator C

SMD 5962-86015

| ASI Part # | SMD Part # |
|--------------------|-------------------|
| MT5C6801C-35/883C | 5962-8601501XA |
| MT5C6801C-35L/883C | 5962-8601502XA |
| MT5C6801C-45/883C | 5962-8601503XA |
| MT5C6801C-45L/883C | 5962-8601504XA |
| MT5C6801C-55/883C | 5962-8601505XA |
| MT5C6801C-55L/883C | 5962-8601506XA |

* ASI part number is for reference only. Orders received referencing the SMD part number will be processed per the SMD.