



## Nine Output 3.3V Buffer

### Features

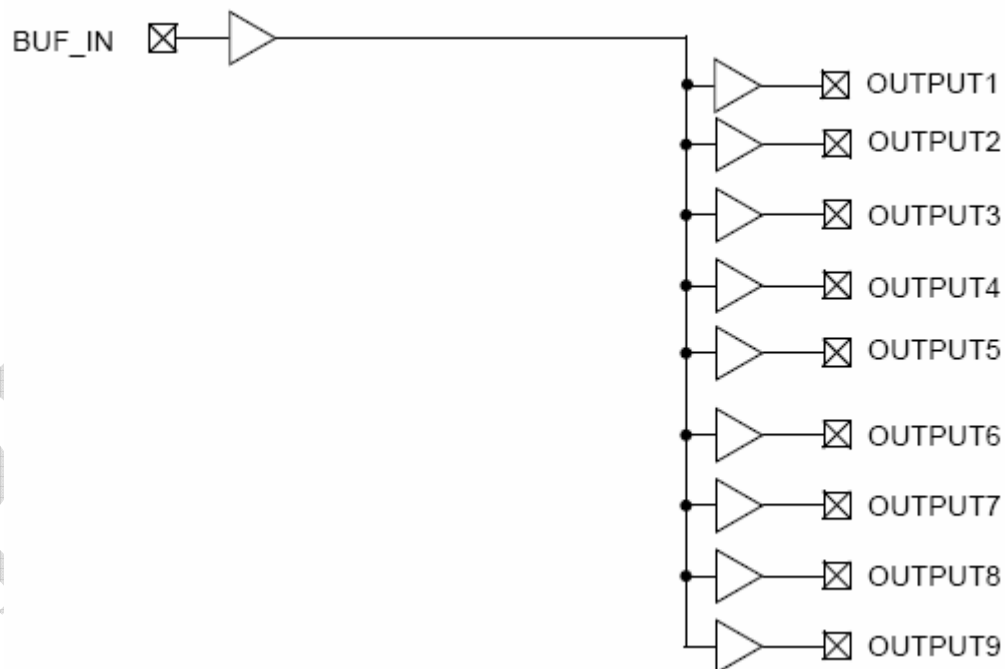
- One-input to Nine-Output Buffer/Driver
- Supports two DIMMs or four SO-DIMMs with one additional output for feedback to an external or chipset PLL
- Low power consumption for mobile applications  
Less than 32 mA at 66.6 MHz with unloaded outputs
- 1nS Input-Output delay
- Buffers all frequencies from DC to 133.33 MHz
- Output-output skew less than 250pS
- Multiple  $V_{DD}$  and  $V_{SS}$  pins for noise and electromagnetic interference (EMI) reduction
- Space-saving 16-pin 150-mil SOIC Package
- 3.3V operation
- Commercial and Industrial temperature parts are available

### Functional Description

The ASM2P2309NZ is a low-cost buffer designed to distribute high-speed clocks in mobile PC systems and desktop PC systems with SDRAM support. The part has nine outputs, eight of which can be used to drive two DIMMs or four SO-DIMMs, and the remaining can be used for external feedback to a PLL. The device operates at 3.3V and outputs can run up to 133.33 MHz.

The ASM2P2309NZ is designed for low EMI and power optimization. It has multiple  $V_{SS}$  and  $V_{DD}$  pins for noise optimization and consumes less than 32 mA at 66.6 MHz, making it ideal for the low-power requirements of mobile systems. It is available in an ultra-compact 150-mil 16-pin SOIC package.

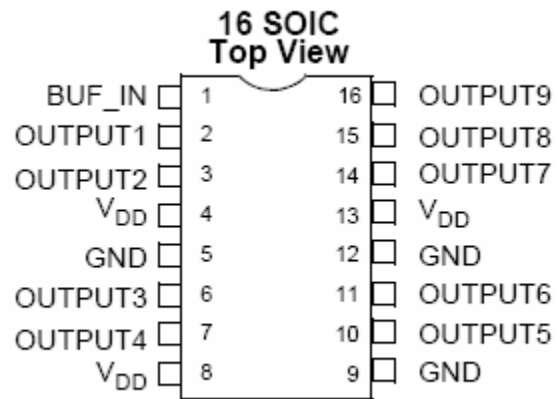
### Block Diagram





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## Pin Configuration for ASM2P2309NZ



## Pin Description for ASM2P2309NZ

Pin	Signal	Description
4, 8, 13	V <sub>DD</sub>	3.3V Digital Voltage Supply
5, 9, 12	GND	Ground
1	BUF_IN	Input Clock
2, 3, 6, 7, 10, 11, 14, 15, 16	OUTPUT [1:9]	Outputs



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### Absolute Maximum Ratings

Parameter	Min	Max	Unit
Supply Voltage to Ground Potential	-0.5	7.0	V
DC Input Voltage (Except REF)	-0.5	$V_{DD} + 0.5$	V
DC Input Voltage (REF)	-0.5	0.7	V
Storage Temperature	-65	+150	°C
Junction Temperature		150	°C
Static Discharge Voltage (As per JEDEC STD 22- A114-B)		>2000	V

Note: These are stress ratings only and functional usage is not implied. Exposure to absolute maximum ratings for prolonged periods can affect device reliability.

### Operating Conditions

Parameter	Description	Min	Max	Unit
$V_{DD}$	Supply Voltage	3.0	3.6	V
$T_A$	(Ambient Operating Temperature), Commercial	0	70	°C
	(Ambient Operating Temperature), Industrial	-40	85	°C
$C_L$	Load Capacitance, $F_{out} < 100$ MHz	-	30	pF
	Load Capacitance, $100$ MHz $< F_{out} < 133.33$ MHz	-	15	pF
$C_{IN}$	Input Capacitance	-	7	pF
BUF_IN, OUTPUT [1:9]	Operating Frequency	DC	133.33	MHz
$t_{PU}$	Power-up time for all $V_{DD}$ 's to reach minimum specified voltage (power ramps must be monotonic)	0.05	50	mS



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## Electrical Characteristics for Commercial and Industrial Temperature Devices

Parameter	Description	Test Conditions	Min.	Max.	Unit
$V_{IL}$	Input LOW Voltage <sup>1</sup>		-	0.8	V
$V_{IH}$	Input HIGH Voltage <sup>1</sup>		2.0	-	V
$I_{IL}$	Input LOW Current	$V_{IN} = 0V$	-	50.0	$\mu A$
$I_{IH}$	Input HIGH Current	$V_{IN} = V_{DD}$	-	100.0	$\mu A$
$V_{OL}$	Output LOW Voltage <sup>2</sup>	$I_{OL} = 8\text{ mA}$	-	0.4	V
$V_{OH}$	Output HIGH Voltage <sup>2</sup>	$I_{OH} = -8\text{ mA}$	2.4	-	V
$I_{DD}$	Supply Current	Unloaded outputs at 66.66 MHz	-	32	mA

Switching Characteristics for Commercial and Industrial Temperature Devices<sup>3</sup>

Parameter	Name	Description	Min.	Typ.	Max.	Unit
$t_D$	Duty Cycle <sup>2</sup> = $t_2 \div t_1$	Measured at 1.4V	40.0	50.0	60.0	%
$t_3$	Rise Time <sup>2</sup>	Measured between 0.8V and 2.0V	-	-	1.50	nS
$t_4$	Fall Time <sup>2</sup>	Measured between 0.8V and 2.0V	-	-	1.50	nS
$t_5$	Output to Output Skew <sup>2</sup>	All outputs equally loaded	-	-	250	pS
$t_6$	Propagation Delay, BUF_IN Rising Edge to OUTPUT Rising Edge <sup>2</sup>	Measured at $V_{DD}/2$	1	5	9.2	nS

Note:

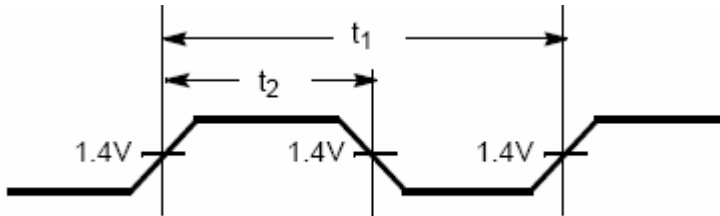
1. BUF\_IN input has a threshold voltage of  $V_{DD}/2$ .
2. Parameter is guaranteed by design and characterization. It is not 100% tested in production.
3. All parameters specified with loaded outputs.



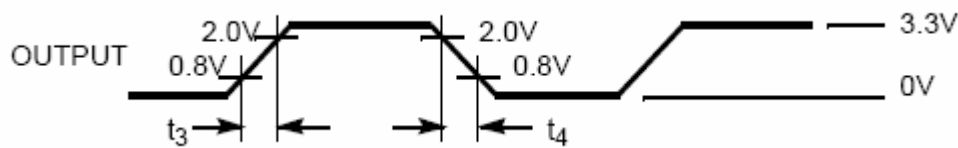
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### Switching Waveforms

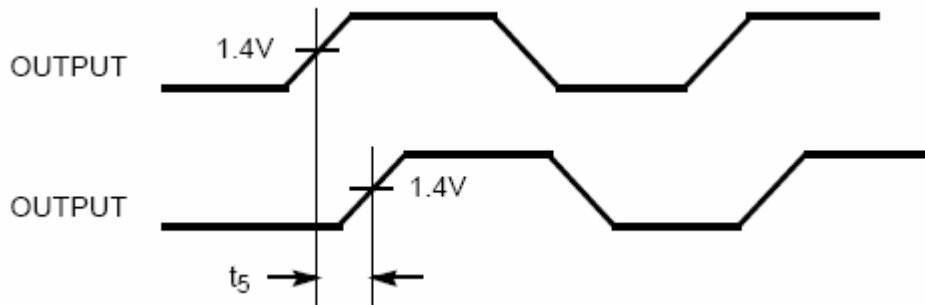
#### Duty Cycle Timing



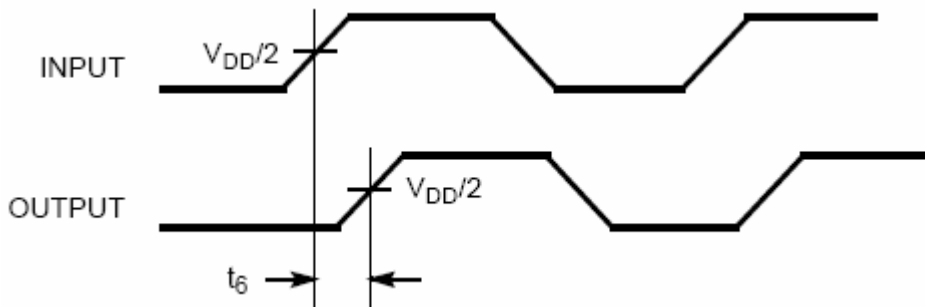
#### All Outputs Rise/Fall Time



#### Output-Output Skew



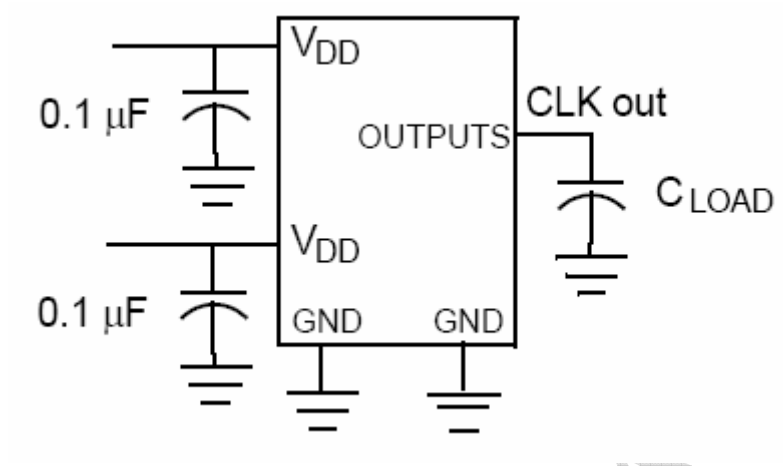
#### Input-Output Propagation Delay





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Test Circuits



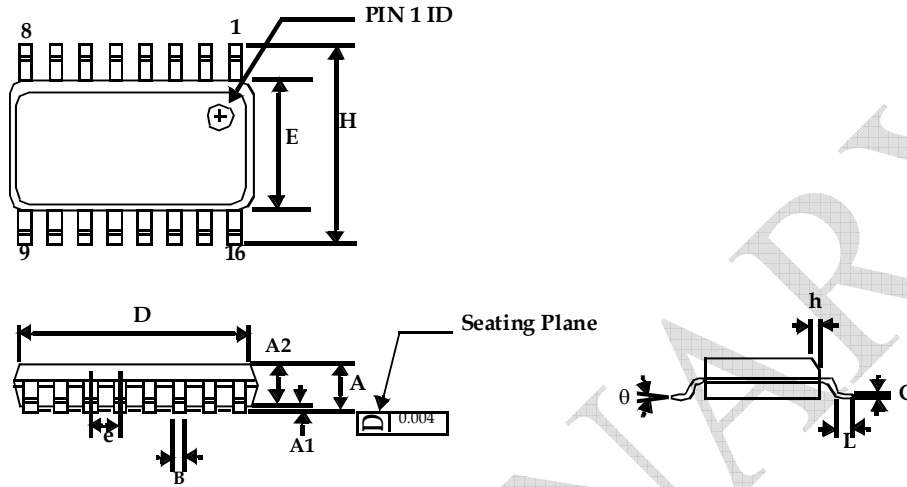
PRELIMINARY



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Package Information

16-lead (150 Mil) Molded SOIC Package



Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
A2	0.049	0.059	1.25	1.50
B	0.013	0.022	0.33	0.53
C	0.008	0.012	0.19	0.27
D	0.386	0.394	9.80	10.01
E	0.150	0.157	3.80	4.00
e	0.050 BSC		1.27 BSC	
H	0.228	0.244	5.80	6.20
h	0.010	0.016	0.25	0.41
L	0.016	0.035	0.40	0.89
θ	0°	8°	0°	8°



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Ordering Codes

Part Number	Marking	Package Type	Operating Range
ASM5P2309NZF-08-ST	5P2309NZF	16-pin 150-mil SOIC, Pb Free	Commercial
ASM5P2309NZF-08-SR	5P2309NZF	16-pin 150-mil SOIC, Tape and Reel, Pb Free	Commercial
ASM5I2309NZF-08-ST	5I2309NZF	16-pin 150-mil SOIC, Pb Free	Industrial
ASM5I2309NZF-08-SR	5I2309NZF	16-pin 150-mil SOIC, Tape and Reel, Pb Free	Industrial
ASM5P2309NZG-08-ST	5P2309NZG	16-pin 150-mil SOIC, Green	Commercial
ASM5P2309NZG-08-SR	5P2309NZG	16-pin 150-mil SOIC, Tape and Reel, Green	Commercial
ASM5I2309NZG-08-ST	5I2309NZG	16-pin 150-mil SOIC, Green	Industrial
ASM5I2309NZG-08-SR	5I2309NZG	16-pin 150-mil SOIC, Tape and Reel, Green	Industrial

Device Ordering Information

A S M 2 P 2 3 0 9 N Z F - 1 6 - S R

R = Tape & reel, T = Tube or Tray

O = SOT	U = MSOP
S = SOIC	E = TQFP
T = TSSOP	L = LQFP
A = SSOP	U = MSOP
V = TVSOP	P = PDIP
B = BGA	D = QSOP
Q = QFN	X = SC-70

DEVICE PIN COUNT

F = LEAD FREE AND RoHS COMPLIANT PART  
G = GREEN PACKAGE

PART NUMBER

X= Automotive (-40C to +125C)	I= Industrial (-40C to +85C)	P or n/c = Commercial (0C to +70C)
1 = Reserved	6 = Power Management	
2 = Non PLL based	7 = Power Management	
3 = EMI Reduction	8 = Power Management	
4 = DDR support products	9 = Hi Performance	
5 = STD Zero Delav Buffer	0 = Reserved	

ALLIANCE SEMICONDUCTOR MIXED SIGNAL PRODUCT

Licensed under US patent #5,488,627, #6,646,463 and #5,631,920.





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Note: This product utilizes US Patent # 6,646,463 Impedance Emulator Patent issued to Alliance Semiconductor, dated 11-11-2003

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