



**DUAL EPAD® PRECISION HIGH SLEW RATE CMOS OPERATIONAL AMPLIFIER**

**KEY FEATURES**

- Factory pre-trimmed  $V_{OS}$
- $V_{OS} = 25\mu V @ I_{OS} = 0.01pA$
- 5 V /  $\mu s$  slew rate
- EPAD ( Electrically Programmable Analog Device)
- Rail-to-rail input/output
- Each amplifier  $V_{OS}$  can be user trimmed to a different  $V_{OS}$  level (optional)
- System level “calibration” capable

**GENERAL DESCRIPTION**

The ALD2724E/ALD2724 is a dual monolithic operational amplifier with MOSFET input that has rail-to-rail input and output voltage ranges. The input voltage range and output voltage range are very close to the positive and negative power supply voltages. Typically the input voltage can be beyond positive power supply voltage  $V^+$  or the negative power supply voltage  $V^-$  by up to 300mV. The output voltage swings to within 60mV of either positive or negative power supply voltages at rated load.

With high impedance load, the output voltage of the ALD2724E/ALD2724 approaches within 1mV of the power supply rails. This device is designed as an alternative to the popular J-FET input operational amplifier in applications where lower operating voltages, such as 9V battery or  $\pm 3.25V$  to  $\pm 5V$  power supplies are being used. The ALD2724E/ALD2724 offers high slew rate of 5.0V/ $\mu s$ .

The rail-to-rail input and output feature of the ALD2724E/ALD2724 expands signal voltage range for a given operating supply voltage and allows numerous analog serial stages to be implemented without losing operating voltage margin. The output stage is designed to drive up to 10mA into 400pF capacitive and 1.5K $\Omega$  resistive loads at unity gain and up to 4000pF at a gain of 5. Short circuit protection to either ground or the power supply rails is at approximately 15mA clamp current. Due to complementary output stage design, the output can source and sink 10mA into a load with symmetrical drive and is ideally suited for applications where push-pull voltage drive is desired.

For each of the operational amplifier, the offset voltage is trimmed on-chip to eliminate the need for external nulling in many applications. For precision applications, the output is designed to settle to 0.1% in 2 $\mu s$ . In large signal buffer applications, the operational amplifier can function as

**ORDERING INFORMATION**

Operating Temperature Range		
-55°C to +125°C	0°C to +70°C	0°C to +70°C
14-Pin CERDIP Package	14-Pin Small Outline Package (SOIC)	14-Pin Plastic Dip Package
ALD2724E DB	ALD2724E SB	ALD2724E PB
ALD2724 DB	ALD2724 SB	ALD2724 PB

\* Contact factory for industrial temperature range

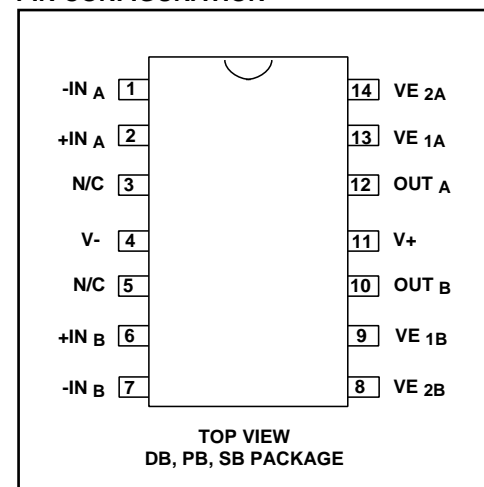
**BENEFITS**

- Ready to use off the shelf standard part
- Custom automated trimming optional
- Remote controlled automated trimming
- In-System Programming capable
- No external components
- No internal clocking noise source
- Simple and cost effective
- Small package size
- Extremely small total functional volume size
- Low system implementation cost

**APPLICATIONS**

- Sensor interface circuits
- Transducer biasing circuits
- Capacitive and charge integration circuits
- Biochemical probe interface
- Signal conditioning
- Portable instruments
- High source impedance electrode amplifiers
- Precision Sample and Hold amplifiers
- Precision current to voltage converter
- Error correction circuits
- Sensor compensation circuits
- Precision gain amplifiers
- Periodic In-system calibration
- System output level shifter

**PIN CONFIGURATION**



## GENERAL DESCRIPTION (cont'd)

an ultra-high input impedance voltage follower/buffer that allows input and output voltage swings from positive to negative supply voltages. This feature is intended to greatly simplify systems design and eliminate higher voltage power supplies in many applications.

Each ALD2724E/ALD2724 operational amplifier features individual, user-programmable offset voltage trimming resulting in significantly enhanced total system performance and user flexibility. EPAD technology is an exclusive ALD design which has been refined for analog applications where precision voltage trimming is necessary to achieve a desired performance. It utilizes CMOS FETs as in-circuit elements for trimming of offset voltage bias characteristics with the aid of a personal computer under software control. Once programmed, the set parameters are stored indefinitely. EPAD offers the circuit designer a convenient and cost-effective trimming solution for achieving the very highest amplifier/system performance.

## FUNCTIONAL DESCRIPTION

The ALD2724E/ALD2724 utilizes EPADs as in-circuit elements for trimming of offset voltage bias characteristics. Each ALD2724E/ALD2724 operational amplifier has a pair of EPAD-based circuits connected such that one circuit is used to adjust  $V_{OS}$  in one direction and the other circuit is used to adjust  $V_{OS}$  in the other direction. While each of the basic EPAD device is a monotonically adjustable (offset voltage trimming) programmable device, the  $V_{OS}$  of the ALD2724E can be adjusted many times in both directions. Once programmed, the set  $V_{OS}$  levels are stored permanently, even when the device power is removed.

### Functional Description of ALD2724E/ALD2724

The ALD2724E is pre-programmed at the factory under standard operating conditions for minimum equivalent input offset voltage. It also has a guaranteed offset voltage program range, which is ideal for applications that require electrical offset voltage programming.

The ALD2724E is an operational amplifier that can be trimmed stand-alone, with user application-specific programming or in-system programming conditions. User application-specific circuit programming refers to a situation where the Total Input Offset Voltage of the ALD2724E can be trimmed with the actual intended operating conditions.

Take the example of an application circuit that uses +5V and -5V power supplies, an operational amplifier input biased at +1V, and an average operating temperature at +85°C; the circuit can be wired up to these conditions within an environmental chamber with the ALD2724E inserted into a test socket while it is being electrically trimmed. Any error in  $V_{OS}$  due to these bias conditions can be automatically zeroed out. The Total  $V_{OS}$  error,  $V_{OST}$ , is now limited only by the adjustable range and the stability of  $V_{OS}$ , and the input noise voltage of the operational amplifier. This Total Input Offset Voltage now includes  $V_{OS}$ , as  $V_{OS}$  is traditionally specified; plus the  $V_{OS}$  error contributions from PSRR, CMRR,  $TCV_{OS}$ , and noise. Typically,  $V_{OST}$  ranges approximately  $\pm 25\mu V$  for the ALD2724E.

In-System Programming refers to the condition where the EPAD adjustment is made after the ALD2724E has been

inserted into a circuit board. In this case, the circuit design must provide for the ALD2724E to operate in both normal mode and in programming mode. One of the benefits of in-system programming is that not only the ALD2724E offset voltage from operating bias conditions has been accounted for, any residual errors introduced by other circuit components, such as resistor or sensor induced voltage errors, can also be programmed and corrected. In this way, the "in-system" circuit output can be adjusted to a desired level eliminating need for another trimming function.

The ALD2724 is pre-programmed at the factory under standard operating conditions for minimum equivalent input offset voltage. The ALD2724 offers similar programmable features as the ALD2724E, but with more limited offset voltage program range. It is intended for standard operational amplifier applications where little or no electrical programming by the user is necessary.

## USER PROGRAMMABLE $V_{OS}$ FEATURE

Each ALD2724E/ALD2724 has four additional pins, compared to a conventional dual operational amplifier which has eight pins. These four additional pins are named VE1A, VE2A for op amp A and VE1B, VE2B for op amp B. Each of these pins VE1A, VE2A, VE1B, VE2B (represented by VExx) are connected to a separate, internal offset bias circuit. VExx pins have initial internal bias voltage values of approximately 1 to 2 Volts. The voltage on these pins can be programmed using the ALD E100 EPAD Programmer and the appropriate Adapter Module. The useful programming range of voltages on VExx pins are 1 Volt to 4 Volts.

VExx pins are programming pins, used during electrical programming mode to inject charge into the internal EPADs. Increasing voltage on VE1A/VE1B decreases the offset voltage whereas increasing voltage on VE2A/VE2B increases the offset voltage of op amp A and op amp B, respectively.

During programming, voltages on VExx pins are increased incrementally to program the offset voltage of the operational amplifier to the desired  $V_{OS}$ . Note that desired  $V_{OS}$  can be any value within the offset voltage programmable ranges, and can be either equal zero, a positive value or a negative value. This  $V_{OS}$  value can also be reprogrammed to a different value at a later time, provided that the useful VE1x or VE2x programming voltage range has not been exceeded. The injected charge is then permanently stored. After programming, VExx pins must be left open in order for these voltages to remain at the programmed levels.

Internally, VE1 and VE2 are programmed and connected differentially. Temperature drift effects between the two internal offset bias circuits cancel each other and introduce less net temperature drift coefficient change than offset voltage trimming techniques such as offset adjustment with an external trimmer potentiometer.

While programming, V+, VE1 and VE2 pins may be alternately pulsed with 12V (approximately) pulses generated by the EPAD Programmer. In-system programming requires the ALD2722E application circuit to accommodate these programming pulses. If needed, this requirement can be accomplished by adding resistors at certain appropriate circuit nodes.

## ABSOLUTE MAXIMUM RATINGS

Supply voltage, V+	_____	13.2V	
Differential input voltage range	_____	-0.3V to V+ +0.3V	
Power dissipation	_____	600 mW	
Operating temperature range	PB,SB package	_____	0°C to +70°C
	DB package	_____	-55°C to +125°C
Storage temperature range	_____	-65°C to +150°C	
Lead temperature, 10 seconds	_____	+260°C	

## OPERATING ELECTRICAL CHARACTERISTICS

T<sub>A</sub> = 25°C V<sub>S</sub> = ±5.0V unless otherwise specified

Parameter	Symbol	2724E			2724			Unit	Test Conditions
		Min	Typ	Max	Min	Typ	Max		
Supply Voltage	V <sub>S</sub>	±3.25		±5.25	±3.25		±5.25	V	Single Supply
	V+	6.5		10.5	6.5		10.5	V	
Input Offset Voltage <sup>1</sup>	V <sub>OS i</sub>		25	100		40	150	μV	R <sub>S</sub> ≤ 100KΩ
Offset Voltage Program Range <sup>2</sup>	ΔV <sub>OS</sub>	±5	±7		±0.5	±2		mV	
Programmed Input Offset Voltage Error <sup>3</sup>	V <sub>OS</sub>		25	100		40	150	μV	At user specified target offset voltage
Total Input Offset Voltage <sup>4</sup>	V <sub>OST</sub>		25	100		40	150	μV	At user specified target offset voltage
Input Offset Current <sup>5</sup>	I <sub>OS</sub>		0.01	10 240		0.01	10 240	pA pA	T <sub>A</sub> = 25°C 0°C ≤ T <sub>A</sub> ≤ +70°C
Input Bias Current <sup>5</sup>	I <sub>B</sub>		0.01	10 240		0.01	10 240	pA pA	T <sub>A</sub> = 25°C 0°C ≤ T <sub>A</sub> ≤ +70°C
Input Voltage Range <sup>6</sup>	V <sub>IR</sub>	-0.3 -2.8		5.3 +2.8	-0.3 -2.8		5.3 +2.8	V V	V+ = +5V V <sub>S</sub> = ±2.5V
Input Resistance	R <sub>IN</sub>		10 <sup>14</sup>			10 <sup>14</sup>		Ω	
Input Offset Voltage Drift <sup>7</sup>	TCV <sub>OS</sub>		5			5		μV/°C	R <sub>S</sub> ≤ 100KΩ
Initial Power Supply Rejection Ratio <sup>8</sup>	PSRR <sub>i</sub>		85			85		dB	R <sub>S</sub> ≤ 100KΩ
Initial Common Mode Rejection Ratio <sup>8</sup>	CMRR <sub>i</sub>		90			90		dB	R <sub>S</sub> ≤ 100KΩ
Large Signal Voltage Gain	A <sub>V</sub>		150			150		V/mV V/mV	R <sub>L</sub> = 10KΩ 0°C ≤ T <sub>A</sub> ≤ +70°C
Output Voltage Range	V <sub>O</sub> low V <sub>O</sub> high	4.99	-4.998 4.998	-4.99	4.99	-4.998 4.998	-4.99	V V	R <sub>L</sub> = 1MΩ V = 5V 0°C ≤ T <sub>A</sub> ≤ +70°C
	V <sub>O</sub> low V <sub>O</sub> high	4.90	-4.96 4.95	-4.90	4.90	-4.96 4.95	-4.90	V V	R <sub>L</sub> = 10KΩ 0°C ≤ T <sub>A</sub> ≤ +70°C
Output Short Circuit Current	I <sub>SC</sub>		15			15		mA	

\* NOTES 1 through 9, see section titled "Definitions and Design Notes".

**OPERATING ELECTRICAL CHARACTERISTICS (cont'd)**
**T<sub>A</sub> = 25°C V<sub>S</sub> = ±5.0V unless otherwise specified**

Parameter	Symbol	2724E			2724			Unit	Test Conditions
		Min	Typ	Max	Min	Typ	Max		
Supply Current	I <sub>S</sub>		5.0	6.5		5.0	6.5	mA	V <sub>IN</sub> = 0V No Load
Power Dissipation	P <sub>D</sub>			65			65	mW	V <sub>S</sub> = ±2.5V
Input Capacitance	C <sub>IN</sub>		1			1		pF	
Maximum Load Capacitance	C <sub>L</sub>		400 4000			400 4000		pF pF	Gain = 1 Gain = 5
Equivalent Input Noise Voltage	e <sub>n</sub>		26			26		nV/√Hz	f = 1KHz
Equivalent Input Noise Current	i <sub>n</sub>		0.6			0.6		fA/√Hz	f = 10Hz
Bandwidth	BW		2.1			2.1		MHz	
Slew Rate	S <sub>R</sub>		5.0			5.0		V/μs	A <sub>V</sub> = +1 R <sub>L</sub> = 2KΩ
Rise time	t <sub>r</sub>		0.1			0.1		μs	R <sub>L</sub> = 2KΩ
Overshoot Factor			15			15		%	R <sub>L</sub> = 2KΩ C <sub>L</sub> = 100pF
Settling Time	t <sub>S</sub>		2			2		μs	0.1% A <sub>V</sub> = -1 R <sub>L</sub> = 5KΩ C <sub>L</sub> = 50pF
Channel Separation	CS		140			140		dB	A <sub>V</sub> = 100

**T<sub>A</sub> = 25°C V<sub>S</sub> = ±5.0V unless otherwise specified**

Parameter	Symbol	2724E			2724			Unit	Test Conditions
		Min	Typ	Max	Min	Typ	Max		
Average Long Term Input Offset Voltage Stability <sup>9</sup>	$\frac{\Delta V_{OS}}{\Delta \text{time}}$		0.02			0.02		μV/ 1000 hrs	
Initial VE Voltage	VE1 <sub>i</sub> , VE2 <sub>i</sub>		1.4			2.5		V	
Programmable Change of VE Range	ΔVE1, ΔVE2	1.5	2.0			0.5		V	
Programmed VE Voltage Error	e(VE1-VE2)		0.1			0.1		%	
VE Pin Leakage Current	i <sub>eb</sub>		-5			-5		μA	

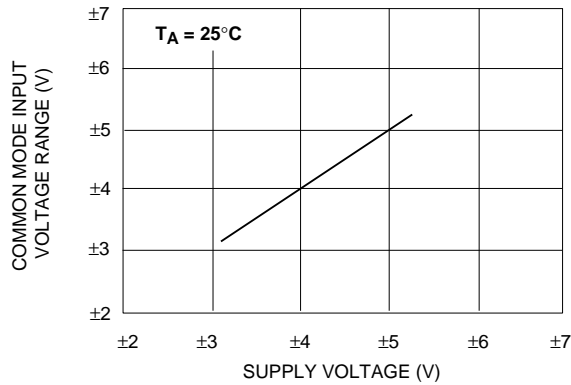
\* NOTES 1 through 9, see section titled "Definitions and Design Notes".

**V<sub>S</sub> = ±5.0V -55°C ≤ T<sub>A</sub> ≤ +125°C unless otherwise specified**

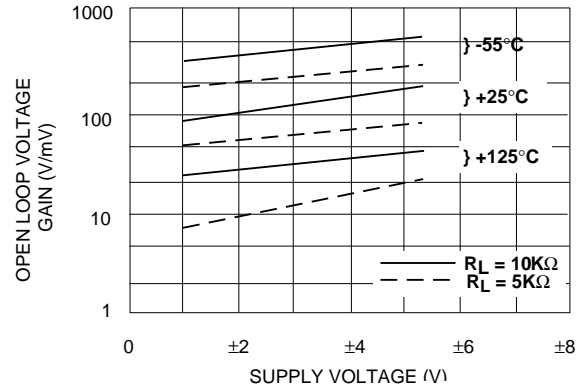
Parameter	Symbol	2724E			2724			Unit	Test Conditions
		Min	Typ	Max	Min	Typ	Max		
Initial Input offset Voltage	V <sub>OSi</sub>		0.7			0.7		mV	R <sub>S</sub> ≤ 100KΩ
Input Offset Current	I <sub>OS</sub>			2.0			2.0	nA	
Input Bias Current	I <sub>B</sub>			2.0			2.0	nA	
Initial Power Supply Rejection Ratio <sup>8</sup>	PSRR <sub>i</sub>		85			85		dB	R <sub>S</sub> ≤ 100KΩ
Initial Common Mode Rejection Ratio <sup>8</sup>	CMRR <sub>i</sub>		97			97		dB	R <sub>S</sub> ≤ 100KΩ
Large Signal Voltage Gain	A <sub>V</sub>	10	25		10	25		V/mV	R <sub>L</sub> = 10KΩ
Output Voltage Range	V <sub>O</sub> low V <sub>O</sub> high	4.8	-4.9 4.9	-4.8	4.8	-4.9 4.9	-4.8	V V	R <sub>L</sub> = 10KΩ

## TYPICAL PERFORMANCE CHARACTERISTICS

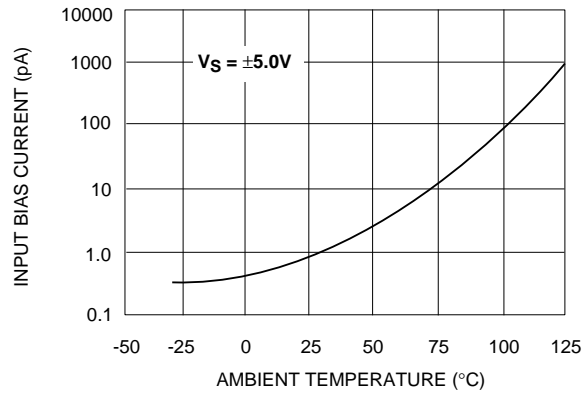
**COMMON MODE INPUT VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE**



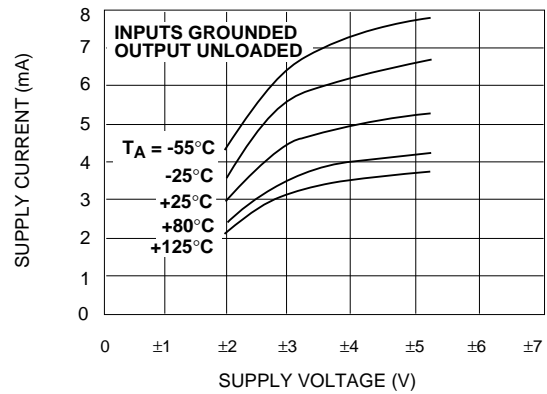
**OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE AND TEMPERATURE**



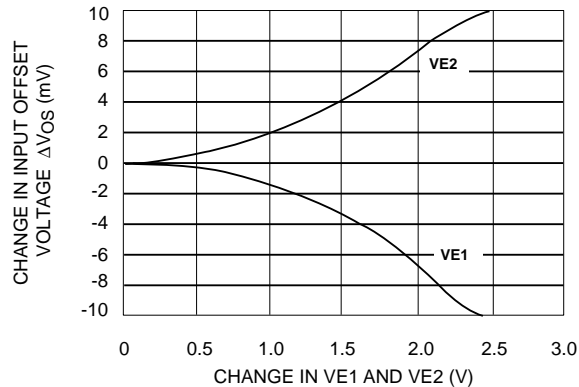
**INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE**



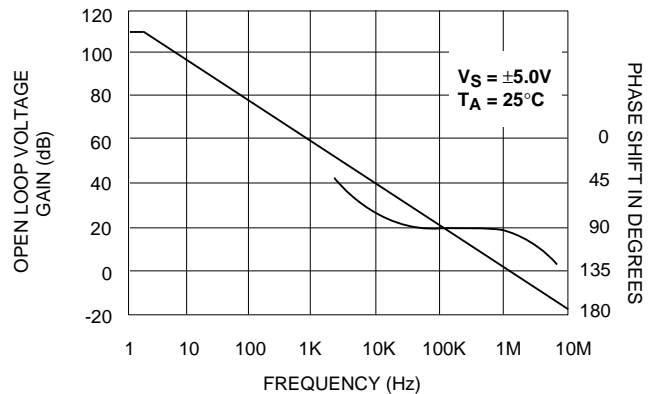
**SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE**



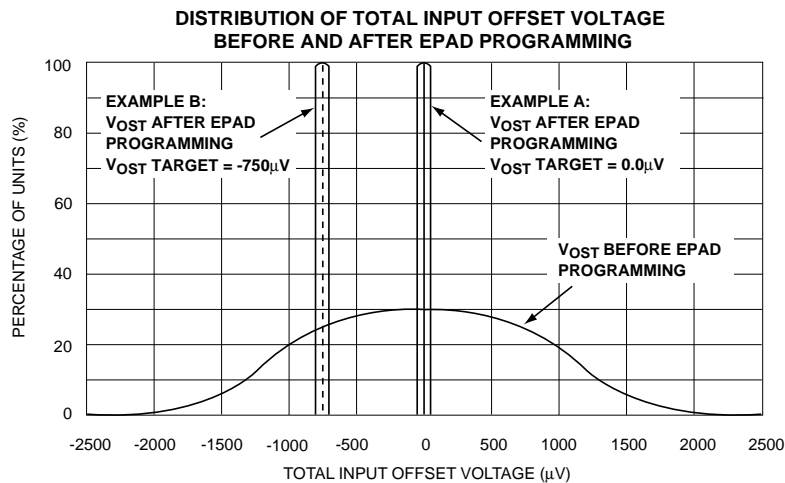
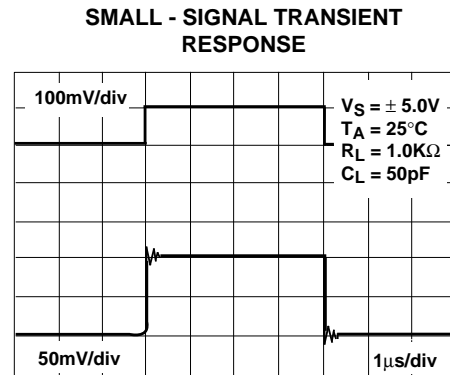
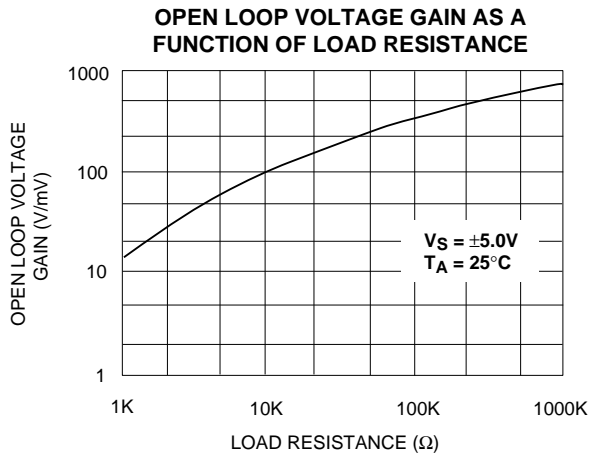
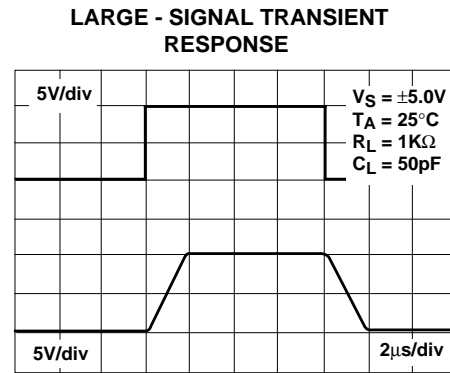
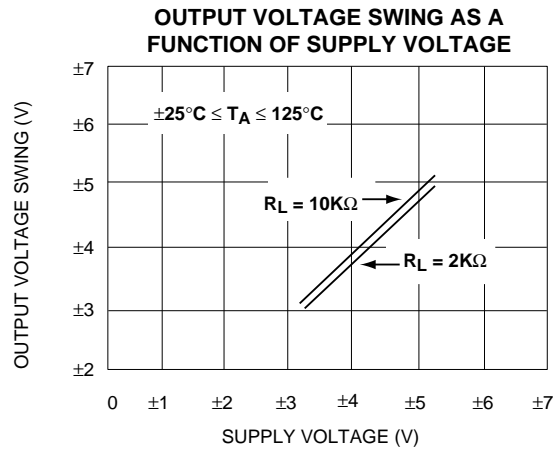
**CHANGE IN INPUT OFFSET VOLTAGE AS A FUNCTION OF CHANGE IN VE1 AND VE2**



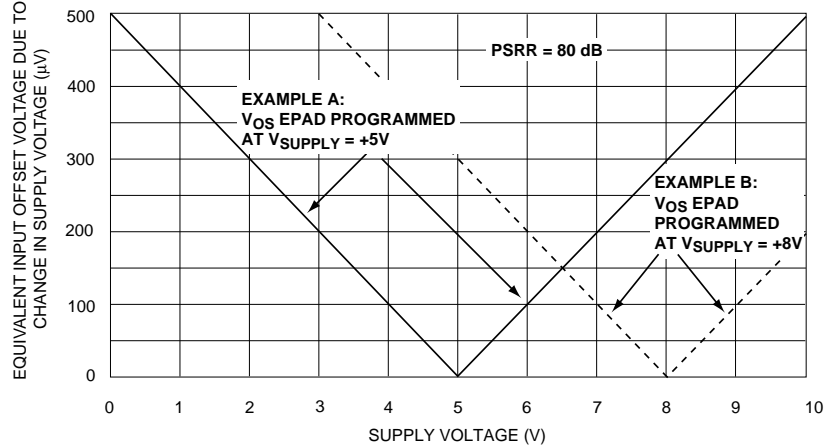
**OPEN LOOP VOLTAGE AS A FUNCTION OF FREQUENCY**



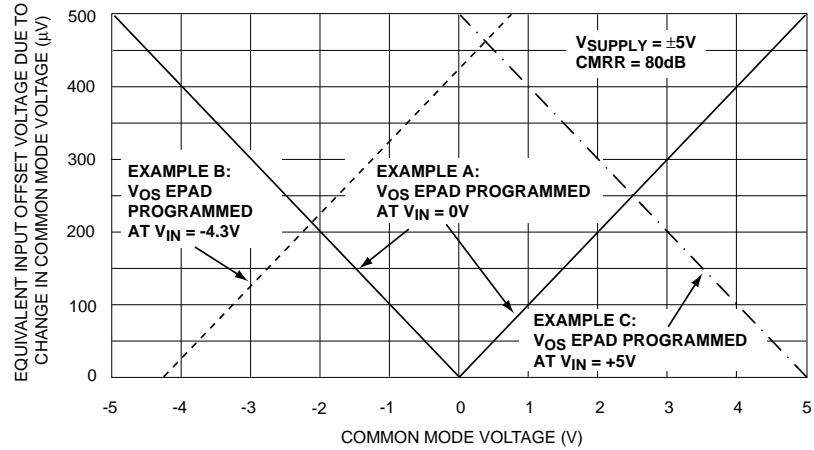
## TYPICAL PERFORMANCE CHARACTERISTICS



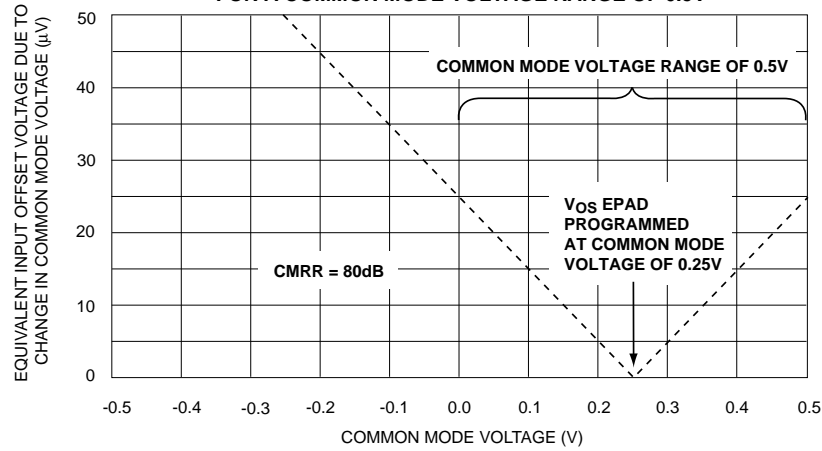
**TWO EXAMPLES OF EQUIVALENT INPUT OFFSET VOLTAGE DUE TO CHANGE IN SUPPLY VOLTAGE vs. SUPPLY VOLTAGE**



**THREE EXAMPLES OF EQUIVALENT INPUT OFFSET VOLTAGE DUE TO CHANGE IN COMMON MODE VOLTAGE vs. COMMON MODE VOLTAGE**



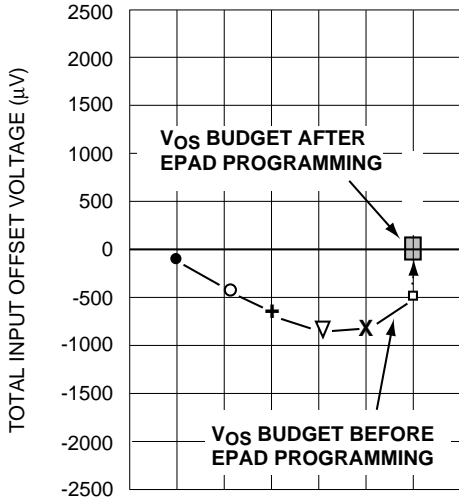
**EXAMPLE OF MINIMIZING EQUIVALENT INPUT OFFSET VOLTAGE FOR A COMMON MODE VOLTAGE RANGE OF 0.5V**



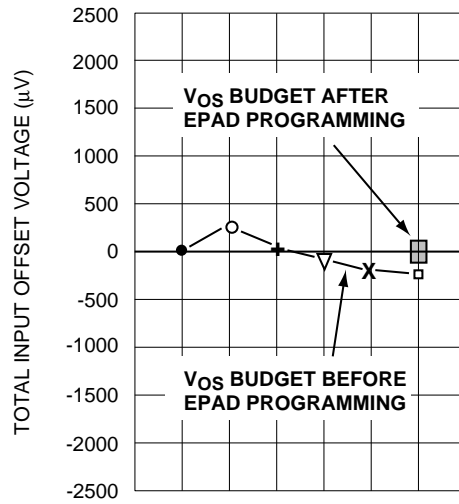


## APPLICATION SPECIFIC / IN-SYSTEM PROGRAMMING

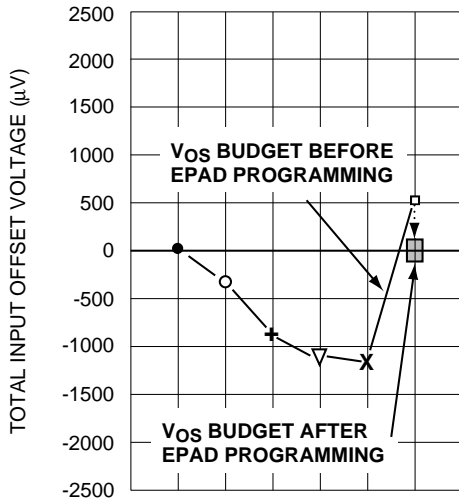
Examples of applications where accumulated total input offset voltage from various contributing sources is minimized under different sets of user-specified operating conditions



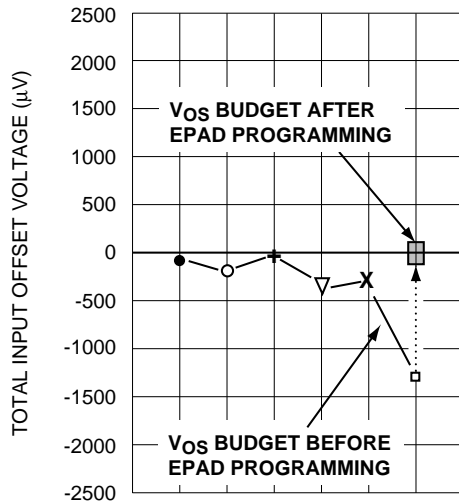
EXAMPLE A



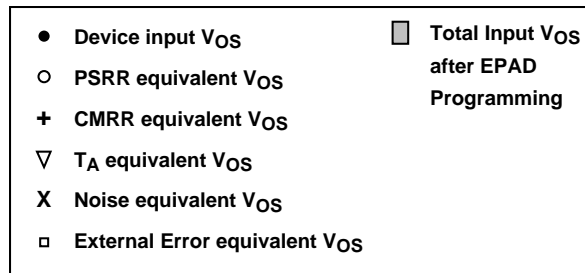
EXAMPLE B



EXAMPLE C



EXAMPLE D



## DEFINITIONS AND APPLICATION NOTES:

1. Initial Input Offset Voltage is the initial offset voltage of the ALD2724E/ALD2724 operational amplifier when shipped from the factory. The device has been pre-programmed and tested for programmability.

2. Offset Voltage Program Range is the range of adjustment of user specified target offset voltage. This is typically an adjustment in either the negative or positive direction of the input offset voltage from an initial input offset voltage. The input offset programming pins, VE1A/VE1B or VE2A/VE2B change the input offset voltages in the negative or positive direction, for each of the amplifier A or B, respectively. User specified target offset voltage can be any offset voltage within this programming range.

3. Programmed Input Offset Voltage Error is the final offset voltage error after programming when the Input Offset Voltage is at target Offset Voltage. This parameter is sample tested.

4. Total Input Offset Voltage is the same as Programmed Input Offset Voltage, corrected for system offset voltage error. Usually this is an all inclusive system offset voltage, which also includes offset voltage contributions from input offset voltage, PSRR, CMRR, TCV<sub>OS</sub> and noise. It can also include errors introduced by external components, at a system level. Programmed Input Offset Voltage and Total Input Offset Voltage is not necessarily zero offset voltage, but an offset voltage set to compensate for other system errors as well. This parameter is sample tested.

5. The Input Offset and Bias Currents are essentially input protection diode reverse bias leakage currents. This low input bias current assures that the analog signal from the source will not be distorted by it. For applications where source impedance is very high, it may be necessary to limit noise and hum pickup through proper shielding.

6. Input Voltage Range is determined by two parallel complementary input stages that are summed internally, each stage having a separate input offset voltage. While Total Input Offset Voltage can be trimmed to a desired target value, it is essential to note that this trimming occurs at only one user selected input bias voltage. Depending on the selected input bias voltage relative to the power supply voltages, offset voltage trimming may affect one or both input stages. For the ALD2724E/ALD2724, the switching point between the two stages occur at approximately 1.5V above negative supply voltage.

7. Input Offset Voltage Drift is the average change in Total Input Offset Voltage as a function of ambient temperature. This parameter is sample tested.

8. Initial PSRR and initial CMRR specifications are provided as reference information. After programming, error contribution to the offset voltage from PSRR and CMRR is set to zero under the specific power supply and common mode conditions, and becomes part of the Programmed Input Offset Voltage Error.

9. Average Long Term Input Offset Voltage Stability is based on input offset voltage shift through operating life test at 125°C extrapolated to T<sub>A</sub> = 25 °C, assuming activation energy of 1.0eV. This parameter is sample tested.

## DESIGN NOTES:

A. The ALD2724E/ALD2724 is internally compensated for unity gain stability using a novel scheme which produces a single pole roll off in the gain characteristics while providing more than 70 degrees of phase margin at unity gain frequency. A unity gain buffer using the ALD2724E/ALD2724 will typically drive 400pF of external load capacitance.

B. The ALD2724E/ALD2724 has complementary p-channel and n-channel input differential stages connected in parallel to accomplish rail-to-rail input common mode voltage range. The switching point between the two differential stages is 1.5V above negative supply voltage. For applications such as inverting amplifier or non-inverting amplifier with a gain larger than 2.5 (5V operation), the common mode voltage does not make excursions below this switching point. However, this switching does take place if the operational amplifier is connected as a rail-to-rail unity gain buffer and the design must allow for input offset voltage variations.

C. The output stage consists of class AB complementary output drivers. The oscillation resistant feature, combined with the rail-to-rail input and output feature, makes the ALD2724E/ALD2724 an effective analog signal buffer for high source impedance sensors, transducers, and other circuit networks.

D. The ALD2724E/ALD2724 has static discharge protection. Care must be exercised when handling the device to avoid strong static fields that may degrade a diode junction, causing increased input leakage currents. The user is advised to power up the circuit before, or simultaneously with, any input voltages applied and to limit input voltages not to exceed 0.3V of the power supply voltage levels.

E. V<sub>Exx</sub> are high impedance terminals, as the internal bias currents are set very low to a few microamperes to conserve power. For some applications, these terminals may need to be shielded from external coupling sources. For example, digital signals running nearby may cause unwanted offset voltage fluctuations. Care during the printed circuit board layout to place ground traces around these pins and to isolate them from digital lines will generally eliminate such coupling effects. In addition, optional decoupling capacitors of 1000pF or greater value can be added to V<sub>Exx</sub> terminals.

F. The ALD2724E/ALD2724 is designed for use in low voltage, micropower circuits. The maximum operating voltage during normal operation should remain below 10 Volts at all times. Care should be taken to insure that the application in which the device is used do not experience any positive or negative transient voltages that will cause any of the terminal voltages to exceed this limit.

G. All inputs or unused pins except V<sub>Exx</sub> pins should be connected to a supply voltage such as Ground so that they do not become floating pins, since input impedance at these pins is very high. If any of these pins are left undefined, they may cause unwanted oscillation or intermittent excessive current drain. As these devices are built with CMOS technology, normal operating and storage temperature limits, ESD and latchup handling precautions pertaining to CMOS device handling should be observed.